Area-Efficient Low-Cost Low-Dropout Regulators Using MOS Capacitors

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***Abstract*—Traditional design of low-dropout regulators offers the use of metal-insulator-metal (MIM) compensation capacitors to prevent instability in the absence of load capacitor with equivalent series resistance (ESR). In addition to area efficiency achieved by replacing these capacitors with MOS transistors, the location of implanted transfer function poles and zeros are adaptively changed according to the value of load current. The idea has been applied to stabilize a 1.2V, 100mA low-dropout regulator in a 0.18µm CMOS n-well process. Using the proposed technique, the regulator meets stability with a small 100pF MOS output capacitor and no ESR.**

I. INTRODUCTION

The increasing demand for portable battery-operated products presents power management designers with new challenges. To increase battery-life and to achieve better power efficiency, low-dropout regulators (LDOs) are essential. Unfortunately, the tradeoff between stability and dropout voltage of linear regulators makes uncompensated LDOs potentially unstable. Conventional LDOs employ the ESR of an off-chip capacitor to stabilize the closed-loop circuit. This resistor introduces a left-half-plane (LHP) zero to the loop-gain transfer function which counteracts the additional negative phase shift introduced by one of the two dominant poles. ESR-based compensation, however, has serious drawbacks. The large capacitor at the output can not be integrated. Its ESR strongly depends on temperature and capacitor type. There are additional transient voltage ripples originated from ESR, bond wires and so forth. Concerning these issues, compensation solutions relying on integrated components are becoming popular [1, 2].

It is very desirable to integrate the analog portion of a large mixed-signal system in standard digital CMOS technologies with no analog features. Digital circuits, as the major part of a state-of-the-art signal processing system, require only a single poly layer for the gates. However, in order to implement constant capacitors for analog applications, a second poly or extra metal layers are introduced into the process, resulting in significant increase in fabrication cost. Furthermore, although available metal layers in mixed-signal technologies can be utilized for MOM (metal-oxide-metal) capacitors, due to the relatively lower scaling rate of the oxide between these layers, the occupied physical area is noticeable [3]. Besides, a parasitic capacitance will exist between the bottom plate of an MOM capacitor and substrate.

To avoid these constraints, one of the possible solutions is to employ MOS gate junctions as capacitor. The gate oxide is thin and compared to MIMs, CMOS capacitors called MOSCAPs have larger capacitance per unit area. The main problem in largely exploiting MOSCAPs in analog applications is due to linearity issues. This is because of different regions a MOSFET experiences when its gate-bulk voltage varies. The regions, shown in Fig. 1, are accumulation, depletion and inversion [4]. For small bias voltages, the transistor is working in depletion thereby leaving the capacitor a function of the gate-bulk voltage. This degrades overall performance and mostly adds complexity to the design of analog circuits [4, 5]. Interestingly, the type of nonlinearity a MOSCAP has can be even helpful in improving the linearity of an LDO. Traditionally-designed LDOs suffer from load-dependent stability due to the variation of load current. Hence the frequency response is only optimized for a particular load current. Frequency compensation based on load-dependent zeros has therefore been proposed to fairly mitigate this issue [6]. The location of each pole or zero in loop transfer function is inversely proportional to the product of a resistance and capacitance.

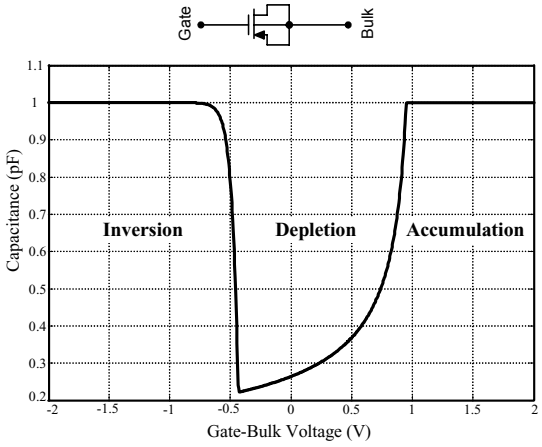

Figure 1. *C-V* charastristic of a p-Channel MOSFET

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Hence load-dependent zeros are produced using variable resistors realized by MOSFETs operating in triode [6]. However, another way to define the location of zeros (even poles) can be based on the variable capacitors. In this paper, we are going to demonstrate the capability of MOSCAPs in fully integrating LDOs in conventional digital technologies.

II. LDO DESIGN USING MOS CAPACITORS

Practically speaking, depletion-mode MOSCAPs can be widely utilized in deep sub-micron technologies [4]. Whenever required, non-linearity compensation techniques can be utilized. Fig. 2 shows a serial-compensated depletion-mode MOSCAP (SCDM) using three transistors. The gates of the two input transistors are connected to ground via a large resistance. Fig. 3 shows the *C-V* diagram of the result [4]. Compared to the uncompensated MOSCAP illustrated in Fig. 1, linearity is meaningfully improved but at the expense of more silicon area.

System-level architecture of an LDO consists of an error amplifier, a pass device, feedback network and a bandgap reference. Fig. 4 shows a possible circuit-level implementation of an LDO along with frequency compensation. Two compensation capacitors, namely C_{C1} and C_{C2}, are intended to properly shape the frequency response of the circuit. Fig. 5 shows the corresponding small-signal equivalent circuit. Assuming R_{C1} to be large, the effect of C_{C1} on the first stage output via i_C is negligible because of the relatively low induced ac current. The transfer function is thus obtained as follows:

$$\frac{V_{fb}}{V_{in}} \approx \frac{LG_0(1+s/z_1).(1+s/z_2)}{(1+s/p_1).(1+s/p_2).(1+s/p_3).(1+s/p_4)}, \quad (1)$$

where:

$$LG_0 = g_{mi}g_{mS}g_{mL}R_iR_S(R_L \,\|\, (R_{F1}+R_{F2}))\frac{R_{F2}}{R_{F1}+R_{F2}}, \quad (2)$$

$$z_1 = 1/R_{C1}C_{C1}, \quad (3)$$

$$z_2 = 1/(R_{C2} - 1/g_{mP})C_{C2}, \quad (4)$$

$$p_1 = 1/R_S(C_S + C_{C2}(1+g_{mP}(R_L \,\|\, (R_{F1}+R_{F2})))), \quad (5)$$

$$p_2 = 1/((R_L \,\|\, (R_{F1}+R_{F2}) \,\|\, R_S)(C_S + C_L)), \quad (6)$$

$$p_3 = 1/R_iC_i, \quad (7)$$

$$p_4 = 1/(C_S + C_{C2})(R_{C1} \,\|\, R_S). \quad (8)$$

C_{C2} dominates the pole at the input of pass device (i.e. p_1) and pushes output pole (p_2) to relatively higher frequencies (well-known pole-splitting action in Miller compensation [3]). R_{C2} in series with C_{C2} creates a LHP zero (z_2) which cancels out the undesirable effect of high frequency poles (p_3, p_4). As C_{C2} is SCDM and R_{C2} is constant, the magnitude of z_2 is not affected by the ripples of output due to load current changes. This is not however true for C_{C1} which is an uncompensated MOSCAP.

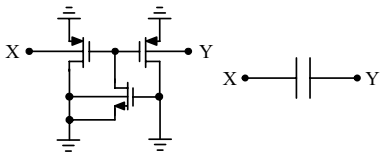

Figure 2. A serial-compensated depletion-mode (SCDM) MOS capacitor

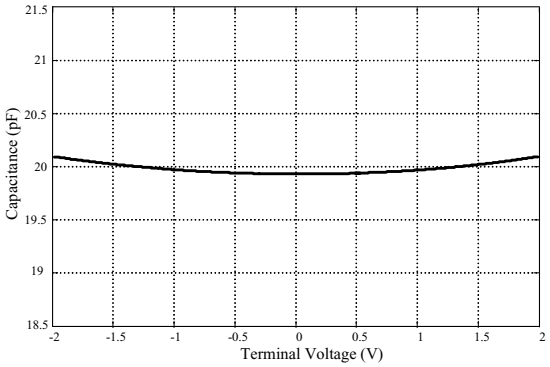

Figure 3. *C-V* charastristic of Fig. 2 (W/L = 1180μ/20μ)

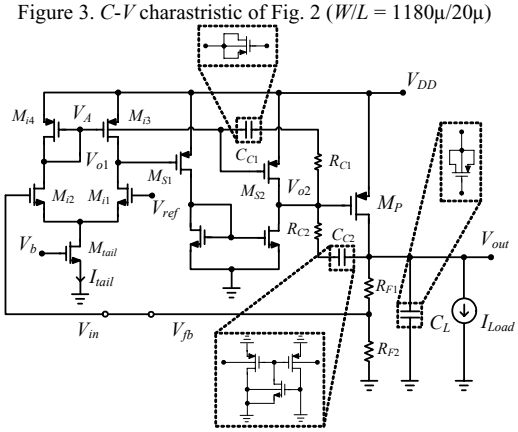

Figure 4. Detailed schematic of MOSCAP-compensated LDO

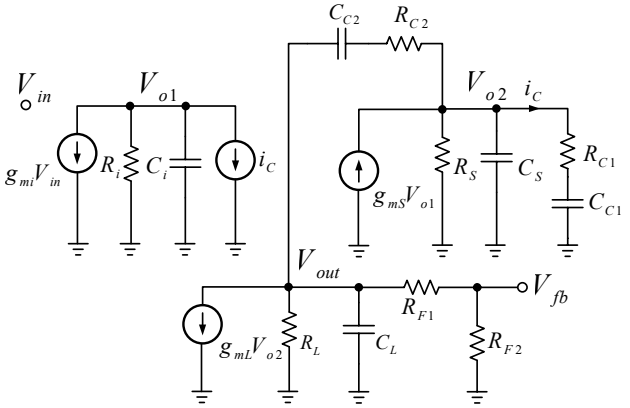

Figure 5. The equivalent small-signal circuit of the loop

As a result, z_1 which is produced by this capacitor becomes a function of the load current. The LHP pole located at the output of LDO increases linearly with the load current according to the following well-known expression [6]:

$$p_2 \approx 1/r_{DSp}C_L = \lambda_p I_{Load}/C_L, \quad (9)$$

where r_{DSp} and λ_p are the output resistance and channel length modulation of pass device, respectively. The zero introduced by C_{C1} is intended to counteract the phase lag introduced by this pole. Based on the well-known *I-V* relation of a MOSFET, the DC component of V_{o2} and V_A are respectively given by:

$$V_{o2} = V_{DD} - |V_{Tp}| - \sqrt{\frac{2I_{Load}}{\mu_p C_{ox}(W/L)_p}}, \quad (10)$$

$$V_A = V_{DD} - V_{SG,i3} = V_{DD} - |V_{Tp}| - \sqrt{\frac{I_{tail}}{\mu_p C_{ox}(W/L)_{i4}}}. \quad (11)$$

μ_p, C_{ox}, $(W/L)_p$ and $(W/L)_{i4}$ are the hole mobility, gate capacitance per unit area and aspect ratio of pass device and M_{i4} respectively. The gate-bulk voltage of C_{C1} (V_{gb}) is therefore expressed as:

$$V_{gb} = V_{o2} - V_A = \sqrt{\frac{I_{tail}}{\mu_p C_{ox}(W/L)_{i4}}} - \sqrt{\frac{2I_{Load}}{\mu_p C_{ox}(W/L)_p}}, \quad (12)$$

This equation shows that V_{gb} is proportional to the square root of I_{Load}. To force C_{C1} working in depletion for the entire range of the load current, V_A can be properly set. If this is done, the capacitor value can be approximated as $a(V_{gb}+b)^2 + c$ where *a*, *b* and *c* are constant (see Fig. 1). Hence:

$$C_{C1} = a\left(\sqrt{\frac{I_{tail}}{\mu_p C_{ox}(W/L)_{i4}}} - \sqrt{\frac{2I_{Load}}{\mu_p C_{ox}(W/L)_p}} + b\right)^2 + c, \quad (13)$$

When I_{Load} increases, to account for the variations of p_2, (13) shows that C_{C1} decreases to push z_1 into higher frequencies. The decrease in C_{C1} however is limited by the difference between minimum and maximum values of C_{C1} in depletion.

It is also important to investigate the effect of power supply on the location of poles and zeros because stability must be independent of V_{DD}. For a particular load current, the source-gate voltage of pass device is constant. Hence V_{o2} follows the variations of V_{DD}. C_{C2}, as an SCDM, is not indeed affected by this phenomenon because its absolute value is almost independent of the operating point (Fig. 3). This is the reason why an SCDM with minor variations is employed for realizing this capacitor. C_{C1}, on the other hand, is dependent on its operating point. Nevertheless, the terminal voltage of this capacitor is as well independent of V_{DD} because the input stage of error amplifier is biased with constant current, I_{tail}. Hence nodes V_A and V_{o2} are both V_{SG} lower than the V_{DD} in which V_{SG} is independent of power supply.

Almost all state-of-the-art LDOs require an on-chip capacitor at the output (C_L in Fig. 4) for enhancing ac and transient responses. MIMs are conventionally employed to implement this capacitor. As an alternative approach, C_L can be an uncompensated MOSCAP with higher density. Fig. 6 shows the C-V diagram of the 100pF integrated output capacitor used in the proposed LDO. Output voltage is large enough to maintain the operating point in accumulation or perhaps inversion. Furthermore, the output is always under regulation to have minor variations in magnitude. This guarantees the fact that C_L is mostly remained in voltage-independent regions under different transient conditions. Employing such a capacitor at the output is very important to significantly reduce silicon area and overall cost. No change in circuit performance of the circuit is observed when 100pF MIM capacitor of initial design is replaced with its equivalent uncompensated MOSCAP. However, the area efficiency is considerable (100000 μm^2 vs. 18000 μm^2 in our technology).

III. Design Example

The LDO shown in Fig. 4 has been simulated in a 0.18µm CMOS digital process. Table I summarizes the performance of the circuit for C_L=100pF.

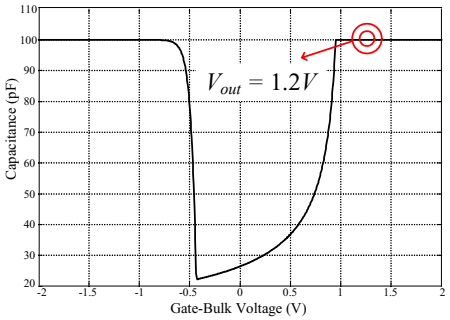

Figure 6. *C-V* diagram of the load capacitance (W/L = 590µ /20µ)

TABLE I. Performance Summary with C_L = 100pF

Technology	0.18µm Standard Digital Technology	
Output Voltage		1.2V
Dropout Voltage		0.2V
Maximum Load Current		100 mA
DC Load Regulation (V_{DD} = 1.4V, I_{Load} = 0.01-100mA)		16 µV/mA
DC Line Regulation (V_{DD} = 1.4-3.4V)	**I_{Load} = 100µA**	0.8mV/V
	I_{Load} = 100mA	1mV/V
Quiescent Current	**I_{Load} = 100µA**	54 µA
	I_{Load} = 100mA	83 µA
Transient Settling Time (at 0.1% error)	**Load (0.01mA –100mA V_{DD} = 1.4V)**	835ns + 1350ns -
	Line (V_{DD} = 1.4-3.4V I_{Load} = 100µA)	280 ns
	Start-up (V_{DD} = 1.4V I_{Load} = 100mA)	295 ns

It requires a 0.9V bandgap reference for regulation. Fig. 7 shows the load-transient response of the circuit for a 100mA current step. The 0.1% settling error is 835ns and 1350ns for positive and negative edges. The line-transient response when V_{DD} changes from 1.4V to 2V is illustrated in Fig. 8. Fig. 9 depicts the start-up transient response for the case of dropout voltage and 100mA load current. During the start-up, the MOSCAP load capacitance changes from 26pF to 100pF when the output settles down to its final value (Fig. 6). Hence, the start-up transient response is non-linear. Nevertheless, simulations show that this variable C_L has even a positive

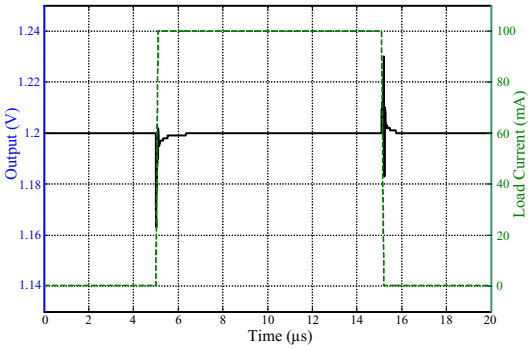

Figure 7. Load-transient response for 100 mA load current change

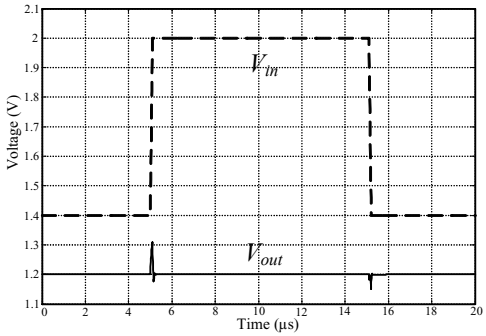

Figure 8. Line-transient response for 0.6V V_{DD} pulse (C_L = 100pF)

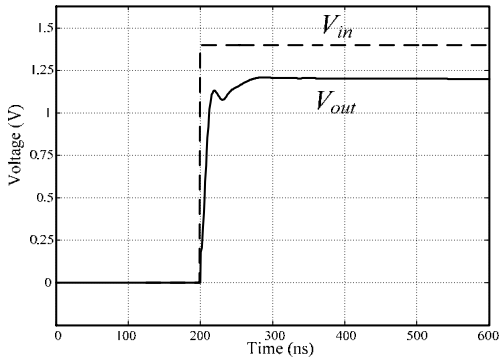

Figure 9. Start-up response for $V_{Dropout}$ = 0.2V (C_L = 26~100pF)

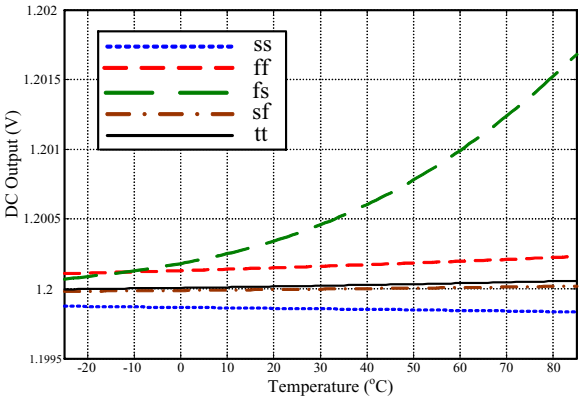

Figure 10. DC output as a function of process and temperature corners [-25ºC, 85ºC], where ss: slow *n*MOS slow *p*MOS; ff: fast *n*MOS fast *p*MOS fs: fast *n*MOS slow *p*MOS sf: slow *n*MOS fast *p*MOS; tt: typical condition

effect on start-up settling time because a smaller load is driven by the circuit when beginning operation. At last, the integrity of the circuit is confirmed in process and temperature corners. Fig. 10 shows the DC output in different conditions.

IV. Conclusion

Integrating all building blocks and reducing the physical area, while achieving the same or better performance, is an important task towards cheaper System-on-Chip (SoC) systems. An efficient way to stabilize the transient response of low-dropout regulators is proposed in this paper. It is based on MOS capacitors which have compact size and are available in all standard digital technologies. Detailed explanations to properly employing the capacitors are given. Realizing the output capacitor, by an uncompensated area-efficient MOSFET is a general viable idea proposed here. It can be applied to all integrated low-cost low-dropout regulators.

References

[1] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[2] R. J. Milliken, J. S. Martinez, and E Sanchez-Sinencio, "Full on-chip low-dropout voltage regulator," *IEEE Trans. Circuits Systems*, vol. 54, no. 9, pp. 1879-1890, Sep. 2007.

[3] G. A. Rincon-Mora, "Active capacitor multiplier in Miller compensated circuits," *IEEE J. of Solid-state Circuit*s, vol. 35, no. 1, pp. 26-32, Jan 2000.

[4] T. Tille, *et al*. "Design of low-voltage MOSFET-only sigma-delta modulators in standard digital CMOS technology," *IEEE Trans. Circuits Systems*, vol. 51, no. 1, pp. 96-109, Jan. 2004.

[5] H. Aminzadeh, M. Danaie, and R. Lotfi, "Design of high-resolution MOSFET-only pipelined ADCs with digital calibration," *IET Design, Automation and Test in Europe (DATE'07)*, pp. 427-432, Apr. 2007.

[6] K. C. Kwok and P. K. T. Mok, "Pole-zero tracking frequency compensation for low dropout regulator," *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 735-738, May 2002.