Simulation-Equation-Based Methodology for Design of CMOS Amplifiers Using Geometric Programming

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***Abstract*—Geometric Programming (GP) has been employed in automatic design of analog integrated circuits. Its major advantage is the ability to find the globally optimum solution to a problem. It however, suffers from dependency on the accuracy of the initial equations and the parameters used in these equations. This, in circuit design, causes discrepancies between GP predictions and simulation results - especially in sub-micron devices - thus resulting in a non-globally optimum circuit design. In this paper, two major sources of this discrepancy are introduced and resolved by an iterative simulation-equation-based design methodology based on GP for operational amplifiers. In order to show the effectiveness of the methodology, it has been applied to two op-amp architectures.**

I. INTRODUCTION

As the demand for high-speed and accurate mixed-signal integrated circuits is increasing, the design of analog circuits such as operational amplifiers (op-amps) is becoming more challenging. Digital designers have developed suits of optimization tools that have helped them enhance productivity. Likewise Computer-Aided-Design (CAD) tools have been of increasing demand in the recent years in the field of analog integrated circuits. There has been extended research in the area of computer aided design of analog circuits. Three main approaches used are equation-based, simulation-based and simulation-equation-based methods.

Equation-based methods like [1] simplify the circuit equations and device models into first or second order estimations and use global optimization techniques like Geometric Programming (GP) for the circuit design. Employing geometric programming has attracted considerable attention by applying its global optimization method in CMOS op-amps and other building blocks of analog circuits [1]. The major limitation of this approach is the incapability of handling non-convex problems, which can be critical in many cases and cause some errors between GP prediction and simulation results especially in deep-submicron devices. CADs that are developed based on these methods solve the optimization problem fast and usually can find the global-optimized solution of the equations but simplified equations can not show the higher order effects which can be rather important for deep-submicron CMOS processes. Thus the achieved optimal solution can deviate substantially from the real optimum circuit.

Simulation-based methods [2] use more complicated circuit models to improve accuracy. They use classical optimization methods like steepest descent and Lagrange multiplier methods. These methods can handle a wide variety of problems which is their main advantage. The main disadvantage of these methods is that most of them find locally optimal designs.

Simulation-equation-based methods, utilized recently in GBOPCAD (Gain Boosting Opamp CAD) [3] and ISECAD (an Iterative Simulation-Equation-Based CAD) [4], gain the benefits of equation-based approaches and that of the simulation-based methods, while avoiding their shortcomings by combining the characteristics of both methods. These methods, also, provide only the locally optimal designs.

In this paper, an innovative method based on an iterative simulation-equation-based approach between circuit simulation and GP core will be presented. First, the solutions to the initial equations (circuit sizes) are obtained based on a metric-optimized methodology according to the desired application such as power optimization. The mentioned initial equations are implemented based on initial assumptions of transistor variables such as carrier mobilities. Next, using these transistor sizes, SPICE simulation is performed and the results are evaluated. According to the simulation results, the initial parameters and equations are corrected and the new circuit parameters are extracted from the corrected equations and this process will continue to reach the required circuit specifications with desired error between GP core prediction and simulation results. We choose MOSEK [5], an optimization tool which is run in MATLAB, as the GP analytical tool and Hspice for the evaluation tool. We developed a code for the interface between them for the purpose of solving the equations, evaluating the circuit and repeating this process automatically.

The organization of the rest of this paper is as follows. In section II geometric programming will be described briefly. Previous reports in the field of analog integrated circuits will be reviewed in section III. Section IV describes the transistor model which is used in this paper, furthermore optimization of a telescopic cascode op-amp will be presented. Also in this section, major sources of discrepancies and the use of an iterative method to solve the problems they cause is pointed out. In section V a design example for a widely-used architecture (two-stage amplifier) is explained. Finally, concluding remarks are presented in the last section.

II. GEOMETRIC PROGRAMMING

Geometric programming is a type of mathematical optimization problem characterized by objective and

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constraint functions that have special forms. A GP problem has the following format:

$$\begin{aligned} &Minimize\ \ f_\circ(x) \\ &Subject\ to\ \ f_i(x) \le 1 \qquad i = 1,....,m \\ &\qquad\quad g_i(x) = 1 \qquad i = 1,....,p \\ &\qquad\quad x_i \rangle 0 \qquad\ \ i = 1,....,n \end{aligned} \tag{1}$$

where $f_i(x)$ are posynomial functions and $g_i(x)$ are monomial ones. A posynomial function is defined as:

$$f(x_1,...,x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_1 k} x_2^{\alpha_2 k} ... x_n^{\alpha_n k} \qquad \begin{matrix} c_j \ge \circ \\ \alpha_{ij} \in R \end{matrix} \tag{2}$$

This function has a real value and consists of n real, positive variables i.e. x_i with non-negative coefficients and any real exponents. Mononomial functions are forms of posynomial functions where there is only one term in the sum. If $c_j \varepsilon R$, then (2) represents a signomial function. Geometric programming can change to a convex form by considering the logs of the function involved i.e., the problem of minimizing a convex function subject to convex inequality constraints and linear equality constraints. This is the key to globally and efficiently solving a geometric programming problem. Although there are several options for solving geometric program problems, probably one of the most efficient GP special purpose solvers is the sophisticated primal dual interior-point methods used in linear programming [1].

III. Previous Works

Previous works consist of developing CAD tools for designing various configurations of operational amplifiers and also improving the accuracy of analog circuit design optimization tools. As reported in [1] we can produce excellent prediction from GP-Based design in long-channel transistors. In [6], a similar work to [1] has been done independently and in parallel to previous work. However compared to [1] their technique addressed second-order effects and is far less restrictive in terms of range of MOS models it supported. Accuracy of performance prediction in the sizing program is mentioned by doing iteration between optimization core and SPICE simulation using a proposed MOS model (*α-A* model). Although both previous reports produced excellent results in long-channel devices, the prediction from GP-based optimization in the short-channel regime can deviate considerably from SPICE simulation.

Reference [7] presented an approach for improving the accuracy of geometric-programming-based analog circuit design optimization especially in deep-submicron devices. They described major sources of discrepancies between the results from optimization and simulation and proposed several methods to reduce the error. Device modeling based on convex piecewise-linear function fitting is introduced to create accurate active and passive device models.

All of the reviewed works above can handle posynomial functions only, but in [8] a technique had been presented to automatically generate posynomial and signomial performance models from full-accuracy SPICE simulations. The latter can be employed in automatic circuit sizing using highly efficient interior-point geometric programming algorithms. They used standard mathematical fitting techniques to model the input-output relationship of circuit which is called performance modeling. The advantage of their fitting is that no intrinsic system knowledge is needed. The model built from this approach is called "black-box" fitting. This approach reduced the time and the effort needed to generate posynomial models to a strict minimum.

In this report, following [7], we show that discrepancies between GP predictions and simulation results in deep-submicron devices can be eliminated by an iterative simulation-equation-based method. It is important to note that the method proposed in this paper is much simpler than the one described in [7]. First we apply our method to a fully differential telescopic cascode amplifier with active load, and explain the presented idea then we will return to this discussion in section V to design more complicated op-amp topology which is known as two-stage op-amp. We have used 0.18–µm TSMC CMOS process model in the presented work.

IV. Optimization of Telescopic Cascode Architecture

A. Transistor Modeling

The transistor model used in this paper for the purpose of GP equation-based optimization has the following simple form:

- The transconductance $g_m = \sqrt{2I\mu_n c_{ox} W / L(1+\lambda V_{DS})}$ is a monomial function of L, W and I.
- The output impedance is given by $g_o = (A\frac{L}{I})^{-1}$, where A is a constant which relates to some parameters of quiescent point such as V_{DS}.
- The overdrive voltage which is monomial function of L, W and I and is: $V_{ov} = \sqrt{\frac{2I}{\mu_n c_{ox} W / L(1+\lambda V_{DS})}}$

This traditional long-channel model fits exactly the format level 1 in Hspice. In level 1 model, second-order effects such as mobility degradation and hot carrier effects have not been taken into consideration, but in 0.18-µm library, used for our simulations, which is considered as deep-submicron one, these short-channel effects occur. These short-channel effects, which are not directly taken into account in the above equations, cause the optimized circuit's Hspice simulation results (Gain, BW, etc.) not to match the purely-equation-based predictions made by GP. This disqualifies the equations the GP optimization was based on thus disqualifying the circuit from being the globally optimum circuit. Here, we try to show that by doing iteration between GP core and Hspice, we can converge the transistor variables such as carrier mobility and A (see the output impedance equation), which will be called convergence parameters from this point on. The final values of the convergence parameters are obtained through an iterative process which sets the error between GP predictions and Hspice simulation less than a desired value, let's say 10%. This validates the equations and thus validates the final globally optimized design.

B. Op-amp Topology

Now we concentrate on telescopic-cascode op-amp which

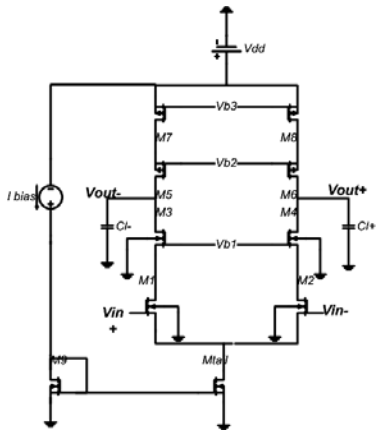

Fig. 1. Fully differential telescopic cascode op-amp

is depicted in Fig. 1, and assume a simple MOS model. Symmetry and matching, device sizing, current equations, bias conditions, quiescent power, open-loop DC gain and unity-bandwidth equations are reported in [1] and we do not rewrite them for the sake of space.

As mentioned before, secondary effects are also considered in this report. One of them is body effect which affects the threshold voltage of transistors and hence I_D. Therefore:

$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{gs} - V_{TH0} + \gamma(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|})^2(1+\lambda V_{DS}) \quad (3)$$

It is clear that the value of V_{SB} can affect the value of I_D hence g_m. Now we define g_{mb} parameter as follows:

$$g_{mb} = \frac{\partial I_D}{V_{BS}} = \mu_n c_{ox}\frac{W}{L}(V_{gs} - V_{TH})(-\frac{\partial V_{TH}}{V_{BS}}) \quad (4)$$

$$= g_m \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}} = \eta g_m$$

If we use small-signal model for this circuit, the voltage gain expression would be:

$$A_V = g_{m1}(\alpha g_{m3} r_{o3} r_{o1} \| g_{m5} r_{o5} r_{o7}) \quad (5)$$

where α is 1+η. Value of η will be updated in each iteration.

Now we try to optimize the circuit of Figure 1 in the 0.18-µm CMOS process with these constraints:

$$\begin{aligned} &Minimize\ \ Power\ \ Dissipation \\ &Subject\ \ to\ \ A_V \geq 70db \\ &\quad BW \geq 628Mrad/s \\ &\quad V_{ovtail} + V_{ov1} + V_{ov3} \leq 0.75 \\ &\quad V_{ov5} + V_{ov7} \leq 0.5 \\ &\quad C_L = 1pF \\ &\quad 0.18\mu m \leq L \leq 0.5\mu m \\ &\quad 0.5\mu m \leq W \leq 500\mu m \\ &\quad SlewRate \geq 20V/\mu s \\ &\quad V_{dd} = 1.8V \end{aligned} \quad (6)$$

In this example we have 8 variables which are transistor sizes and the bias current: W_1, W_3, W_5, W_7, W_{tail}, L, L_{tail} and I_{tail}. In order to make the voltage gain expression posynomial,

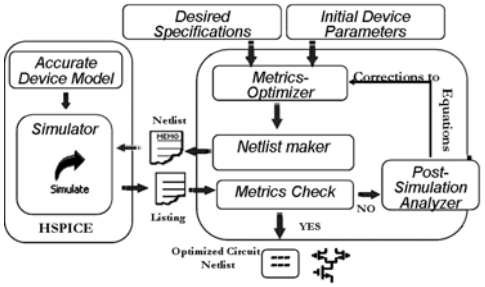

Fig. 2. General overview of proposed methodology

all transistors except the mirror one have the same channel length. The objective of this optimization is minimizing the power dissipation subject to the other given constraints. Two major sources of equation-based results and simulation results discrepancies in sub-micron devices are carrier mobility and output impedance variations. We consider them as an error factor and try to modify them in related matrices which are written in MOSEK, in order to make the error between GP and Hspice output less than a desired value. As shown in Fig. 2 the desired op-amp specifications, the transistor model equations and the initial device parameters which include the convergence parameter are given to MOSEK for the sake of calculating a globally-optimized circuit. The values of the convergence parameters are initially assumed as suitable values by the user, to be corrected through iterations. MOSEK calculates transistor sizes and bias current with given device parameters. Then MATLAB is called upon to prepare the op-amp netlist according to the MOSEK-calculated transistor sizes and bias current values and to call Hspice to simulate the op-amp. After simulation of Hspice, the output file will be scanned by MATLAB and measured metrics such as DC gain, UGF and power dissipation will be extracted. Then MATLAB is used again to analytically compare the simulation results and the GP equation-based predicted results, in this round of iteration, through which corrections to the convergence parameters will be applied. The new set of convergence parameters will be used in another round of optimization process as explained above. These iterations are repeated until the difference between simulated metrics and GP prediction satisfy the desired error. Gain error and bandwidth error are defined as follows:

$$Gerror = \frac{|A_{sim} - A_{MAT}|}{A_{sim}} \times 100 \quad (7)$$

$$BWerror = \frac{|BW_{sim} - BW_{MAT}|}{BW_{sim}} \times 100 \quad (8)$$

It is worth saying that if the values of the convergence parameters in the first round which are assumed by the user are far from suitable values, the proposed procedure may not converge.

C. Simulation Results

The procedure in previous section is utilized to obtain the required specifications for the design example. After 7 iterations the open-loop measured metrics satisfies the application requirements. The whole design process takes 30

Table 1. GPCAD prediction and HSPICE simulation for TSMC 0.18-µm telescopic-cascode op-amp after 7 iterations

Performance measure	Spec.	GPCAD	Hspice
DC gain (db)	> 70	73.2	73.8
Unity gain BW (MHz)	> 100	100	92.7
SR (V/ µs)	> 20	62	62
Power (mW)	As minimum as possible	0.12	0.12

seconds using a 2.8-GHz Pentium IV processor.

Table 1, describes the design problem, and shows the predicted performance of the design obtained by GPCAD and the simulated performance with TSMC model. The first column identifies the performance measure, the second gives the specification, the third, labeled GPCAD shows the performance of the design obtained after seven iterations, the last column shows the value of specification as simulated from our design. In this case study, a 0.8% error for A_V and 8% error for BW have been achieved.

V. Another Case Study

This example uses a two-stage op-amp (Fig. 3) as the design problem. Here we optimize the circuit by proposed method. Circuit constraints are as follows:

$$\begin{aligned} &\max imizeBandwidth \\ &subject\ \text{to}\ A_V \geq 70dB \\ &\quad \text{Swing} \geq 1.4\text{V} \\ &\quad \text{Power} \leq 0.2\text{mW} \\ &\quad C_L = 1pF \\ &\quad 0.18\mu\text{m} \leq \text{L} \leq 0.5\mu\text{m} \\ &\quad 0.5\mu\text{m} \leq \text{W} \leq 75\mu\text{m} \\ &\quad 1.5\text{pF} \leq C_c \leq 10pF \\ &\quad \text{PM} = 90\text{deg} \\ &\quad V_{dd} = 1.8V \end{aligned} \tag{9}$$

Table 2 shows brief descriptions of this optimization after 3 iterations consuming 20 seconds. It can be observed that there is a great agreement between GPCAD optimization and Hspice simulation. As it is clear there is little error between GPCAD and Hspice for voltage gain and there is only 7% error for bandwidth.

VI. Conclusion

We have presented a novel iterative method utilizing geometric programming to optimize the design of CMOS op-amps. Furthermore, by minimizing the error between GP predictions and simulation results we have assured that GP's final design is in fact very close to the theoretical globally-optimized design expected from GP. This method is very fast, efficient and uses simple transistor models. The presented idea is verified by optimizing two different topologies where final discrepancies between GP prediction and SPICE simulation was acceptable. Finally it is notable that this methodology is not restricted to op-amp design and can be applied to the design of different analog circuit blocks.

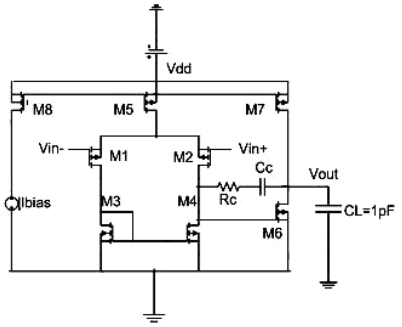

Fig. 3. Two stage op-amp

Table 2. GPCAD prediction and Hspice simulation for two-stage op-amp after 3 iterations

Performance measure	Spec.	GPCAD	Hspice
Max. output (V)	> 1.7	1.7	1.69
Min. output (V)	< 0.1	0.1	0.08
Power (mW)	< 0.2	0.2	0.21
DC gain (db)	> 70	70	70
Unity gain BW (MHz)	Max.	65.7	61.6
Phase Margin (deg)	90	90	88

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