Modified Model for Settling Behavior of Operational Amplifiers in Nanoscale CMOS

Hamidreza Rezaee-Dehsorkh, *Student Member, IEEE*, Nassim Ravanshad, *Student Member, IEEE*, Reza Lotfi, *Member, IEEE*, and Khalil Mafinezhad, *Member, IEEE*

***Abstract*—An accurate time-domain model for the settling behavior of folded-cascode operational amplifiers is presented. Using a velocity–saturation model for MOS transistors makes the proposed model suitable for nanoscale CMOS technologies. Both linear and nonlinear settling regimes and their combination are considered. Transistor-level HSPICE simulation results of a fully differential single-stage folded-cascode amplifier using BSIM4v3 models of a standard 90-nm CMOS process are presented to verify the accuracy of the proposed models.**

***Index Terms*—Integrated circuit modeling, nanoscale CMOS, operational amplifiers (opamps), settling behavior, velocity saturation.**

I. Introduction

HIGH-SPEED switched-capacitor (SC) circuits are very popular in analog and mixed-signal integrated systems. The operational amplifier (opamp) is one of the most important building blocks of SC circuits whose settling behavior basically limits the speed of the SC circuits. Therefore, a more accurate modeling of the settling behavior of opamps is important in the design of high-speed SC circuits.

There have been several attempts to model the settling behavior of the opamp [1]–[8]. None of the approaches, however, has considered the effect of short-channel devices in modern nanometer-range CMOS technologies. As the feature size in modern nanoscale CMOS technologies reduces, the behavior of transistors with very short channels considerably deviates from the conventional models of MOS transistors. One of the main reasons for this deficiency is the velocity saturation effect [9].

This brief presents a mathematical model predicting the step response of an opamp, considering both linear settling and nonlinear settling (slewing) with reasonable accuracy, in nanoscale CMOS technologies. An improved-accuracy nonlinear settling model is obtained by the large-signal analysis of the opamp behavior in slewing phase. Then, the entire settling behavior is modeled by assuming a continuous waveform for the output signal. Although a fully differential single-stage folded-cascode architecture is selected as the case study, a similar approach can be used for other opamp topologies.

The rest of this brief is organized as follows. In Section II, the nonlinear settling (or slewing) of the opamp using large-signal analysis is described. In Section III, the small-signal settling (linear settling) of the opamp is analyzed. Section IV combines the linear and nonlinear settling regions in a complete settling model. Simulation results confirming the accuracy of the model are addressed in Section V, followed by conclusions in Section VI.

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The authors are with the Integrated Systems Laboratory, Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad 9177948944, Iran (e-mail: hr_rezaee@ieee.org; n_ravanshad@ieee.org; rlotfi@ieee.org; kh_mafi@yahoo.com).

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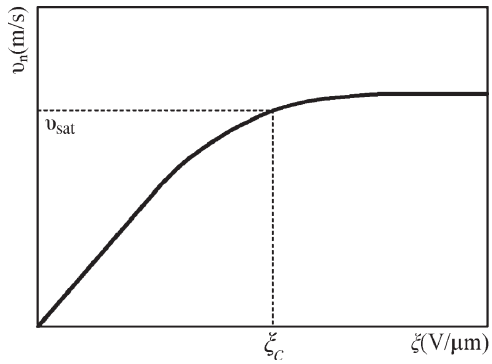

Fig. 1. Carrier velocity saturation.

II. Nonlinear Settling

In this section, after a short discussion on the behavior of short-channel devices, a modified model for the nonlinear settling of opamps in nanometer CMOS is presented.

A. Short-Channel Transistor

The behavior of short-channel MOS transistors considerably deviates from long-channel devices in the triode and saturation regions mainly due to the velocity saturation of charge carriers. For small electrical fields, the velocity of the carriers is proportional to the electric field, and the carrier mobility is constant. At high electrical fields, however, the carriers fail to follow this linear model. In fact, when the electrical field across the channel reaches a critical value ξ_c, the velocity of the carriers saturates due to scattering effects, as illustrated in Fig. 1 [9].

With a simple model that is valid in all the operation regions of a MOS transistor, its behavior is expressed by

$$I_D = \beta\left(V_{\rm ov}V_{\rm min} - \frac{V_{\rm min}^2}{2}\right)(1+\lambda V_{\rm DS}) \quad V_{\rm ov} \geq 0 \qquad (1)$$

where $V_{\rm min} = \min(V_{\rm ov}, V_{\rm DS}, V_{\rm DSAT})$, and $V_{\rm ov} = V_{\rm GS} - V_T$ [9].

In (1), the drain–source voltage $V_{\rm DSAT}$ at which the critical electrical field is reached and velocity saturation occurs is constant and approximated by $V_{\rm DSAT} \simeq L\xi_C = L\upsilon_{\rm sat}/\mu$. By neglecting the channel-length modulation effect, (1) turns into

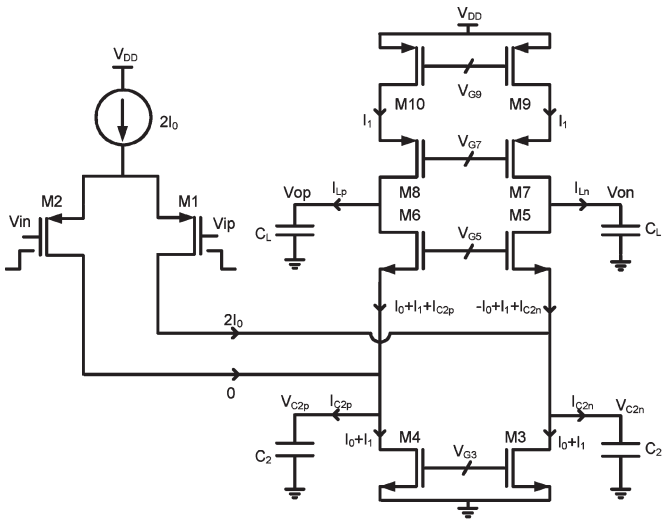

Fig. 2. CMOS fully differential folded-cascode opamp with a large step applied at the input.

(2) for velocity-saturated transistors [9]. The saturation drain voltage $V_{\rm DSAT}$ can be calculated by equating the current at the drain to the current given by

$$I_D = \beta\left(V_{\rm ov}V_{\rm DSAT} - \frac{V_{\rm DSAT}^2}{2}\right). \tag{2}$$

B. Nonlinear Settling in the Opamp With Short-Channel Transistors

It can be shown that small-signal-based analyses for the slewing (nonlinear settling) of an opamp [1]–[5] are not suitable for this phase of settling that naturally has nonlinear behavior [6], [7], and large-signal analysis must be used to model the opamp settling behavior in slewing phase. As previously mentioned, a fully differential single-stage folded-cascode structure with short-channel devices is selected as the case study. Fig. 2 shows a folded-cascode opamp with a large step input applied at time $t = 0$. At this moment, this large input makes $\rm M_1$ become velocity saturated and $\rm M_2$ turn off. It is assumed that under this condition, the drain current of $\rm M_1$ is $2I_0$ (where $2I_0$ is the tail current of the opamp), and the current of $\rm M_2$ is 0. In addition, it is assumed that $\rm C_2$ is the parasitic capacitor at the drain of $\rm M_{3,4}$, and $\rm C_L$ is the overall output capacitance (including the load capacitor and the opamp output parasitic capacitance). Considering the voltage across $\rm C_2$ to be constant at $t = 0$, all the other transistors are on (and velocity saturated). Under this condition, (2) can be used to model the behavior of the transistors.

Substituting $V_{\rm GS5}$ by $V_{\rm G5} - V_{C2n}(t)$, the drain current of $\rm M_5$ is obtained as

$$I_{M5}(t) = \beta_5\, V_{\rm Dsat5}\left(V_{G5} - V_{C2n}(t) - V_{T5} - \frac{V_{\rm Dsat5}}{2}\right). \tag{3}$$

Writing Kirchhoff's current law (KCL) at the drain terminal of $\rm M_3$, one can obtain

$$I_{M5} = I_1 - I_0 + I_{C2n}. \tag{4}$$

Substituting (3) in (4) and considering $I_{C2n} = C_{2n}(dV_{C2n}(t)/dt)$, we have

$$I_1 - I_0 + C_{2n}\frac{dV_{C2n}(t)}{dt} = \beta_5\, V_{\rm Dsat5}\left(V_{G5} - V_{C2n}(t) - V_{T5} - \frac{V_{\rm Dsat5}}{2}\right). \tag{5}$$

Solving the differential equation of (5) with the initial condition expressed as

$$V_{C2n}(0) = V_{G5} - \frac{I_1}{\beta_5 V_{\rm Dsat5}} - V_{T5} - \frac{V_{\rm Dsat5}}{2} \tag{6}$$

$(I_{M5}(0) = I_1)$ results in

$$V_{C2n}(t) = \frac{I_0 - I_1}{\beta_5 V_{\rm Dsat5}} + V_{G5} - V_{T5} - \frac{V_{\rm Dsat5}}{2} - \frac{I_0}{\beta_5 V_{\rm Dsat5}} e^{-\frac{\beta_5 V_{\rm Dsat5}}{C_2}t}. \tag{7}$$

Writing KCL at the negative output node $(V_{\rm on})$, one gets

$$I_{\rm Ln} = I_1 - I_1 + I_0 + I_{C2n} = I_0 + I_{C2n} \tag{8}$$

$$C_L\frac{dV_{\rm on}(t)}{dt} = I_0 - C_2\frac{dV_{C2n}(t)}{dt}. \tag{9}$$

By integrating (9) and substituting (7) in it, one can obtain

$$V_{\rm on}(t) = \frac{I_0 t}{C_L} - \frac{C_2 I_0}{C_L\beta_5 V_{\rm Dsat5}}\left[1 - e^{-\frac{\beta_5 V_{\rm Dsat5}}{C_2}t}\right] + V_o(0) \tag{10}$$

where $V_o(0)$ is the initial voltage of the opamp outputs just before applying the input step (the initial voltages of both opamp outputs are considered the same and equal to the common-mode voltage).

Computing the positive output voltage in the slewing phase can similarly be done as explained here. Writing KCL at the drain terminal of $\rm M_4$, one gets

$$I_{M6} = I_1 + I_0 + I_{C2p} \tag{11}$$

$$\beta_5 V_{\rm Dsat5}\left(V_{G5} - V_{C2p}(t) - V_{T5} - \frac{V_{\rm Dsat5}}{2}\right) = I_1 + I_0 + C_{2p}\frac{dV_{C2p}(t)}{dt}. \tag{12}$$

Solving (12) with the initial condition results in

$$V_{C2p}(t) = -\frac{I_0 + I_1}{\beta_5 V_{\rm Dsat5}} + V_{G5} - V_{T5} - \frac{V_{\rm Dsat5}}{2} + \frac{I_0}{\beta_5 V_{\rm Dsat5}} e^{-\frac{\beta_5 V_{\rm Dsat5}}{C_2}t}. \tag{13}$$

Writing KCL at the positive output $(V_{\rm op})$ results in

$$I_{\rm Lp} = I_1 - I_1 - I_0 - I_{C2p} = -I_0 - I_{C2p} \tag{14}$$

$$C_L\frac{dV_{\rm op}(t)}{dt} = -I_0 - C_2\frac{dV_{C2p}(t)}{dt}. \tag{15}$$

Integrating (15) and substituting (13) in it leads to

$$V_{\rm op}(t) = -\frac{I_0 t}{C_L} + \frac{C_2 I_0}{C_L\beta_5 V_{\rm Dsat5}}\left[1 - e^{-\frac{\beta_5 V_{\rm Dsat5}}{C_2}t}\right] + V_o(0). \tag{16}$$

TABLE I
CIRCUIT PARAMETERS (AT TYPICAL CORNER, 27 °C)

Symbol	Value	Parameter Description
V_{DD}	1 V	supply voltage
$2I_0$	0.8 mA	tail current
I_1	0.5 mA	cascode current
β_1	80 mA/V^2	transconductance parameter of M_1, M_2
β_5	65 mA/V^2	transconductance parameter of M_5, M_6
V_{Dsat1}	98 mV	velocity saturation voltage of M_1, M_2
V_{Dsat5}	120 mV	velocity saturation voltage of M_5, M_6
C_2	104 fF	parasitic capacitance at the drain of M_3, M_4
C_L	131 fF	overall output capacitance
β	1	feedback factor
V_{in}	200 mV	input step voltage
A_0	30.17 dB	openloop gain of amplifier
δ	0.58	damping factor
ω_n	54 G rad/s	natural frequency

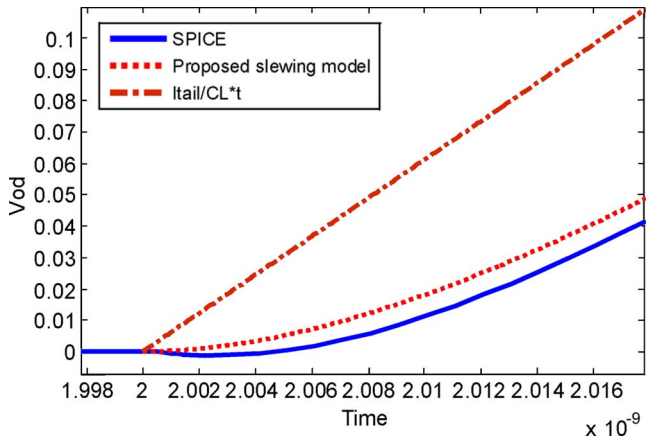

Fig. 3. Comparison of simulation results with the proposed model and conventional slewing model of $I_{\rm tail}.t/{\rm C_L}$ for a large input step applied at $t = 2$ ns.

Thus, the opamp differential output voltage in the slewing phase can be written as

$$V_{o,\rm sr}(t) = V_{\rm op}(t) - V_{\rm on}(t) = -\frac{2I_0 t}{C_L} + \frac{2C_2 I_0}{C_L \beta_5 V_{\rm Dsat5}}\left[1 - e^{-\frac{\beta_5 V_{\rm Dsat5}}{C_2}t}\right]. \quad (17)$$

To justify the accuracy of the proposed model for the slewing phase of a fully differential single-stage folded-cascode opamp, circuit-level simulations were performed with HSPICE using BSIM4v3 models of a 90-nm standard CMOS process. Some of the amplifier parameters and the simulation conditions are shown in Table I. In the opamp, the length of all the devices has been chosen as the minimum value of 90 nm. Fig. 3 compares the simulation results with the proposed slewing model [see (17)] and the conventional slewing model of $I_{\rm tail}.t/{\rm C_L}$. It can be seen that the conventional slewing model is not a good estimate of the HSPICE simulation results. On the other hand, the proposed model has a very good agreement with the HSPICE simulation results. Note that in the real circuit, the assumed initial conditions are changed due to signal feedthrough from the input step. Neglecting the channel-length modulation is the other assumption that reduces the accuracy of the proposed model.

III. LINEAR OR SMALL-SIGNAL SETTLING

Pole-zero analysis of a folded-cascode amplifier shows that this amplifier can be modeled by just two poles [10], [11]. An open-loop transfer function of a two-pole system can be presented as

$$H_{\rm OL}(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (18)$$

where ω_{p1} and ω_{p2} are the open-loop poles, and A_0 is the dc gain of the amplifier. Considering a constant feedback factor (β), the closed-loop transfer function is

$$H_{\rm cl}(s) = \frac{A_0}{1 + \beta A_0}\frac{\omega_n^2}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (19)$$

where

$$\omega_n = \sqrt{(1 + A_0\beta)\omega_{p1}\omega_{p2}} \quad (20)$$

$$\delta = \frac{\omega_{p1} + \omega_{p2}}{2\omega_n}. \quad (21)$$

When $0 < \delta < 1$, then the two-pole system has an underdamped step response that is expressed by

$$V_{o,\rm step}(t) = \frac{V_{\rm step}A_0}{1 + \beta A_0}\left[1 - Ae^{-\delta\omega_n t}\sin(\omega t + \phi)\right] \quad (22)$$

where $V_{\rm step}$ is the amplitude of the input step, and

$$A = \frac{1}{\sqrt{1 - \delta^2}} \quad (23)$$

$$\omega = \omega_n\sqrt{1 - \delta^2} \quad (24)$$

$$\phi = \arccos(\delta). \quad (25)$$

Since in most cases, for the fastest step response the opamp should exhibit an underdamped behavior, only this case (i.e., the case for $0 < \delta < 1$) is considered here.

IV. COMPLETE SETTLING BEHAVIOR

The linear and nonlinear settling curves must be connected to each other in a manner that their combination is a continuous waveform with a continuous derivative [3], [8]. In other words, the following two conditions must be satisfied:

$$V_{o,\rm sr}(t_{\rm sr}) = V_{o,\rm lin}(t_{\rm sr}) \quad (26)$$

$$\left.\frac{dV_{o,\rm sr}(t)}{dt}\right|_{t=t_{\rm sr}} = \left.\frac{dV_{o,\rm lin}(t_{\rm sr})}{dt}\right|_{t=t_{\rm sr}} \quad (27)$$

where $V_{o,\rm sr}(t)$ is the differential output voltage obtained from slewing, $V_{o,\rm lin}(t)$ is the differential output voltage obtained from small-signal settling, and $t_{\rm sr}$ is the time at which the slewing phase terminates. Fig. 4 graphically shows the combination of the linear and nonlinear settling curves for an underdamped two-pole amplifier. $V_{\rm sr0}$ is the differential output voltage at the

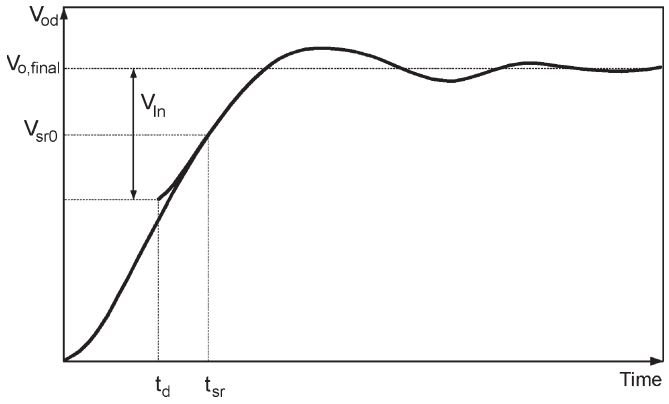

Fig. 4. Combination of the linear and nonlinear settling curves for an underdamped two-pole folded-cascode amplifier.

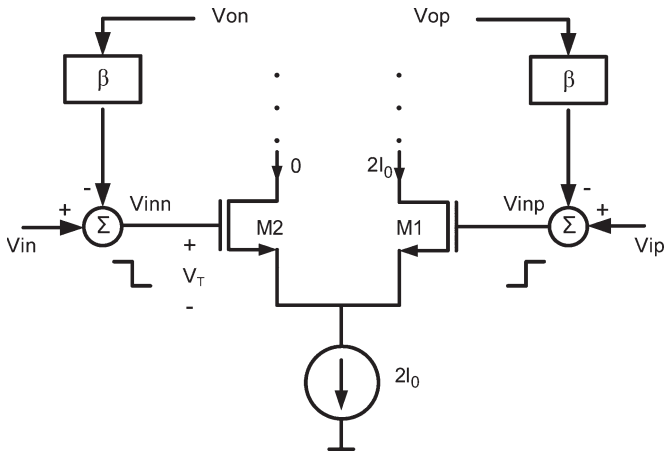

Fig. 5. Fully differential amplifier at the end of the slewing phase and the beginning of the linear settling regime.

end of the slewing phase, $V_{o,\mathrm{final}}$ is the final output differential voltage of the amplifier, V_{ln} is the amplitude of the linear settling voltage, and t_d is the initial delay time of the linear settling phase.

At the end of the slewing, the opamp behaves linearly, and the output differential voltage can be obtained from

$$V_{o,\mathrm{lin}}(t) = V_{o,\mathrm{final}} - V_{\mathrm{ln}} + V_{\mathrm{ln}}\left(1 - Ae^{-\delta\omega_n(t-t_d)}\sin\left(\omega(t-t_d)+\Phi\right)\right), \quad t > t_d. \tag{28}$$

Applying (17) and (28) to the continuity conditions of (26) and (27) leads to

$$V_{o,\mathrm{final}} - V_{\mathrm{ln}} + V_{\mathrm{ln}}\left(1 - Ae^{-\delta\omega_n(t_{\mathrm{sr}}-t_d)}\sin\left(\omega(t_{\mathrm{sr}}-t_d)+\Phi\right)\right) = \frac{2I_0}{C_L}t_{\mathrm{sr}} - \frac{2C_2I_0}{C_L\beta_5 V_{\mathrm{Dsat5}}}\left(1 - e^{-\frac{\beta_5 V_{\mathrm{Dsat5}}}{C_2}t_{\mathrm{sr}}}\right) \tag{29}$$

$$\frac{2I_0}{C_L} - \frac{2I_0}{C_L}e^{-\frac{\beta_5 V_{Dsat5}}{C_2}t_{sr}} = V_{\mathrm{ln}}A\omega_n e^{-\delta\omega_n(t_{\mathrm{sr}}-t_d)}\sin\left(\omega(t_{\mathrm{sr}}-t_d)+\Phi-\tan^{-1}\frac{\omega}{\delta\omega_n}\right). \tag{30}$$

In (29) and (30), V_{ln}, t_d, and t_{sr} are unknown variables. Therefore, another equation is needed to find these unknown variables. Fig. 5 shows the input signals and the bias condition of input pair transistors for a fully differential amplifier at the end of the slewing phase. When M_2 is about to turn on, V_{GS2} is approximately equal to V_T. Assuming M_1 is still on and velocity saturated, we have

$$V_{\mathrm{sr0}} = \left(V_{\mathrm{id}} - \left(V_{\mathrm{inp}} - V_{\mathrm{inn}}\right)\right)/\beta = \left(V_{\mathrm{id}} - \frac{2I_0}{\beta_1 V_{\mathrm{Dsat1}}} - \frac{V_{\mathrm{Dsat1}}}{2}\right)\Big/\beta \tag{31}$$

where V_{id} is the input differential voltage, and β is the feedback factor.

Applying this result to (17), t_{sr} can be computed as

$$t_{\mathrm{sr}} = \frac{C_2}{\beta_5\, V_{\mathrm{Dsat5}}}\mathrm{lambertw}\left(-e^{-\frac{V_{\mathrm{sr0}}C_L\beta_5 V_{\mathrm{Dsat5}}+2C_2I_0}{2C_2I_0}}\right) + \frac{C_2}{\beta_5\, V_{\mathrm{Dsat5}}} + \frac{V_{\mathrm{sr0}}C_L}{2I_0} \tag{32}$$

where lambertw is Lambert's W function ($w = \mathrm{lambertw}(x)$ means $x = w.e^w$).

Therefore, the two unknown variables left in (29) and (30), i.e., V_{ln} and t_d, can be solved using (29), (30), and (32) as

$$t_d = t_{\mathrm{sr}} - \frac{\arctan\left(\frac{V_{\mathrm{srp}}\sin(\phi)}{\omega_n V_{o,\mathrm{final}} - \omega_n V_{\mathrm{sr0}} - V_{\mathrm{srp}}\cos(\phi)}\right)}{\omega} \tag{33}$$

$$V_{\mathrm{ln}} = \frac{V_{o,\mathrm{final}} - V_{\mathrm{sr0}}}{Ae^{-\delta\omega_n(t_{\mathrm{sr}}-t_d)}\sin\left(\omega(t_{\mathrm{sr}}-t_d)+\Phi\right)} \tag{34}$$

where V_{srp} is the derivative of the slewing equation [i.e., (17)] at $t = t_{\mathrm{sr}}$ and equal to

$$V_{\mathrm{srp}} = \frac{2I_0}{C_L} - \frac{2I_0}{C_L}e^{-\frac{\beta_5\ V_{\mathrm{Dsat5}}}{C_2}t_{\mathrm{sr}}}. \tag{35}$$

The settling time of an amplifier with an input step signal is the time at which the amplifier output has entered the vicinity of the final value and remained within a specified error. In other words

$$|V_{o,\mathrm{final}} - V_{o,\mathrm{lin}}(t)| < \varepsilon \quad \text{if} \quad t > t_{\mathrm{set}} \tag{36}$$

or

$$\left|V_{\mathrm{ln}}Ae^{-\delta\omega_n(t-t_d)}\sin\left(\omega(t-t_d)+\Phi\right)\right| < \varepsilon \quad \text{if} \quad t > t_{\mathrm{set}} \tag{37}$$

where ε is the settling error.

Since (37) cannot analytically be solved, an approximation that overestimates the accurate value is used to calculate the settling time as

$$\left|V_{\mathrm{ln}}Ae^{-\delta\omega_n(t-t_d)}\sin(\omega(t-t_d)+\Phi)\right| < \left|V_{\mathrm{ln}}Ae^{-\delta\omega_n(t-t_d)}\right| < \varepsilon \tag{38}$$

and therefore

$$t_{\mathrm{set}} = \frac{\ln\left(\frac{V_{\mathrm{ln}}A}{\varepsilon}\right)}{\delta\omega_n} + t_d. \tag{39}$$

V. Simulation Results

Fig. 6 compares the complete settling behavior of the amplifier as estimated by the proposed model with the results of HSPICE simulation. All the simulations were performed with HSPICE using BSIM4v3 level-54 models of a 90-nm standard

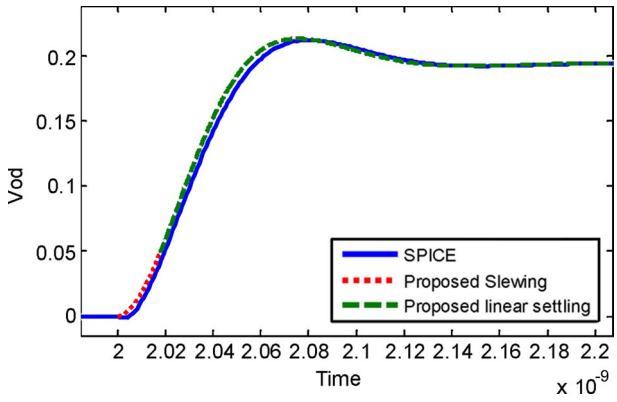

Fig. 6. Estimated and SPICE simulation of the step response of a nanoscale CMOS fully differential folded-cascode amplifier applied at $t = 2$ ns.

TABLE II
COMPARISON RESULTS FOR SETTLING ERROR $\varepsilon = 0.0005$

Corner	SPICE simulation settling time	Numerical computation of settling time error w.r.t. simulation	Approximated settling time error w.r.t. simulation
PTNT, 27 °C	185 ps	-1.64 %	6.67 %
PSNS, 85 °C	229 ps	-2.4 %	10.13 %
PSNF, 85 °C	221 ps	-2.64 %	6.12 %
PFNS, 85 °C	214 ps	-2.43 %	8.68 %
PFNF, 85 °C	209 ps	-3.12 %	3.41 %
PSNS, -40 °C	158 ps	-0.47 %	5.20 %
PSNF, -40 °C	153 ps	-0.83 %	2.1 %
PFNS, -40 °C	148 ps	-0.54 %	4.05 %
PFNF, -40 °C	145 ps	-1.1 %	1 %

CMOS process. Some of the amplifier parameters and the simulation conditions are shown in Table I. It can be seen that the proposed models for the settling behavior of the folded-cascode amplifier predict the HSPICE simulation results very well. Tables II and III present the comparison results of HSPICE simulations, numerical computations of the proposed model [i.e., (37)], and the approximated settling time [i.e., (39)] of a PMOS-input folded-cascode amplifier in process/temperature corners for two cases of settling error. Table II shows a high-precision settling case $(\varepsilon = 0.0005)$, and Table III shows a low-precision settling case $(\varepsilon = 0.01)$. The comparison results of Tables II and III show that the error between the proposed approximated settling time and the HSPICE simulation results has always been less than about 10%. In some cases, there may be a difference between overshoot of the proposed settling model and the simulation result. That is because the overshoot of a two-pole system is an exponential function of δ (i.e., $\exp(-\delta\pi/\mathrm{sqrt}(1-\delta^2))$), and a little error in the estimation of δ leads to bigger deviations in the value of the overshoot.

VI. CONCLUSION

The settling behavior of a fully differential single-stage folded-cascode amplifier has been presented by taking into account both linear and nonlinear settling phases with very-short-channel devices. To model the opamp nonlinear settling in the slewing phase, large-signal analysis has been used, and for the linear settling behavior, a two-pole model has been employed. Using the velocity–saturation model for MOS transistors, the proposed model is suitable for nanoscale CMOS technologies. The proposed model was verified by means of transistor-level simulations. All of the simulation results were in very good agreement with the predicted results. The proposed model can readily be used in computer-aided design tools as well.

TABLE III
COMPARISON RESULTS FOR SETTLING ERROR $\varepsilon = 0.01$

Corner	SPICE simulation settling time	Numerical computation of settling time error w.r.t. simulation	Approximated settling time error w.r.t. simulation
PTNT, 27 °C	103.1 ps	-3.42 %	-0.49 %
PSNS, 85 °C	127.2 ps	-3.61 %	2.18 %
PSNF, 85 °C	121.5 ps	-4.06 %	-0.56 %
PFNS, 85 °C	118.5 ps	-3.88 %	0.99 %
PFNF, 85 °C	114.2 ps	-4.31 %	-2.08 %
PSNS, -40 °C	88 ps	-2.43 %	-1.1 %
PSNF, -40 °C	83.9 ps	-2.35 %	-2.06 %
PFNS, -40 °C	80.9 ps	-0.99 %	-0.1 %
PFNF, -40 °C	77.8 ps	-0.89 %	-0.84 %

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