Ultra-low voltage common-mode voltage detector circuit

M. Daliri and M. Maymandi-Nejad

A new common-mode voltage detector circuit to be used in the common-mode feedback loop of ultra-low voltage fully differential amplifiers is presented. The proposed circuit behaves linearly for most of the signal range and is able to operate with supply voltages as low as 0.4 V. The design issues and simulation results of the circuit in 0.18 μm CMOS technology are presented.

Introduction: Owing to reliability issues, the supply voltage of modern CMOS circuits has reduced. Moreover, in some applications, such as bio-implantable ICs, it is desirable to use very low supply voltages. Using low supply voltages causes the dynamic range (DR) and the signal-to-noise ratio (SNR) of analogue circuits to decrease. Using fully differential architectures can help to improve DR and SNR. However, fully differential circuits require a common-mode (CM) feedback [1]. Ideally, a common-mode feedback (CMFB) circuit should behave linearly and should only respond to CM voltages. Lacking these features causes the conversion of differential-mode voltage (DM) to CM voltage and vice versa and increases the THD of the circuit [1]. Designing a CMFB circuit that is able to operate under a very low supply voltage is a nontrivial task, mainly because of the difficulty of detecting the CM voltage. In [2] a pacemaker front end is designed with a supply voltage of 1 V. In this design, to overcome the problem of designing the CMFB, the authors have decided to use two single-ended amplifiers instead of a fully differential one. Clearly, this approach increases the power consumption of the circuit and takes up more area. In this Letter we present a CM voltage detector which is able to operate with ultra-low voltage supplies.

The simplest way to detect the CM voltage is to use two equal resistors connected between the two outputs of a fully differential amplifier. In such a case the value of the resistors should be very high to keep the differential gain of the amplifier large. Implementing such large resistors on silicon takes a lot of space and is not very desirable. Hence, designers typically try to use NMOS or PMOS transistors to detect the CM voltage. At very low supply voltages NMOS or PMOS transistors turn off within a considerable range of voltages and are not able to provide the rail-to-rail operation. Fig. 1 shows two possible circuits to detect the CM voltage. The response of these two circuits to a CM voltage ranging from 0 to 0.8 V is also shown in Fig. 1. Clearly, these circuits fail to detect the CM voltage when the voltage is very close to *GND* or V_{dd}.
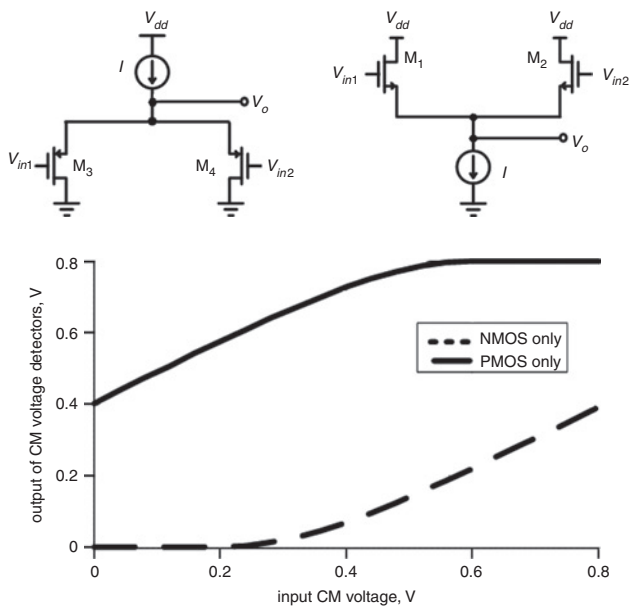

Fig. 1 *Two possible circuits which can detect CM voltage and their response to CM voltage*

Proposed CM detector circuit: Fig. 2 shows the proposed circuit for detecting the CM voltage. In the proposed circuit, a combination of PMOS and NMOS transistors are used in a source follower configuration. In the case of very low supply voltages, transistors of this circuit operate in the sub-threshold as well as strong inversion regions. Hence, to analyse this circuit, one should use the unified equation for the drain current provided in [3] which is valid for all operating regions. The output voltage of the circuit can be found using the KCL at the output node (V_o). Applying this technique and using the equation for the drain currents provided in [3] the response of the proposed circuit to a CM voltage can be calculated. The result obtained from the calculation is compared with that of simulation in the 0.18 μm CMOS technology and is illustrated in Fig. 3. As can be seen, the two curves match quite well and in both cases the output voltage follows the input CM voltage with a gain of approximately 1.
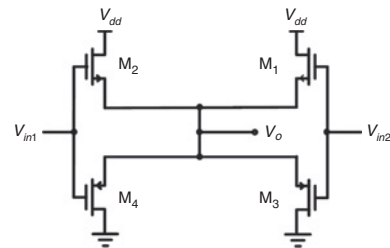

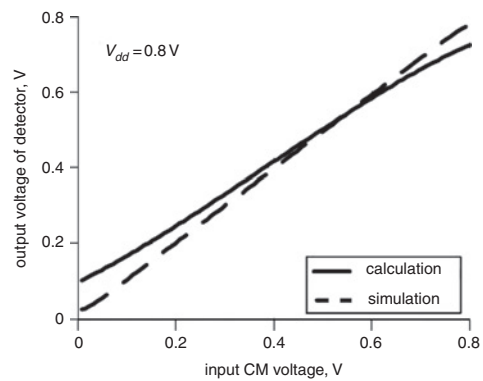**Fig. 2** *Proposed detector circuit*

Fig. 3 *Response of detector circuit to CM voltage*

Another important parameter for a CM detector is its gain to DM voltages ($A_d = V_o/V_{id}$). Ideally, a CM detector should only respond to the CM voltage and its gain to a DM voltage should be zero. This is not the case in practice and the designer should try to reduce the DM gain of the CM detector as much as possible. In the proposed circuit this can be achieved by selecting proper sizes for the PMOS and NMOS transistors. The differential gain (A_d) of the circuit with respect to the ratio of $(W/L)_p$ (W/L ratio of the PMOS transistors) to $(W/L)_n$ (W/L ratio of the NMOS transistors) is shown in Fig. 4. Clearly, there is an optimum ratio in which the detector has the minimum differential gain.
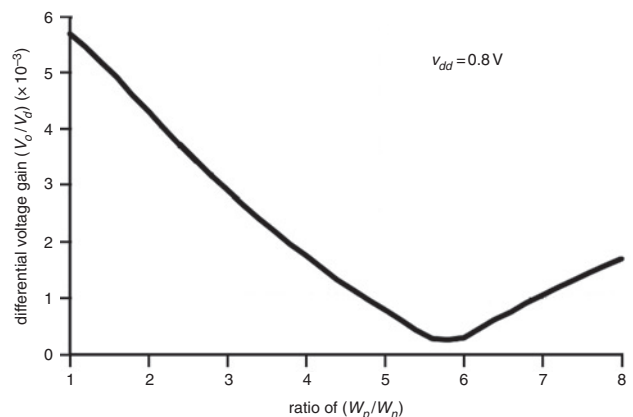

Fig. 4 *Impact of ratio of PMOS and NMOS transistor sizes on differential gain (V_o/V_d) of detector*

ELECTRONICS LETTERS   19th June 2008   Vol. 44   No. 13

To find the supply voltage range that the CM detector circuit can operate with the circuit is simulated with supply voltages ranging from 0.1 to 2 V and the response of the circuit to CM voltage is obtained. The output is then approximated by a second-order equation; i.e. $a_2x^2 + a_1x + a_0$. The coefficients of the second-order polynomial are shown in Fig. 5 for different supply voltages. Ideally, a_2 should be zero and a_1 should be 1. According to Fig. 5, the absolute value of the coefficient a_2 starts to increase sharply for supply voltages below 0.4 V while the coefficient a_1 is close to 1 for supply voltages above 0.1 V. This means that the proposed circuit is able to operate with very low supply voltage (down to 0.1). However, its response to common-mode voltage becomes nonlinear for supply voltages below approximately 0.4 V. The offset voltage at the output of the CM detector circuit (a_0) changes by approximately 12 mV when the supply voltage varies from 0.2 to 2 V. This amount of offset variation is negligible compared to the CM voltage variation of about 1.8 V.
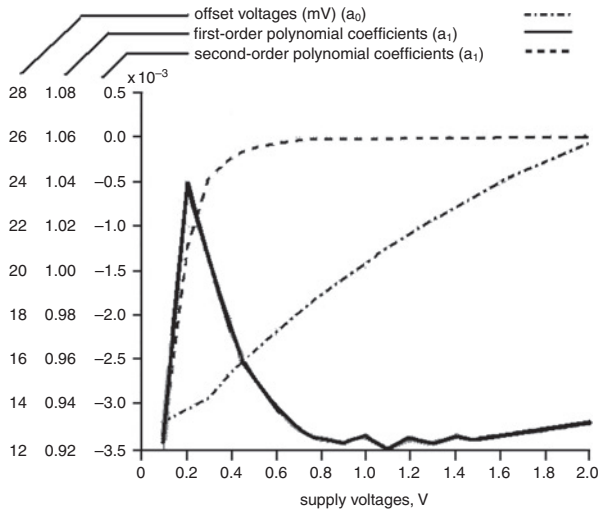

Fig. 5 *Polynomial coefficients of output voltage against supply voltage*

Conclusion: A CM voltage detector circuit to be used in the feedback loop of a common-mode feedback is presented. The proposed circuit is able to operate with a very low supply voltage (as low as 0.1 V if some degree of nonlinearity can be tolerated). The design issues and simulation results of the proposed circuit are presented.

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