V. Conclusion

We have proposed a novel approach, in which data is written row-by-row into a matrix and read diagonal-wise, for designing collision-free parallel interleavers. To improve the performance of the designed interleaver, a random mapping and swapping scheme has been used to augment the spread distance of the interleaver. The proposed collision-free parallel interleavers are competitive with the collision-prone S-random interleaver and slightly outperform the interleaver specified by the 3GPP standard. To minimize the decoding delay in a highly-parallel decoder, two warm-up-free parallel architectures, the parallel SW architecture, and the PW architecture, have been proposed for long and short turbo codes, respectively. Compared to the warm-up parallel SW architecture, the proposed warm-up-free parallel SW architecture increases the speed by 6%–34% at a cost of a hardware increase of 1% for an 8-parallel decoder, while the proposed warm-up-free PW architecture doubles the speed at a cost of hardware increase of 12%.

References

[1] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo-codes," in *Proc. Int. Conf. Commun. (ICC)*, 1993, pp. 1064–1070.

[2] A. Giulietti, L. van der Perre, and A. Strum, "Parallel turbo coding interleavers: Avoiding collisions in accesses to storage elements," *Electron. Lett.*, vol. 38, no. 5, pp. 232–234, Feb. 2002.

[3] L. Bahl, J. Cocke, F. Jelinek, and J. Raviv, "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inf. Theory*, vol. 20, no. IT-2, pp. 284–287, Mar. 1974.

[4] Z. Wang, Z. Chi, and K. K. Parhi, "Area-efficient high-speed decoding schemes for turbo decoders," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 6, pp. 902–912, Dec. 2002.

[5] *3GPP2 (3rd Generation Partnership Project 2) Specifications*, [Online]. Available: http://3gpp2.com/

[6] S. Dolinar and D. Divsalar, "Weight distributions for Turbo codes using random and nonrandom permutations," *Telecommun. Data Acquisition (TDA) Progress Rep.*, vol. 42, no. 122, pp. 56–65, Aug. 15, 1995.

[7] Z. Wang, Y. Tang, and Y. Wang, "Low hardware complexity parallel turbo decoder architecture," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2003, pp. 53–56.

[8] S. Crozier and P. Guinand, "High-performance low-memory interleaver banks for turbo-codes," in *Proc. IEEE 54th Veh. Technol. Conf.*, 2001, pp. 2394–2398.

[9] J. Kwak and K. Lee, "Design of dividable interleaver for parallel decoding in turbo codes," *Electron. Lett.*, vol. 38, no. 22, pp. 1362–1364, Oct. 2002.

[10] A. J. Viterbi, "An intuitive justification and a simplified implementation of the MAP decoder for convolutional codes," *IEEE J. Sel. Areas Commun.*, vol. 16, no. 2, pp. 260–264, Feb. 1998.

[11] F. Raouafi, A. Dingninou, and C. Berrou, "Saving memory in turbo-decoders using the max-log-MAP algorithm," *IEE Colloq. Turbo Codes Dig. Broadcasting—Could It Double Capacity?*, pp. 14/1–14/4, 1999, (Ref. No. 1999/165).

[12] Y. Wu, B. D. Woerner, and T. K. Blankenship, "Data width requirements in SISO decoding with modulo normalization," *IEEE Trans. Commun.*, vol. 49, no. 11, pp. 1861–1868, Nov. 2001.

[13] H. Dawid, G. Gehnen, and H. Meyr, "MAP channel decoding: Algorithm and VLSI architecture," in *Proc. Workshop VLSI Signal Process., VI*, 1993, pp. 141–149.

[14] A. Worm, H. Lamm, and N. Wehn, "A high-speed MAP architecture with optimized memory size and power consumption," in *Proc. IEEE Workshop Signal Process. Syst.*, 2000, pp. 265–274.

DTMOS Technique for Low-Voltage Analog Circuits

Mohammad Maymandi-Nejad and Manoj Sachdev

***Abstract*—In this paper, the application of dynamic threshold MOS (DTMOS) technique for low-voltage analog circuits is explored. The body terminal of PMOS transistors in bulk CMOS technology can be used as the forth terminal to enhance the performance of low-voltage analog circuits. To show the effectiveness of this technique, we have designed a continuous time common mode feedback (CMFB) circuit for a sub 1-V opamp and a new sub 1-V, 1-bit quantizer. A 0.8-V opamp with embedded CMFB and a 0.8-V, 1-bit quantizer for low-voltage $\Delta\Sigma$ modulators are implemented in 0.18-μm CMOS technology. The simulation results as well as the measurement data of these blocks are presented in this paper.**

***Index Terms*—1-bit quantizer, CMOS analog circuits, comparator, $\Delta\Sigma$ modulator, dynamic threshold MOS (DTMOS), operational amplifier.**

I. Introduction

THE continuous trend toward smaller feature size for transistors in the CMOS technology, demands for lower supply voltages [1]. This is due to the very thin gate oxide in advanced technologies. In addition, in many applications such as implantable biomedical devices, hearing aids [2], etc., the circuit should be operated with a miniature battery. Often, commercial miniature batteries provide a voltage in the range of 0.9 to 1.5 V with limited energy capacity [3]. In such applications, the volume and the weight of the battery is one of the primary concerns. These concerns force analog circuit designers to look for low-voltage, low-power circuit architectures and techniques. Reducing the supply voltage in analog circuits is not trivial compared to digital circuits. In particular, supply voltage reduction in analog circuits reduces its dynamic range which in turn, degrades the signal–to–noise ratio (SNR) of signals. Moreover, as CMOS technology scales down the output resistance of MOS transistors is reduced. As a consequence, the maximum achievable gain from a MOS amplifier is reduced. Similarly, reduced output resistance makes the design of supply independent biasing network a challenging task. As a result, analog designers must continuously find low-voltage circuit techniques in order to be consistent with technology trends [4], [5]. In this context, the dynamic threshold MOS (DTMOS) technique, which was originally used in digital circuits, has the potential to enhance the performance of a low-voltage analog circuit [6].

In this paper, we show how the DTMOS technique can be helpful in the design of low-voltage analog circuit blocks. We designed a low-voltage, fully differential amplifier with a common mode feedback (CMFB) circuit and a low-voltage comparator, incorporating the DTMOS technique in bulk CMOS technology [7], [8]. In the case of CMFB, the DTMOS technique helps in reducing the circuit complexity while not consuming extra power. Similarly, in the case of the comparator, the DTMOS technique makes it possible to get a rail-to-rail input range.

This paper is organized as follows. In Section II, an overview of the DTMOS technique is given. The common mode feedback circuit and

Manuscript received September 22, 2005.

M. Maymandi-Nejad is with the Electrical Engineering Department, Ferdowsi University of Mashhad, Mashhad 9177948944, Iran (e-mail: maymandi@um.ac.ir).

M. Sachdev is with the Electrical and Computer Engineering Department, University of Waterloo, Waterloo N2L 3G1, ON, Canada (e-mail: msachdev@ece.uwaterloo.ca).

Digital Object Identifier 10.1109/TVLSI.2006.884174

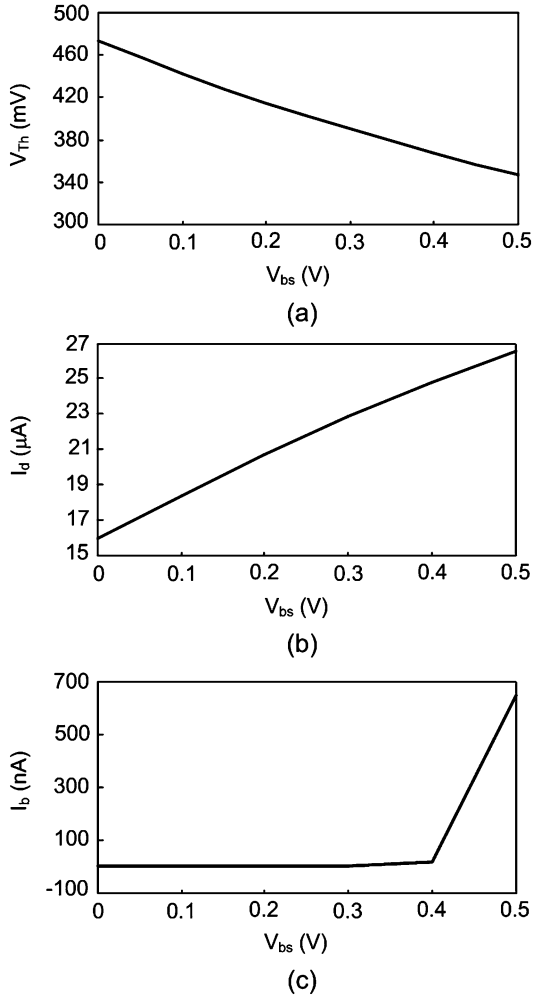

Fig. 1. Effect of forward body bias on (a) threshold voltage; (b) drain current; and (c) body current of a minimum size PMOS transistor.

the quantizer circuit are discussed in Sections III and IV, respectively. Finally, conclusions are drawn in Section V.

II. DTMOS Technique

The DTMOS technique was first introduced in 1994 [9], [10]. Since then, many novel circuit applications of this technique have been proposed. The DTMOS technique is mostly used in digital applications in which the gate and body of the MOSFET are tied together. This is to reduce the leakage current during off state and reducing the threshold voltage during on state to increase the overdrive voltage. It is also possible to use the DTMOS technique in bulk CMOS technology for analog circuit applications. However, in analog applications the body terminal of the MOSFET transistor is normally used as a forth terminal.

In the standard bulk CMOS technology, it is possible to use the body of PMOS transistors as a fourth terminal to the MOSFET. Fig. 1 depicts the impact of the forward body bias ($V_{\rm bs}$) on the threshold voltage V_T, drain current I_d, and the body current (the current going into the body terminal) I_b of a PMOS transistor. As can be seen in Fig. 1(a), by changing the absolute value of $V_{\rm bs}$ from 0 to 0.5 V, the threshold voltage reduces by more than 25%. Increasing $|V_{\rm bs}|$ also causes drain current to increase [Fig. 1(b)]. However, note that as the body-source junction becomes more forward biased, more current goes into the body terminal of the MOSFET [Fig. 1(c)], which is not desirable. Nevertheless, as can be seen in Fig. 1(c), a forward bias of up to about 0.4 V is acceptable. Even for a forward bias of 0.5 V, the body current is still much smaller than the drain current and can be ignored in many applications.

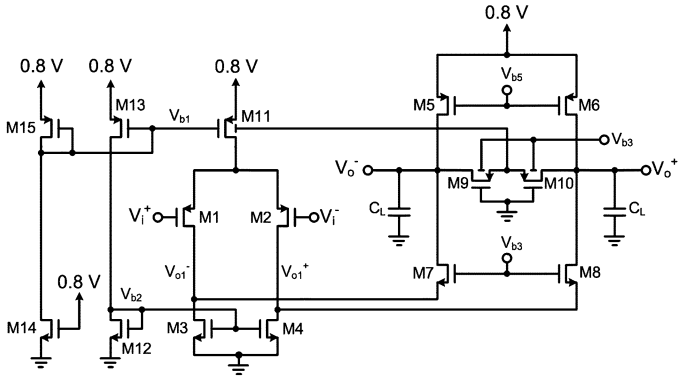

Fig. 2. Schematic of the folded cascode amplifier with embedded CMFB.

Several issues should be considered while using the bulk as the forth terminal of the transistor. First of all, the bulk terminal has a lower transconductance $g_{\rm mb}$ compared to gate transconductance g_m. Second, the parasitic capacitance of the bulk terminal can be larger than that of the gate. This is due to the relatively large area of the n-well in which the PMOS transistor is formed. Therefore, body terminal should not be part of a high frequency path. Finally, the forward bias voltage of the body terminal should not exceed a fraction of a volt.

Despite the limitations of using the bulk terminal of a PMOS transistor, the DTMOS technique can have several advantages in low-voltage analog circuits. First, in low-voltage applications there is not much voltage headroom for signal swing and reducing the threshold voltage can be helpful. Second, having a fourth terminal can be advantageous since it can result in a simpler circuit with a fewer number of transistors. Third, the voltage range at the body terminal of a PMOS transistor normally covers the range of voltages which is not covered by the gate of the transistor. Therefore, using the bulk terminal makes it possible to extend the input voltage range of a circuit. These issues will be addressed in more detail in subsequent sections of this paper.

III. Continuous Time Common Mode Feedback (CMFB) Circuit Using DTMOS Technique

In fully differential analog architectures, the CMFB plays a critical role in bias stabilization [11]. In an analog amplifier transistors are typically biased in the saturation region in order to provide adequate gain. A CMFB is necessary to guarantee that all transistors are biased on the desired operating point. A CMFB circuit also improves the common mode rejection ratio (CMRR) of the amplifier. In this section, we discuss a continuous time CMFB circuit using the DTMOS technique.

A. Folded Cascode Amplifier With a CMFB Circuit Using DTMOS

Fig. 2 illustrates the schematic of a sub 1-V folded cascade amplifier with the proposed CMFB circuit. The amplifier is designed to operate with a single power supply voltage of 0.8 V. The input transistors (M_1, M_2) and the active load transistors (M_3, M_4) are biased in the saturation region. Therefore, it is necessary to adjust the current of the transistor M_{11} to twice that of the current passing through M_3 or M_4. Any variation in biasing voltages V_{b1} or V_{b2} causes a large voltage change at the output (V_o^+ and V_o^-). Bias voltage variations change operating points of transistors and may cause some of them to operate in the linear region which is not desirable. In order to compensate bias voltage variations, often CMFB circuits are used. Since the tail current

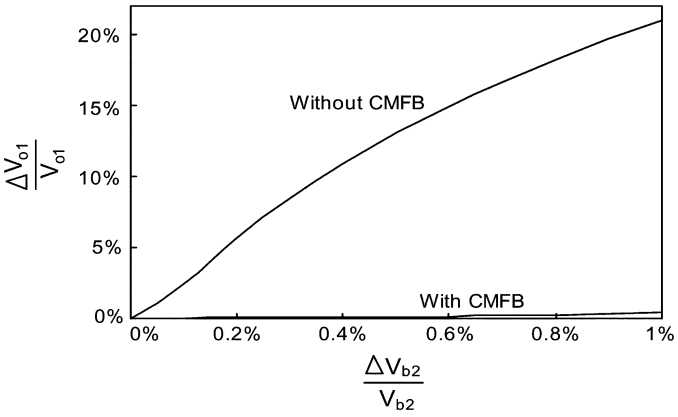

Fig. 3. Percentage variation of V_{o1} versus percentage variation of V_{b2}.

transistor (M_{11}) is a PMOS transistor, it is possible to apply feedback voltage to its body to counter the biasing voltage variations. Two PMOS transistors (M_9, M_{10}), acting as two large resistors, are employed to detect the common mode voltage. The feedback voltage (V_f) is applied to change the body voltage of the tail current source transistor M_{11}. Bodies of M_9 and M_{10} are biased at approximately 0.4 V to improve the operating range of the CMFB technique. In the steady state, the source voltage of M_9 and M_{10} is approximately 0.6 V. This forward biases the body of M_9 and M_{10} by a voltage of approximately 0.2 V. Therefore, the threshold voltage of these transistors is reduced, making them suitable for low-voltage operation. Using the previously mentioned circuit technique, a negative continuous time CMFB mechanism is realized. This CMFB loop compensates any perturbation in V_{b1}, V_{b2}, and V_{b5} by changing the body voltage of M_{11}. As a result of the CMFB, the amplifier can tolerate larger parameter variations during fabrication and the CMRR of the amplifier is improved.

B. Simulation Results

To verify the effectiveness of the proposed CMFB circuit against parametric variations, the circuit is simulated with and without the CMFB. The simulations are carried out for two different situations: 1) without any perturbations in biasing transistors and 2) with perturbations in biasing transistors. Fig. 3 shows the percentage of voltage change at the output of the first stage (V_{o1}^+, V_{o1}^-) due to a change in V_{b2}. Clearly, the proposed CMFB effectively reduces the impact of any source that causes common mode errors, like the bias voltage V_{b2}.

The feedback transistors of the proposed CMFB circuit should be sized such that they do not load the output stage of the amplifier. The equivalent resistance of the feedback transistors M_9 and M_{10} affects the amplifier's differential mode and common mode gains. If the resistance of M_9 and M_{10} is low, then it will degrade the differential gain of the amplifier. Therefore, the W/L ratio of these transistors should be as small as possible to keep this resistance as high as possible. On the other hand, if the resistance of M_9 and M_{10} is very large, then the feedback gain will be reduced. This reduces the effectiveness of the CMFB and, hence, the CMRR. Therefore, in order to size the feedback transistors a designer should strike a compromise between the CMRR and the differential gain of the amplifier. Table I shows the simulation results of the amplifier for three different sizes of the feedback transistors. The biasing current of the amplifier is kept the same for all three different sizes of the feedback transistor. As can be shown in Table I, the differential gain of the amplifier decreases as the W/L ratio of the feedback transistors increases. Meanwhile, increasing the W/L ratio of M_9 and M_{10} increases.

TABLE I
EFFECT OF THE SIZE OF M_9 AND M_{10} ON THE PERFORMANCE OF THE AMPLIFIER

M9, M10 W/L (μm)	Differential mode gain	Common mode gain	CMRR (dB) (@ 1 KHz)
0.25/20	394	2.0	45.89
0.6/20	390	1.6	47.46
0.95/20	370	1.4	48.45

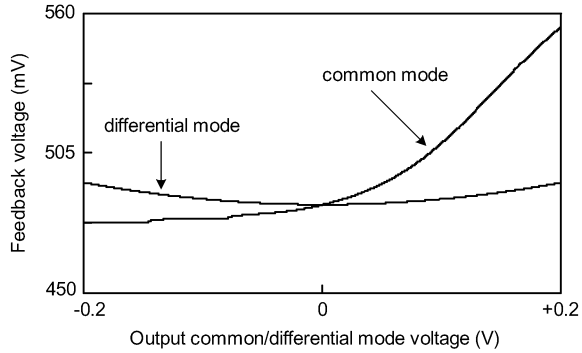

Fig. 4. Feedback voltage generated by the CMFB circuit with respect to the common mode and differential mode output voltage.

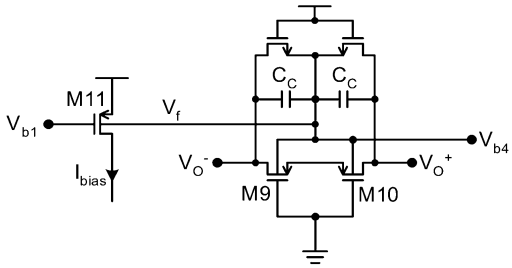

Fig. 5. Using CMOS combination for sampling the common mode voltage.

Another point that should be mentioned here is that the feedback voltage generated by the common mode voltage sampling circuit should be independent of the differential output voltage. In the previous amplifier, two PMOS transistors are used as two large resistors to sample the output common mode voltage. Clearly, the two transistors can not behave exactly as two linear resistors. Fig. 4 shows the response of the sampling circuit to the common mode as well as the differential mode voltage at the output of the amplifier. It is apparent from this figure that the feedback voltage changes as a result of differential output voltage, which is not desirable. In order to improve the behavior of the common mode sampling circuit one can use two NMOS transistors in parallel to the PMOS transistors as shown in Fig. 5. The feedback voltage generated by this circuit is shown in Fig. 6 with respect to the common mode and the differential mode output voltage. Comparing Fig. 4 with Fig. 6, it is clear that using both PMOS and NMOS transistors for sampling the common mode voltage improves the performance of the common mode sampling circuit.

C. Measurement Results

The 0.8-V folded cascode amplifier of Fig. 2 with embedded CMFB, is implemented in 0.18-μm CMOS technology. The die microphotograph is shown in Fig. 7. For comparison purposes, we implemented the amplifier with and without the CMFB. The amplifier without the CMFB occupies an area of approximately 4500 μm^2. The CMFB circuit required an additional area of approximately 10 μm by 60 μm which is 13% of the area of the amplifier. The two amplifiers are tested

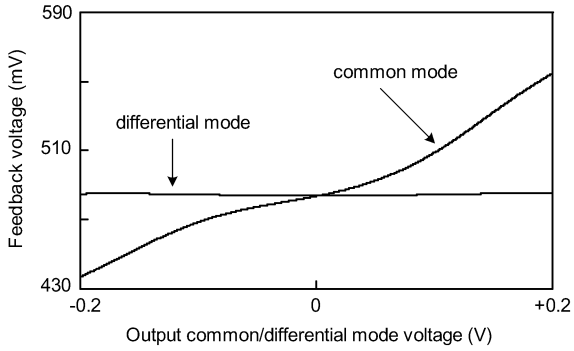

Fig. 6. Feedback voltage generated by the feedback of the circuit of Fig. 7 with respect to the common and differential output voltage.

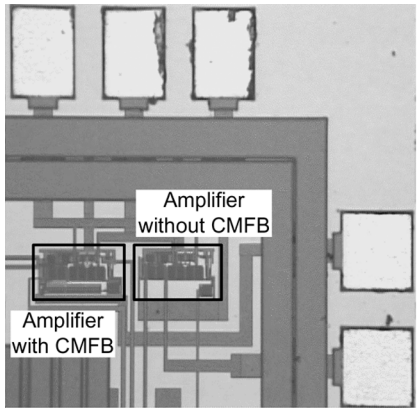

Fig. 7. Die microphotograph showing part of the chip that includes the two amplifiers (with and without CMFB).

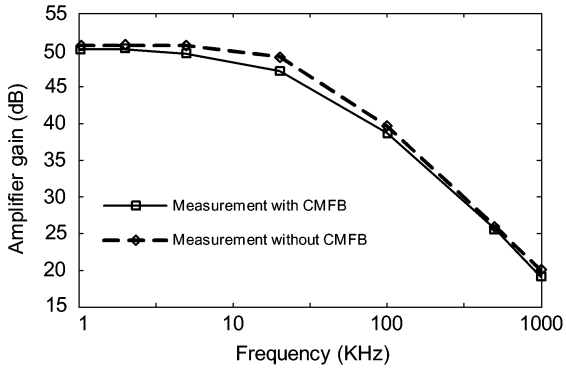

Fig. 8. Frequency response of the amplifier with and without the CMFB circuit.

at room temperature with a power supply voltage of 0.8 V. The load capacitance, including capacitances of the input/output (I/O) pad, trace, and test equipment is estimated to be approximately 4 pF.

Fig. 8 shows the measured frequency response of the two amplifiers. The gain of the amplifier with the CMFB is approximately 0.5 dB less than the gain of the amplifier without the CMFB. This is expected since the CMFB transistors reduce the overall resistance at the output of the amplifier. The measured performance parameters of the two amplifiers as well as the post layout simulations results are summarized in Table II. The implemented amplifier has an input offset voltage of 0.22 mV. Also, note that the CMFB has improved the CMRR by approximately 12 dB.

TABLE II
MEASURED PERFORMANCE PARAMETERS OF AMPLIFIERS

	Measurement with CMFB	Measurement without CMFB	Post layout with CMFB
DC diff. gain (dB)	50.1	50.6	52.1
GBW (MHz)	9.1	10	11.2
CMRR (dB) (@ 1 KHz)	48.4	36.1	51.2
Input offset voltage (mV)	0.22	0.22	N/A
Power consumption (V_{dd}=0.8V)	51μW	51μW	45μW

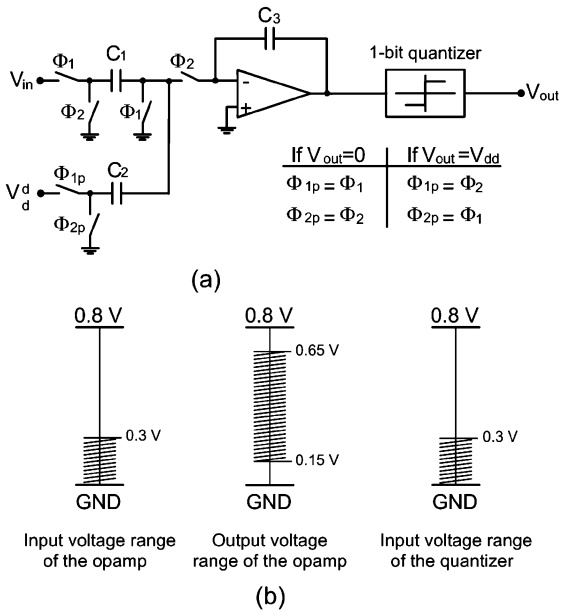

Fig. 9. Simple first-order $\Delta\Sigma$ modulator and the voltage range at different points of the circuit.

IV. 1-Bit Quantizer With Rail-to-Rail Input Range for Sub 1-V $\Delta\Sigma$ Modulators

Delta-sigma analog-to-digital (ADC) converters are very suitable for low-voltage applications. Most $\Delta\Sigma$ ADCs use a 1-bit quantizer at the output. In a sub 1-V $\Delta\Sigma$ modulator, not only the design of different building blocks becomes more difficult, but also the coupling of signals amongst these blocks becomes a nontrivial task. Fig. 9(a) shows the schematic of a simple first-order $\Delta\Sigma$ modulator. In a low-voltage modulator, the opamp, switches, and the quantizer should all operate with a low-supply voltage. In an opamp, depending upon the type of transistors (NMOS or PMOS) used at the input stage, the opamp input voltage range will be close to either $V_{\rm dd}$ or GND. However, the output voltage of the opamp is normally biased at $V_{\rm dd}/2$. In the quantizer, the input range is also close to either of the supply rails. The voltage ranges at the input and output of the opamp as well as at the input of the quantizer are shown in Fig. 9(b). Clearly, the output range of the opamp and the input range of the quantizer have a very small overlap. This makes the signal coupling of these two blocks difficult [12]. One way to overcome this problem is to shift the output voltage of the opamp to lower voltages. This dc shifting is not trivial in low-voltage circuits and consumes extra power. Alternatively, we can use a quantizer with rail-to-rail input range. This helps the designer couple the quantizer directly to the opamp.

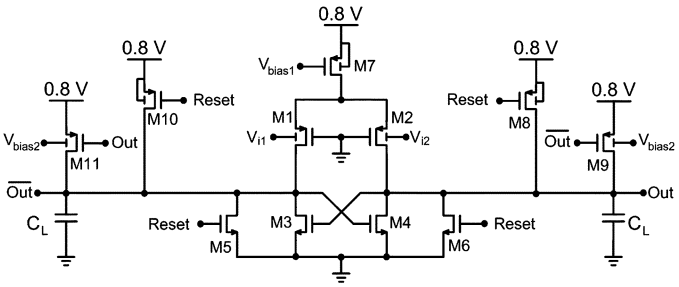

Fig. 10. Schematic of the 1-bit quantizer.

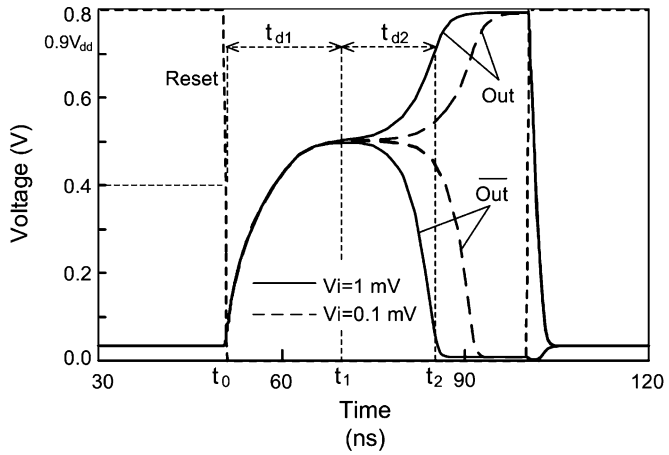

Fig. 11. Transient response of the comparator for two different input levels.

A. 1-Bit Quantizer Using DTMOS Technique

We have used the body of the PMOS transistors as the input terminals to make a track and latch comparator with rail-to-rail input range. Fig. 10 shows the schematic of the quantizer. The gate terminals of the input PMOS transistors (M_1 and M_2) are connected to ground while the body contacts are used as inputs. The comparator (quantizer) has two operational phases which are separated by the *Reset* signal. In the case of a $\Delta\Sigma$ modulator, the *Reset* is connected to the system clock. When the *Reset* is high, the comparator is in the tracking phase. In a typical track and latch comparator, during the tracking phase the comparator is biased at the metastable point by shorting the two outputs to each other by a switch [13]. This method is not suitable for low-voltage application, since it is not easy to turn on the switch that shorts the two outputs. To avoid this problem during the tracking phase, the two outputs of the comparator are shorted to GND by transistors M_5 and M_6. In the tracking phase, the current through transistor M_7 is divided between the two transistors M_1 and M_2. Depending upon the body voltage of these transistors, their drain currents are different. When the *Reset* gets low (latching phase), the voltages at the two outputs start rising. After the output voltages reach a certain value (the switching threshold voltage of the comparator) the cross coupled transistors M_3 and M_4 form a positive feedback and, depending upon the initial currents of M_1 and M_2, one of the outputs goes to $V_{\rm dd}$ and the other one goes to GND.

B. Simulation Results

Fig. 11 illustrates the transient response of the comparator with a capacitive load of 1 pF running at a frequency of 10 MHz. The transient response depicts two cases: 1) $V_i = 1$ mV and 2) $V_i = 0.1$ mV. Clearly, when the input has a larger value, the comparator response is faster. This is because the difference between the currents of M_1 and M_2 is larger which, in turn, enables the quantizer to reach the final state faster. The delay response of the comparator in the latching phase can be divided into two time periods. In the first period, it takes finite time t_{d1}, to charge outputs to the quantizer switching threshold. During this time the positive feedback is not yet operational. In the second period when the positive feedback is effective, it takes time t_{d2}, for outputs to reach their final values. Table III shows t_{d1}, t_{d2}, and the total delay ($t_{d=}t_{d1+}t_{d2}$) of the comparator for different differential values of V_i. From this table, it is apparent that there is a compromise between the maximum operating frequency of the comparator and the input voltage resolution. According to Table III, when the differential input voltage is 10 μV, the delay of the comparator is 49.15 ns. This delay should be smaller than a half period of the clock. Therefore, running the comparator at a clock frequency of 10 MHz can provide a signal resolution of 10 μV. Increasing the clock frequency reduces the quantizer resolution.

TABLE III
DELAY OF THE COMPARATOR FOR DIFFERENT DIFFERENTIAL INPUT VALUES

V_i	10 μV	100 μV	1 mV	10 mV
t_{d1} (ns)	26.25	23.05	19.95	16.75
t_{d2} (ns)	22.9	19.2	15.8	12.3
t_d (ns)	49.15	42.25	35.75	29.05

In the proposed circuit, transistors M_8 to M_{11} are used to speed up the circuit. These transistors source currents to output nodes after the *Reset* is inactivated and, hence, t_{d1} is reduced. The body of transistors M_9 and M_{11} are forward biased to reduce their threshold voltage. It is also possible to increase the biasing current and size of the input transistors to reduce the delay. Therefore, there is a compromise between speed and power consumption, too.

C. Measurement Results

The quantizer of Fig. 10 is implemented in 0.18-μm CMOS technology on the same chip with the amplifier. It takes an area of approximately 45 μm by 40 μm. In order to drive the capacitive load of about 4 pF due to I/O pads and packaging pins, two large drivers are added at the outputs of the quantizer. To test the performance of the quantizer, a sine wave signal with a frequency of 1 kHz and an amplitude of 70 mV is applied to the input of the circuit. The clock frequency is chosen to be 1 MHz. The supply voltage used to test the quantizer is 0.8 V. The dc offset of the quantizer is measured to be approximately 10 mV. The quantizer is capable to operate at frequencies of up to 2.5 MHz. The limitation in the clock frequency is coming from the large load at the output of the buffers implemented on the chip to drive the I/O pads. The quantizer itself is able to operate at higher frequencies.

V. CONCLUSION

In this paper, we discussed the DTMOS technique and its potential advantages in analog circuits. To show the effectiveness of this technique, we presented a method to implement a continuous time CMFB circuit for fully differential amplifiers using the DTMOS technique. The DTMOS technique makes the CMFB circuit simple and when the CMFB is used in a folded cascode amplifier, it does not consume any extra power. The measurement results of the amplifier show that the proposed CMFB circuit has increased the CMRR of the amplifier by 12 dB. As another example, to show the benefit of using DTMOS technique, a new track and latch comparator (quantizer) was presented. Using the DTMOS technique allows us to implement a quantizer with a rail-to-rail input voltage range. This is advantageous in sub-1-V circuits. The simulation and measurement results of the proposed quantizer were presented.

REFERENCES

[1] *"International Technology Roadmap for Semiconductor,"* Semiconductor Industry Association, 2001.

[2] F. Callias, F. H. Salchli, and D. Girard, "A set of four IC's in CMOS technology for a programmable hearing aid," *IEEE J. Solid-State Circuits*, vol. 20, no. 4, pp. 301–302, Apr. 1989.

[3] *Energizer*, [Online]. Available: http://www.energizer.com

[4] F. Maloberti, F. Francesoni, P. Malcovati, and O. J. A. P. Nys, "Design considerations on low-voltage low-power data converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 11, pp. 853–863, Nov. 1995.

[5] V. Peluso, P. Vancoreland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV low-power delta-sigma A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.

[6] T. Lehman and M. Cassia, "1-V power supply CMOS cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1082–1086, Jul. 2001.

[7] M. Maymandi-Nejad and M. Sachdev, "Continuous time common mode feedback technique For sub 1-V analog circuits," *Electron. Lett.*, vol. 38, no. 23, pp. 1408–1409, Nov. 2002.

[8] M. Maymandi-Nejad and M. Sachdev, "1-bit quantizer with rail to rail input range for sub 1-V delta sigma modulators," *Electron. Lett.*, vol. 39, no. 12, pp. 894–895, Jun. 2003.

[9] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," in *Int. Electron Devices Meeting, Techn. Digest*, 1994, pp. 809–812.

[10] F. Assaderaghi, "DTMOS: Its derivatives and variations, and their potential applications," in *Proc. 12th Int. Conf. Microelectron.*, 2000, pp. 9–10.

[11] J. F. Duque-Carillo, "Control of common mode component in CMOS continuous time fully differential signal processing," in *Analog Integrated Circuits and Signal Processing, An International Journal*. Norwell, MA: Kluwer, 1993.

[12] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV Low Power $\Delta\Sigma$ A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.

[13] M. Dessouky and A. Kaiser, "Very low voltage digital audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.

Reduced Complexity Interpolation Architecture for Soft-Decision Reed–Solomon Decoding

Xinmiao Zhang

***Abstract*—Reed–Solomon (RS) codes are one of the most widely utilized block error-correcting codes in modern communication and computer systems. Compared to hard-decision decoding, soft-decision decoding offers considerably higher error-correcting capability. The Koetter–Vardy (KV) soft-decision decoding algorithm can achieve substantial coding gain, while maintaining a complexity polynomial with respect to the code word length. In the KV algorithm, the interpolation step dominates the decoding complexity. A reduced complexity interpolation architecture is proposed in this paper by eliminating the polynomial updating corresponding to zero discrepancy coefficients in this step. Using this architecture, an area reduction of 27% can be achieved over prior efforts for the interpolation step of a typical (255, 239) RS code, while the interpolation latency remains the same.**

***Index Terms*—Guruswami–Sudan (GS) algorithm, interpolation, Koetter–Vardy (KV) algorithm, Reed–Solomon (RS) code, soft-decision decoding, VLSI architecture.**

I. INTRODUCTION

REED–SOLOMON (RS) codes have very broad applications in satellite and deep-space communications, frequency-hopping spread-spectrum systems, and magnetic and optical recording. Numerous research has been carried out on the decoding of RS codes since they were introduced in the 1960s. RS codes are maximum distance separable (MDS) codes, i.e., the minimum distance of an (n, k) code is $d_{\min} = n - k + 1$. Traditional RS decoding algorithms, such as the Berlekamp–Massey algorithm (BMA) [1], can correct errors up to $d_{\min}/2$. In contrast, list-decoding algorithms attempt to find all the codewords within a distance that is longer than $d_{\min}/2$ from the received word. A breakthrough in list-decoding was achieved by Sudan [2] and Guruswami–Sudan (GS) [3] based on an algebraic interpolation technique.

Compared to hard-decision decoding, soft-decision decoding of RS codes can achieve better performance by making use of the reliability information available from the channel. Koetter and Vardy incorporated the soft information received from the channel into the interpolation process of the GS algorithm [4]. As a result, substantial coding gain can be achieved while the complexity is polynomial with respect to the codeword length. The two major steps of the Koetter–Vardy (KV) algorithm are the interpolation and the factorization. Various algorithmic and architectural modifications [5]–[8] have been proposed to facilitate the hardware implementation of these two steps. After applying these modifications, the complexity of the interpolation step dominates. The interpolation step consists of discrepancy coefficient computation and polynomial updating. In this paper, a novel scheme is proposed to reduce the complexity of polynomial updating by exploring the characteristics of the discrepancy coefficients. For practical decoding with frame error rate (FER) less than 10^{-2}, the proposed interpolation architecture can achieve an area reduction of 27% for a (255, 239) RS code, while the latency remains the same.

Manuscript received October 31, 2005; revised April 23, 2006.

The author is with the Department of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, OH 44106-7071 USA (e-mail: xxz36@case.edu).

Digital Object Identifier 10.1109/TVLSI.2006.884177