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An ultra low-power low-voltage switched-comparator successive approximation analog to digital converter

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Abstract: A 9-bit ultra low-power successive approximation analog-to-digital converter (SA-ADC), which is able to operate at very low supply voltage, is presented. The low power consumption is achieved by using new switched-comparator architecture. In the proposed architecture the comparator, which is one of the most power hungry blocks of the SA-ADC, is switched off after the decision-making interval as well as during reset time to save power. The SA-ADC is simulated in the 0.18 μm CMOS technology and the simulation results are provided. The switched-comparator SA-ADC consumes 412 nW at 0.5 V and as a result of the proposed switching scheme a power saving of 17.4% is obtained. It provides a signal-to-noise-and-distortion ratio (SNDR) of 50.36 dB at the sampling rate of 12.5 kS/s.

Keywords: SA-ADC, low-power, switched-comparator

Classification: Integrated circuits

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1 Introduction

In many applications such as bio-implantable devices, portable communication devices, hearing aids, etc., there is a growing demand for the development of low voltage and low power circuits and system building blocks. Low power consumption is of great interest because it increases the battery lifetime. One of the main building blocks in many applications is the analog-to-digital converter (ADC) which serves as an interface between the analog world and the digital processing unit. In most biomedical applications and many other low power applications the operating frequency of the ADC is not very high. Since SA-ADCs have low power consumption and low operating frequency, they are of great interest in such applications. In [1] a 0.5 V SA-ADC is presented and the design issues of the ADC with ultra low supply voltage are addressed. The SA-ADC in [1] consumes 850 nW at 0.5 V and has a SNDR of 43.3 dB (8-bit mode) at the sampling rate of 4.1 kS/s. A 0.9 V 8-bit SA-ADC dedicated for low power applications is presented in [2]. This SA-ADC employs a bootstrapped switch, which is placed in the sample-and-hold block. It provides a peak SNDR of 47.7 dB and consumes 2.47 μW at the supply voltage of 0.9 V and the sampling rate of 200 kS/s.

In all these designs the comparator of the SA-ADC, which is one the most power hungry blocks, is always on. In order to reduce the power consumption of the ADC it is possible to turn the comparator off when the decision is made and the comparator is not needed until the next clock cycle. In this paper a SA-ADC is presented in which a track and latch comparator is used and the comparator is turned off during most of a clock cycle. This reduces the power consumption of the comparator considerably.

2 The architecture of a SA-ADC

Fig. 1 (a) shows the block diagram of a SA-ADC. It consists of a sample-and-hold (S/H), a comparator, a successive approximation register (SAR), and a digital to analog converter (DAC). As the name implies, DAC's output voltage successively approximates the sampled input voltage. The register bits are set, one at a time, and produce an input to the DAC. In each clock cycle, using binary search algorithm, one bit of the digital output is obtained. The SAR is a digital circuit and can be designed to be very low power. The DAC is typically implemented by switched capacitors and is not a very power consuming block. The comparator, which is typically a track and latch comparator, is an analog circuit and consumes a considerable amount of power compared to other blocks. Hence, the design of the comparator is critical in an extremely low power SA-ADC. Fig. 1 (b) shows a typical track and latch comparator. The operation of this comparator can be divided into two phases ('reset' and 'evaluation' phases). During the reset phase (when the clock signal *clk* is high) the two outputs are shorted to ground by transistors M3a and M3b. During the evaluation phase M3a and M3b turn off and the bias current (I_{bias}) is divided between the two input transistors (M1 and M2) depending on the inputs. As a result the voltages at the *out* and *out*$^-$

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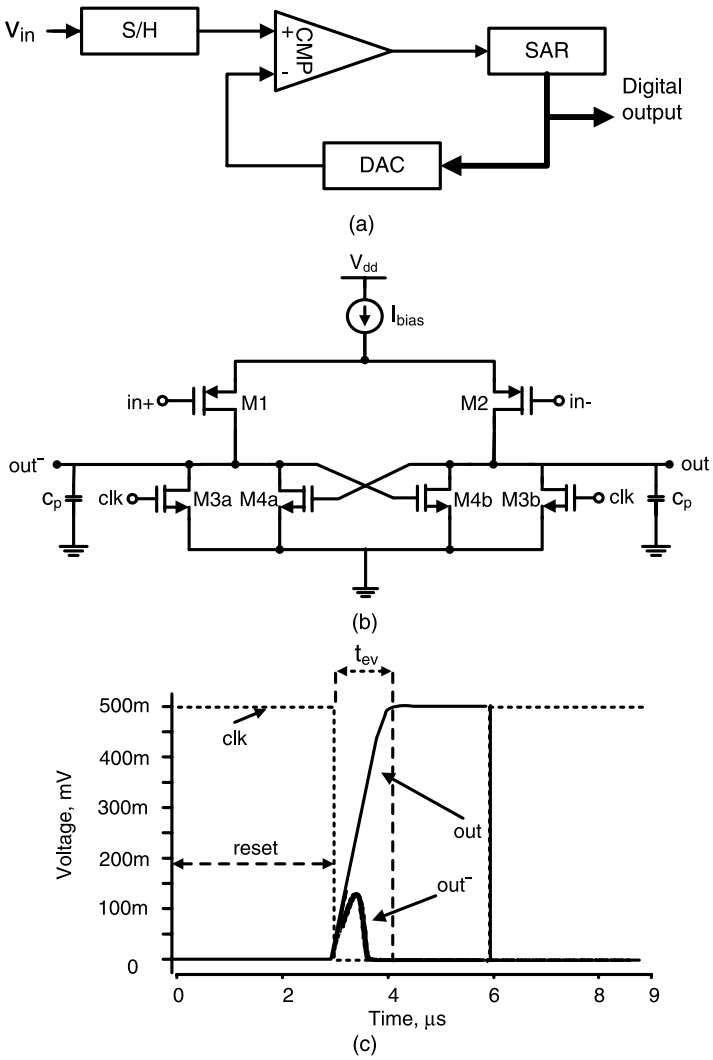

Fig. 1. (a) block diagram of a successive approximation ADC. (b) schematic diagram of a typical track and latch comparator. (c) transient response of the comparator.

nodes rise until the positive feedback due to the cross coupled transistors M4a and M4b is activated and one of the output nodes goes to V_{dd} and the other one goes to GND. This is shown in Fig. 1 (c). The time required for the outputs to settle to their final values is called evaluation time and is shown by t_{ev} on the figure. The evaluation time t_{ev} is a function of the bias current (I_{bias}), the input differential voltage and the parasitic capacitances (C_p) at the output nodes. The bias current I_{bias} determines the speed of the comparator and should be large enough such that the outputs can reach V_{dd} and GND during half of the clock cycle (the evaluation phase). Hence, a faster comparator consumes more power. In the next section we propose a switched-comparator SA-ADC. In the proposed circuit an additional clock signal is used which serves as an enable to turn on the comparator only during the decision-making interval.

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3 The proposed switched-comparator SA-ADC

In many low power applications the comparator is not needed to be always on because the frequency of operation is not high. Moreover, sometimes ADCs are not required to operate at their maximum speed. In such cases the comparator is idle for most of the time. Hence, it can be switched off during a specific period of time in each clock cycle in order to save power. This is the main idea used in the proposed comparator (hence the name 'switched-comparator').

Fig. 2 (a) shows the schematic diagram of the proposed comparator. It is designed as a regenerative resetable circuit with additional transistors M5a, M5b for power reduction. This comparator requires two separate clock signals (*clk1* and *clk2*). The timing diagram of *clk1* and *clk2* and the transient response of the comparator are shown in Fig. 2 (b). When *clk1* is high the comparator is in the reset phase. When both *clk1* and *clk2* are low transistors M3a and M3b turn off and transistors M5a and M5b turn on and the comparator goes into the evaluation phase. In the evaluation phase the out-

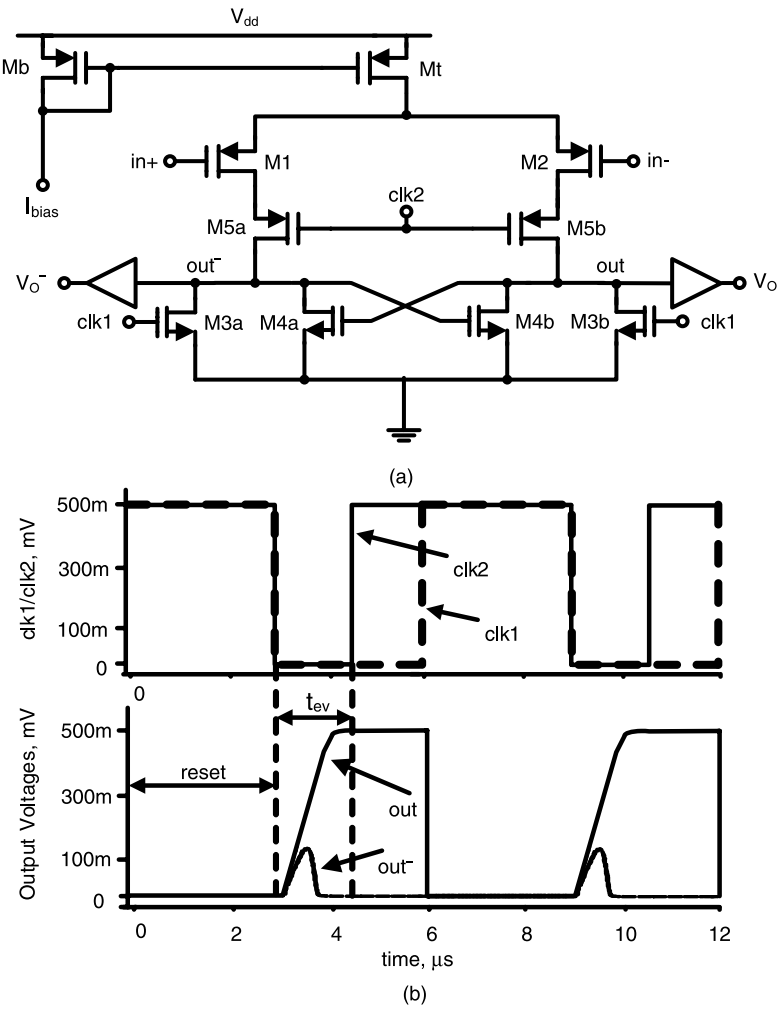

Fig. 2. (a) schematic diagram of the proposed comparator. (b) transient response of proposed comparator.

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put voltages start rising and after reaching a certain value (i.e. the switching threshold of the comparator), the positive feedback formed by cross-coupled transistors M4a and M4b causes one of the outputs to go to V_{dd} and the other one to go to GND. After reaching this point, *clk2* becomes high (and remains high during the reset phase of the next cycle), hence transistors M5a and M5b turn off and prevent further flow of current between the supply rails. This leads to a reduction in the power dissipation. Note that in the traditional comparator (like the one shown in Fig. 1) the current continues to flow from Mt to M1 and/or M2. In this way, the current is taken from V_{dd} only during t_{ev} and the comparator is off in the remaining part of the cycle. The time interval during which *clk2* is low (t_{ev}) should be chosen large enough to give the output voltages enough time to reach their final values under the worst case condition. The worst case scenario happens when the input differential voltage is minimum and the input common mode voltage is maximum. For a tail current (I_{Mt}) of 0.5 μA and a *clk1* period of 6 μs, we set t_{ev} to 1.5 μs. This value is chosen based on the worst case evaluation time in our application. The worst case evaluation time is obtained by choosing the minimum value for the differential input voltage and the maximum value for the input common mode voltage. It is worth mentioning that in the designed SA-ADC the input common mode voltage range is between 0 V and $V_{dd}/2$.

The addition of transistors M5a and M5b makes the design of the circuit more challenging since these transistors are placed in series with the input transistors M1 and M2 and may degrade the speed of the circuit. Note that in a low voltage circuit, transistors M1 and M5a (and also M2 and M5b) form a cascode configuration during the evaluation phase. However, these transistors operate in the subthreshold region, and therefore, should be sized large enough so that they can operate with the required speed. Also, note that the *clk2* can be generated from *clk1* with a few digital delay elements and static gates. These extra gates do not increase the power consumption of the circuit noticeably since the power consumption of CMOS static gates is negligible.

In the proposed comparator, the two output nodes *out* and out^- are connected to buffers before being connected to the rest of the circuit. This ensures that the comparator transient response is not affected by the comparator load. The buffers also ensure a rail-to-rail voltage swing at the final outputs (V_O and $V_O{}^-$). Although most of the transistors of the comparator operate in week inversion, the maximum operation frequency of the circuit is high enough since only a small capacitive load has to be driven at the drain of M5a and M5b.

In our circuit current of the tail transistor Mt is chosen to be 0.5 μA based on the simulation results. In order to generate this tail current a bias current of 50 nA is chosen for the current mirror transistor Mb, and Mt is sized 10 times larger than Mb. This increases the power consumption of the circuit by an amount of 25 nW. In a complete circuit, typically there is bias network that generates all the bias voltages needed in the circuit. If this is the case then this extra 25 nW can be eliminated.

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The proposed comparator is successfully used in a SA-ADC in the 0.18 μm CMOS technology. The sample-and-hold circuit is based on the bootstrapped circuit presented by Abo et al [3]. The DAC is implemented using binary weighted capacitors. The capacitors are multiples of a unit capacitor of 20 fF. Since switching at ultra low supply voltage is only possible if dc level of the signal to be switched is close to V_{dd} or GND, we used V_{dd} and GND as reference levels in DAC's switches so that the switches can be implemented using a single NMOS or PMOS transistor. A shunt capacitor is used in the DAC as capacitor divider to adjust the amplitude of input signals. The amplitude of the input voltage is chosen to be half of the supply voltage, i.e. 250 mV. The implemented SAR is based on the design presented in [4]. The heart of the SAR and control logic is an edge-triggered D flip-flop. Simulation results show that the total power dissipation of the switched-comparator SA-ADC is 412 nW at 0.5 V. If the proposed switched-comparator technique is not used, the power consumption would be 499 nW. Hence, a considerable power reduction of approximately 17.4% is obtained. Power consumption of the comparator, the sample-and-hold, DAC and SAR are 12.2 nW, 119.5 nW, 26.3 nW and 254.6 nW, respectively. Note that a major part of the power consumption comes from the SAR. The power saving due to the proposed switching scheme would be larger if a lower power SAR is used.

Table I. comparison between SA-ADC presented in [1] and the proposed SA-ADC.

	Supply voltage	Sampling rate	Number of bits	Input signal swing	SNDR	Power dissipation	Technology
SA-ADC presented in [1]	0.5V	4.1kS/s	8	0.125V	43.3dB	850nW	0.18µm CMOS, V_{tn}=0.43V, V_{tp}=-0.38V
Designed SA-ADC	0.5V	12.5kS/s	9	0.25V	50.36dB	412nW	0.18µm CMOS, V_{tn}=0.445V, V_{tp}=-0.437V

Table I provides a comparison between the designed SA-ADC and the converter presented in [1]. It should be mentioned that the results in [1] are obtained from measurement of the fabricated SA-ADC while in our case the specification are obtained from simulations.

4 Conclusion

Successive approximation ADCs (SA-ADC) are suitable candidates for low frequency low power applications, like biomedical devices. The power consumption of a SA-ADC can be reduced by switching the comparator block off after the decision is made in each clock cycle. A 9-bit ultra low power switched-comparator SA-ADC is presented in this paper. The proposed SA-

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ADC can operate with a supply voltage of as low as 0.5 V in 0.18 μm CMOS technology. The HSPICE simulation results show considerable reduction in power dissipation when the switched-comparator technique is used (a power reduction of approximately 17.4%). The ADC provides a SNDR of 50.36 dB at the supply voltage of 0.5 V at a sampling rate (f_s) of 12.5 kS/s and input frequency of 31 f_s/64.

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