# An Ultra-Low-Power 10-Bit 100-kS/s Successive-Approximation Analog-to-Digital Converter

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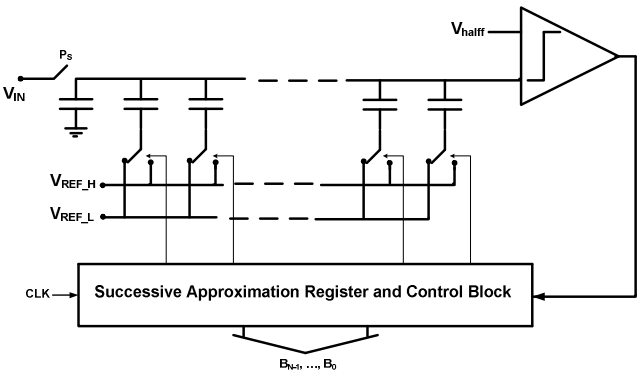
***Abstract*— Successive-approximation analog-to-digital converters (SA-ADCs) have recently been widely used for moderate-speed moderate-resolution applications where power consumption is of major concern. In this paper, several techniques are proposed to further reduce the power consumption of an SA-ADC. These solutions include a split-segmented architecture for the capacitor-based digital-to-analog converter (DAC), a modified switching scheme for the DAC, and employing a smaller supply voltage for the comparator and the successive-approximation register while using a new power-efficient digital level converter. Spectre simulation results of a single-ended 10-bit 100kS/s SA-ADC in a 0.13-µm CMOS technology employing the proposed techniques show that the ADC (excluding reference buffers) consumes less than 1 µW of power while offering an effective number of bits of 9.2.**

## I. INTRODUCTION

Successive-approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in energy-efficient moderate-resolution/moderate-speed applications due to their minimal active analog circuit requirements [1-12]. In a SA-ADC, a digital-to-analog converter (sub-DAC) tries to estimate the value of each sample of the input analog signal through successive approximations and comparisons. Based on the ADC resolution, after a particular number of cycles, the digital word stored in the successive-approximation register (SAR) corresponds to the analog sample with a particular quantization error. Fig. 1 demonstrates a single-ended realization example of a capacitor-based SA-ADC [1]. In this ADC, during the sampling phase when the sampling switch is on, the most-significant bit (MSB) is set to "1" while all other bits are "0" and thus the bottom plates of half of the capacitors are tied to $V_{REF\_H}$ and the rest to $V_{REF\_L}$. After disconnecting the sampling switch, the input signal, already sampled on the sub-DAC capacitors is compared to $V_{half}=(V_{REF\_H}-V_{REF\_L})/2$ and the MSB is decided to remain "1" or set back to "0". Then, the next most-significant bit is set to "1" and this procedure is repeated until all *N* bits are found. One advantage of this architecture is that the input common-mode level of the comparator is constant thus reducing its dynamic offset voltage [2]. Nevertheless, this architecture can readily be converted to a fully-differential version.




Single-ended realization example of an SA-ADC

In this paper, in order to reduce the energy required to charge the capacitors, a modified architecture for the capacitive sub-DAC as well as a modified switching scheme is proposed. In order to be able to reduce the power consumption of the comparator and the digital circuits of the SAR by applying smaller supply voltage, power-efficient level converters are introduced for the interface between the SAR and the switches. As a design example, an ultra-low-power 10-bit 100kS/s SA-ADC has been designed and simulated using Spectre in a 0.13-µm CMOS technology.

The remainder of the paper is organized as follows. The proposed low-power solutions are explained in Section II. Design considerations of the realized ADC are addressed in Section III. Section IV presents simulation results of the ADC followed by conclusions in Section V.

## II. POWER-REDUCTION SOLUTIONS

In a successive-approximation ADC, power is consumed in the sub-digital-to-analog converter (sub-DAC), the comparator and the digital logic circuit. It should be noted that, usually, the power consumption of neither of these blocks can be ignored. In this section, first a modified architecture for the sub-DAC is presented, then the effect of a modification of the switching scheme of the sub-DAC on its power consumption is discussed and finally the advantages of the proposed dual-supply architecture are addressed. Although discussions are

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presented for a single-ended configuration (Fig. 1 (where $V_{REF\_H}=V_{DD}$ and $V_{REF\_L}=V_{SS}$)), they hold for fully-differential architectures as well.

### A. Unary-Weighted Capacitive DAC

In the sub-DAC, the power is mainly consumed while charging the capacitors. In conventional binary-weighted architectures, for each sample of the input signal, regardless of its value, all capacitors are, one by one, charged to $V_{DD}$ (and then discharged back or not, depending on the output of the corresponding comparison). However, if a unary-weighted (or thermometer-coded) architecture is used, then depending on the value of the input sample, fewer capacitors are needed to be charged. Let's consider a 5-bit example with an input smaller than $V_{DD}/2$ (corresponding to MSB equal to "0"). When the DAC input code changes from "10000" to "01000", in the binary-weighted DAC, 16 capacitors already connected to $V_{DD}$ are connected back to $V_{SS}$ and new 8 capacitors already discharged are connected to $V_{DD}$. The case for a unary-weighted DAC is different, as just 8 of the capacitors already connected to $V_{DD}$ are switched back to $V_{SS}$. In other words, for inputs smaller than $V_{DD}/2$, half of the capacitors are never charged. Assuming an equal probability for the input signal to be above or below $V_{DD}/2$, the power consumption of the sub-DAC is reduced by 25%. For those SARs where the "i-1"th code (i.e. $B_{i-1}$) is set high slightly earlier than the time when the previous code (i.e. $B_i$) is being decided, the power saving introduced by this technique would be less but still considerable and useful.

### B. Modified Switching Scheme

In conventional SA-ADC switching schemes, all bits (including the MSB) are reset to "0" at the beginning of the conversion process of each new input sample. A modified switching scheme is proposed here, where the MSB is not reset to "0" for every new sample. Instead, if the value of MSB for the previous analog sample has been "1", it is kept unchanged and therefore the corresponding capacitor(s), equal to half of the entire capacitors in the unary-weighted array, is kept un-discharged; i.e. the MSB capacitor(s) are kept charged until the input signal crosses the $V_{DD}/2$ level.

### C. Choice of Supply Voltages

In the comparator, the power consumption will reduce for smaller supply voltage, $V_{DD}$. In applications where the speed is low enough to allow small $V_{DD}$'s for the comparator (and also the offset requirement of the comparator can be met), this choice is advisable. In the 0.13-µm CMOS technology we have selected, in order to save power, a supply voltage as low as 0.5 V is suitable for the comparator with a clock frequency of 1.1 MHz (i.e., 11 times the sampling frequency of 100kS/s).

For digital circuits, the dynamic power consumption reduces with $V_{DD}^2$. The short-circuit power consumption also reduces considerably at lower supply voltages, especially if the supply voltage is smaller than the sum of the threshold voltages of the *n*- and *p*-MOS devices. Finally, the leakage power consumption also reduces proportionally with $V_{DD}$.

Although a smaller supply voltage leads to less power consumption for the comparator and the digital circuits, for the sub-DAC, however, this smaller supply voltage not only increases the sensitivity of the ADC to comparator noise, but also makes the switches more challenging to implement. Employing two different supply voltages for the analog and digital parts of the ADC is advantageous from a power-consumption point of view. It, however, introduces implementation challenges which will be discussed in the following Section.

## III. Circuit Implementation

In this paper, the power-reduction techniques mentioned above have been applied to a single-ended SA-ADC. In this section, design considerations for this ADC are discussed.

### A. Proposed Architecture

In a successive-approximation ADC, the unit capacitor value is determined either by the maximum kT/C noise power or by the required matching [3], although considering the parasitic non-linear capacitors at the input of the comparator is also important. In order to reduce the size of the entire capacitance, the "split architecture" [13] has been widely employed. In this paper, we propose the architecture shown in Fig. 2. The architecture is split into two parts by the attenuating capacitor, $C_A$, where a unary-weighted architecture is used to implement the $B_U$ most significant bits and a binary-weighted configuration to implement the $B_B$ least-significant bits (where $B_U+B_B=N$). In choosing the segmentation factor, i.e. the choice of $B_U$ and $B_B$, the power consumption and area overhead introduced by the binary-to-thermometer decoder (which drastically increases with the resolution, $B_U$) should also be considered not to be too large to compensate for the power saving proposed by the architecture.

In our 10-bit design, both $B_B$ and $B_U$ have been chosen equal to 5; therefore, 31 similar capacitors each sized $C_u$ are split from five binary-weighted capacitors of $C_u$, $2C_u$, … $16C_u$ (in addition to a non-switched capacitor of $C_u$) by an attenuating capacitor of $C_A$ (with a size of $32/31.C_u$) The value for the unit capacitor, $C_u$, in this 10-bit ADC is determined by the required matching rather than thermal noise and is chosen equal to 93fF. Compared to a sub-DAC without the splitting capacitor,

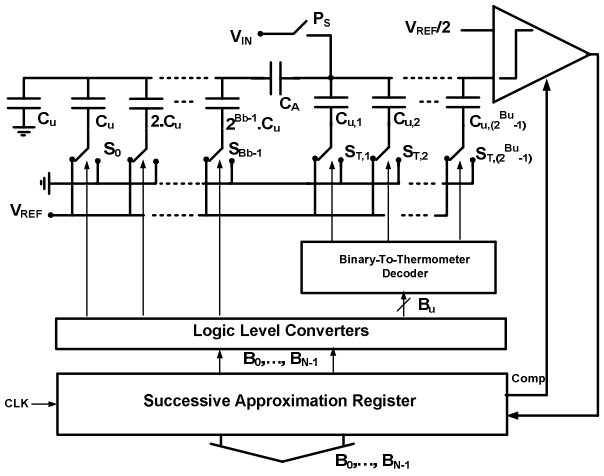


Figure 2. The proposed SA-ADC architecture

(with the same unit capacitor), the entire capacitance driven by the input signal is 32 times smaller. Compared to split architecture with the same unit capacitor, the power consumption is smaller not only because of the unary architecture but also because of the modified switching scheme.

With a supply voltage of 1-V (and also reference levels of 1V and 0V), a bootstrapped switch [14] is employed to guarantee good linearity for high-frequency inputs. For all other switches of the sub-DAC, minimum-sized *p*- or *n*-MOS devices have been employed. In the ADC layout, special attention must be paid to the parasitic capacitance at the left plate of $C_A$ (Fig. 2), which degrades the linearity of the ADC. Any non-linear parasitic capacitance at the DAC output node (comparator input), also limits the linearity at high frequencies.

### *B. Comparator*

For the comparator, in order to be able to handle a common-mode input level equal to its supply voltage (both equal to 0.5 V), the configuration depicted in Fig. 3 is employed. In this circuit, a regenerative latch is preceded by a pre-amplifier and followed by another latch. The input pre-amplifier (where all devices are biased in weak inversion) amplifies the input differential signal with a voltage gain of 3. In order for the pre-amplifier to operate correctly, the load devices are biased in the triode region. In the second phase (when the RESET signal becomes LOW), due to positive feedback, regeneration occurs, and the differential signal is converted to final digital levels of $V_{DD}$ and $V_{SS}$, respectively. With this architecture, signals with large input common-mode level can be applied to the comparator. Another advantage of this architecture is that the current can be adjusted for different sampling frequencies (with an on- or off-chip current source).

### *C. Logic Level Converter*

In the designed SA-ADC, the sampling switch and the sub-DAC, are controlled by a (digital) control block. Therefore, between the digital circuit (SAR) with supply voltage of 0.5V and the analog circuit with supply voltage of 1V (and reference levels of (1V, 0V)), a level converter is needed to convert the logic levels of (0V, 0.5V) to (0V, 1V) in an efficient way (i.e. with minimum additional power consumption).

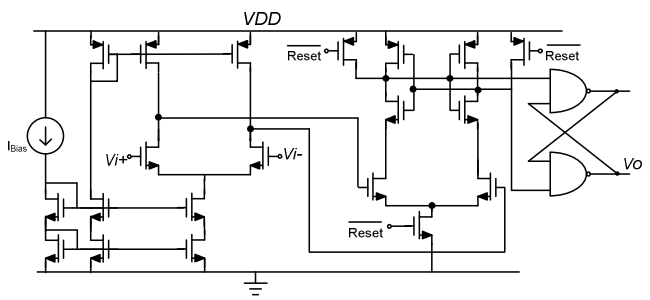


Figure 3. Schematics of the employed low-voltage comparator

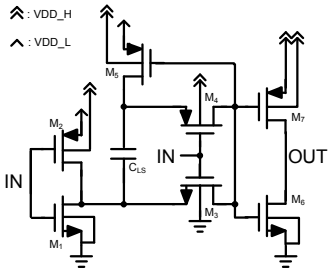


Figure 4. Proposed level converter:

For this purpose, the circuit proposed in [15] can be employed. However, here, we propose a simpler and more power-efficient level-converter circuit, shown in Fig. 4. The circuit works as follows: when the input signal is high (VDD_L), the output of the first inverter, which is low (VSS), is connected through pass transistor M3 (controlled by the input signal "IN") to the second inverter and thus the output of the second inverter, "OUT", is high (VDD_H). Meanwhile, the level-shifter capacitor, CLS, is charged with voltage VDD_L. When the input becomes low (VSS), the output of the first inverter turns high (VDD_L) and the top plate of the capacitor is shifted up to 2.VDD_L-$V_{DROP}$ where $V_{DROP}$ is the amount of voltage drop across the capacitor during the transition. This voltage is now high enough to be converted to a strong "low" output by the second inverter with little static current dissipation in the second inverter, provided that VDD_L is not less than half of VDD_H. In the entire ADC, ten level converters have been used and the outputs of the five more-significant bits are then applied to the binary-to-thermometer decoder working with a supply voltage of 1V.

### *D. SAR and Control Logic*

For the successive-approximation register, the structure employed in [3] has been modified to accommodate the switching scheme presented in Section-II-B. In order to minimize the power consumption, special attention is paid in low-power design of D-Flip-Flops. For the binary-to-thermometer decoder, the well-known row-column decoding scheme has been used.

## IV. SIMULATION RESULTS

A 1-V, 10-bit, 100kS/s SA-ADC has been designed and simulated in a 0.13-µm CMOS technology with Spectre. All devices are typical transistors with nominal threshold voltages. MIM capacitors with a density of roughly 2fF/µm$^2$ have been employed. A 1-V supply has been used for the sub-DAC and the binary-to-thermometer decoder and a 0.5-V supply has been employed for the comparator/SAR. With a single-supply voltage of 1 V, however, a DC-DC down-converter [16] can also be employed. Our simulations show that for the current level of the comparator and SAR, the efficiency of that DC-DC converter is more than 87%. The power consumption of the binary-to-thermometer decoder is 80nW (less than the power saving introduced by changing the binary DAC to unary DAC in the MSB part of the split architecture).

Table 1. Simulated Performance of the ADC

| | |
|---|---|
| Resolution | 10 bits |
| Sampling Rate | 100 kS/s |
| Input Voltage Range | 1 $V_{p-p}$ |
| Supply Voltage<br>(DAC, bin-thermo. decoder)<br>(Comparator, SAR) | <br>1 V<br>0.5 V |
| Current Consumption<br>(excluding reference buffers)<br>1-V Supply<br>0.5-V Supply | <br><br>470nA<br>1.05µA |
| Power Consumption | 1µW |
| THD<br>$f_{in}$=48.4375 kHz | <br>-60dB |
| SNDR | 57dB |
| FOM | 17 fJ/conversion-step |
| Technology | 0.13-µm CMOS |

For measuring the dynamic performance of the ADC, a sine-wave input signal has been applied to the converter. Simulated value of total harmonic distortion for a Nyquist-frequency input is -60dB. The current drawn from the 1-V supply voltage is 470nA and that of the 0.5-V supply, is 1.05uA. Our simulations show that if the same supply voltage of 1-V is used for the comparator and SAR, although the level converters can be omitted in this situation, the entire power consumption of the comparator/SAR will increase by a factor of more than 2. Table-1 summarizes the ADC performance. By defining the Figure-Of-Merit (FOM) as in [2] (i.e. $FOM=P_{diss}/(2^{ENOB}.f_S)$, where $P_{diss}$ is the power consumption, ENOB is the effective number of bits and $f_S$ is the sampling frequency) then this design would show a comparative FOM with the state-of-the-art provided that the measurement results also confirm with the simulations above.

## V. CONCLUSIONS

In this paper, several techniques to further reduce the power consumption of a moderate-frequency moderate-resolution SA-ADC were proposed and employed in a design of a 10-bit 100kS/s ADC. To reduce the power consumption of the capacitive DAC, a split-segmented architecture as well as a modified switching scheme was presented. For the comparator and the SAR, a smaller supply voltage was used and a power-efficient level converter was introduced. Simulation results of the ADC confirm that its effective number of bits is more than 9.2 for an input frequency of 48 kHz while consuming less than 1 µW. Although the proposed techniques were applied to a single-ended architecture, they are also applicable to fully-differential architectures.

## ACKNOWLEDGMENT

This work was supported in part by the Dutch Technology Foundation (STW) under grant DTC.6418 (BioSens).

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