A 0.8-V 420nW CMOS Switched-Opamp Switched-Capacitor Pacemaker Front-End With a New Continuous-Time CMFB

M. Daliri, M. Maymandi-Nejad
Electrical Eng. Department, Ferdowsi University of Mashhad, Mashhad, Iran
mo_da834@stu-mail.um.ac.ir, maymandi@um.ac.ir

Abstract—**A low-voltage low-power pacemaker Front-End for detecting QRS complex is presented in this paper. The circuit includes a switched-opamp switched-capacitor (SO-SC) preamplifier with a gain of 40db, a fourth-order Butterworth SO-SC filter with a sampling frequency of 1kHz, and an opamp with a new continuous time common mode feedback (CMFB) circuit which is able to operate with a very low supply voltage. The whole circuit operates with a supply voltage of 0.8V and consumes a power of 420nW.**

***Index Term*— Pacemaker, CMOS, Butterworth filter, Switched OpAmp, Switched-Capacitor, Low voltage, Continuous- time Common-Mode Feedback.**

I. INTRODUCTION

Cardiac pacemakers are the most popular implantable biomedical devices. These kinds of devices have to rely on a miniature battery as their energy source. Hence, power consumption is the main design issue in designing the electronic circuits of the pacemakers [1]. A typical pacemaker consists of several analog and digital sub-circuits. In order to detect the heartbeat, typically the QRS complex is detected in the front end circuit of a pacemaker. The front-end includes analog circuits to amplify, filter, and detect the QRS complex for further processing in the digital domain. Since the front end is mainly composed of analog circuits, the power consumption of this block becomes very important. Moreover, low voltage operation of this block is critical since miniature batteries provide a voltage of as low as 0.9V [2]. Therefore, there has been intensive research on the front end of a pacemaker, focusing on reducing its power consumption and supply voltage [3,4,5,6]. On the other hand fully differential architectures can provide higher signal to noise ratios compared to single ended circuits. One of the challenges of designing fully differential circuits in a low voltage application is the design of the common mode feedback (CMFB) circuit that can provide the required voltage swing. Lasanen et al [1] have designed a pacemaker front end, consisting a continuous time preamplifier and an 8^{th} order filter which works with a supply voltage of 1.0V-1.8V. In this design, they have used two single ended amplifiers instead of a fully differential one to overcome the problem of designing a low voltage CMFB circuit. Using two separate amplifiers in parallel causes the power consumption to increase. A pacemaker front end containing a continuous time preamplifier and an 3^{rd} order filter is designed by Lentola et al [4], taking a current of 900nA from a 2.0-2.8V supply. In this design, a single ended architecture is adopted for the implementation of the circuit. Single ended amplifiers do not need CMFB. However, the SNR of the system would be lower compared to a fully differential one. In this paper, we present a pacemaker front end, implemented in 0.18µm CMOS technology and operating with a supply voltage of as low as 0.8V. The circuit includes a preamplifier and a 4^{th} order Butterworth filter to detect QRS complex. We have used a new CMFB circuit, which is able to operate with very low supply voltages.

The paper is organized as follows. In section II the system level specifications of the front end are presented. The designed circuit of the front end is discussed in section III and the simulation results are provided. Conclusions are drawn in section IV.

II. System Description

The QRS complex is a good indication of the heartbeat. The amplitude of the QRS complex is very small; i.e. between 100µv and 2mv, depending on how it is measured. This means that the signal has to be amplified to a suitable level before further processing. In practice the quality of the QRS signal can be degraded by internal and external interference signals. Table I shows some of the heart signals as well as internal interference signals. As shown in this table, the largest signal among the signals of the heart is the QRS complex. Therefore, it is easier to detect heartbeat by detecting the QRS signal. This will lead to a better signal to noise ratio and a more reliable performance. Moreover, the frequency range of the QRS signal is between 20Hz to 60Hz. Therefore, to reduce the impact of unwanted signals a pass band filter for this frequency range should be used.

The implemented front end presented in this paper is optimized for detecting the QRS complex. The output of the front end can be used by a digital signal processing unit for further processing. Fig.1 shows the schematic block diagram of the designed front end. In order to increase the overall signal to noise ratio, a fully differential architecture is used. As illustrated in Fig. 1, the front end is consisted of a switch-opamp switch-capacitor (SO-SC) preamplifier with a gain of 40dB and a SO-SC 4^{th} order Butterworth filter. The preamplifier is designed to have a cutoff frequency of 100Hz. Hence the preamplifier also acts as a low pass filter. The passband of the filter is from 20Hz to 60Hz. In order to reduce the power consumption of the front end, switched-opamp technique is used in the design of these blocks. Besides lower power consumption, switched-opamp technique is more suitable for low voltage applications [7, 8]. We have used Filter Solutions software for designing the required Butterworth filter and obtaining the filter

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TABLE I.
SPECIFICATIONS OF THE INTRACARDIAC SIGNALS

signals	Frequency	Amplitude
Ventricular QRS signal	20-60 Hz	2-10 mV
Atrial P signal	40-80 Hz	0.1-2mV
T wave of repolarization	<7Hz	1-10mV
Disturbance signal from muscles	100-2 KHz	0.1-2mV

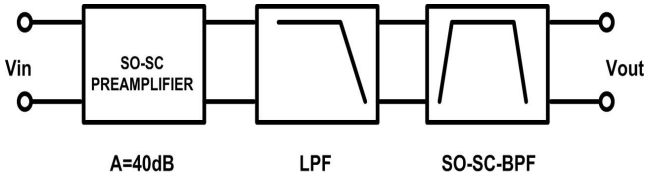

Figure 1. The implemented pacemaker analog Front-End.

coefficients. The circuit is designed to operate with a supply voltage of 0.8V. This ensures that the circuit will be able to use a single miniature battery as its power source. Particular care was taken to minimize power consumption of the circuit. This is achieved by using low voltage/ low power circuit techniques.

III. CIRCUIT DESCRIPTION

The whole signal path in the implemented circuit is differential which helps reduce the impact of noise. In this section each of the individual blocks of the front end will be discussed separately.

A. Low Power OpAmp

Since the signal path in the front end is differential, a two stage fully differential opamp is designed and used in the SO-SC preamplifier and filter blocks. Fig. 2 shows the schematic diagram of the opamp. The input stage of the opamp is realized with PMOS transistors in order to reduce the flicker noise. The opamp is to be switched on and off periodically in our design. Therefore, the second stage of the opamp is switched by two NMOS transistors M_{SW1} and M_{SW2}, which are controlled by a clock signal. We have avoided turning off the first stage of opamp to decrease its recovery time when the opamp turns on. After the clock signal becomes zero, the outputs of the opamp take 0.2ms to settle. If both first and second stages are switched then the settling time would be 0.8ms, which is too long for our design. Transistors M_3 and M_6 are connected as diodes. These diode-connected transistors (M_3, M_6) stabilize the common mode (CM) voltage of the first stage. The cross-coupled transistors (M_4, M_5) are used to increase the gain [9]. Using this technique, the first stage does not require a common mode feedback (CMFB). However, in order to stabilize the common mode voltage at the output of the opamp, the second stage needs a CMFB. Since our circuit is to operate with a supply voltage of 0.8V, the design of the CMFB for this opamp is a non-trivial task. In the pacemaker

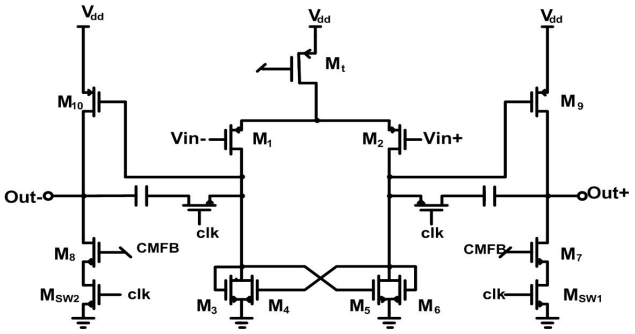

Figure 2. The schematic diagram of the proposed switched opamp.

Front-end designed by Lasanen et al [1] to avoid the problem of designing a low voltage CMFB, two single ended amplifiers are used instead of a fully differential one. Using two separate amplifiers in parallel causes the power consumption to increase. We have designed a new CMFB circuit, which is able to operate with supply voltages of as low as 0.5V.

B. The New Continuous -Time CMFB Circuit

A CMFB circuit is critical in the operation of any fully differential opamp. A new continuous time CMFB structure is used in our design, which can operate with a supply voltage of as low as 0.5V. Fig.3 shows the schematic diagram of the proposed CMFB circuit. The output of this circuit is only a function of the common mode voltage applied to its inputs and any differential voltage does not affect the output voltage. Note that the output of the opamp (out^+ and out^-) are connected to the input of the CMFB. The output of the CMFB then adjusts the bias voltage of transistors M_7 and M_8 of the opamp.

Fig. 4 shows the response of the CMFB to common mode voltages. In this figure, the common mode voltage at the input of the CMFB (the dashed line) changes from 0 to 0.8V. As can be seen, the output of the CMFB follows the input voltage relatively well for the entire voltage range. The supply voltage in this simulation is 0.8V. In order to find the supply voltage range that this CMFB circuit can operate with, the CMFB circuit is simulated with supply voltages ranging from 0V to 2V and the response of the CMFB to common mode voltage are obtained. The output of the CMFB is approximated by a second order equation; i.e. $a_2x^2+a_1x+a_0$. The coefficients of the second order polynomial are shown in Fig. 5 for different supply voltages.

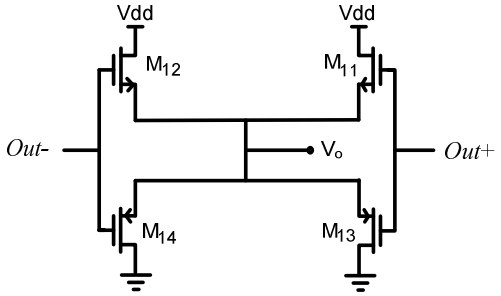

Figure 3. The low voltage continuous time CMFB circuit.

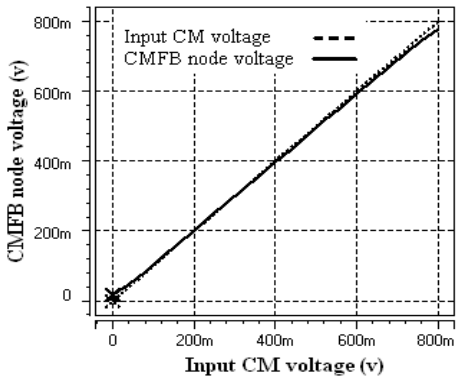

Figure 4. Output voltage of the CMFB circuit vs. its input CM voltage.

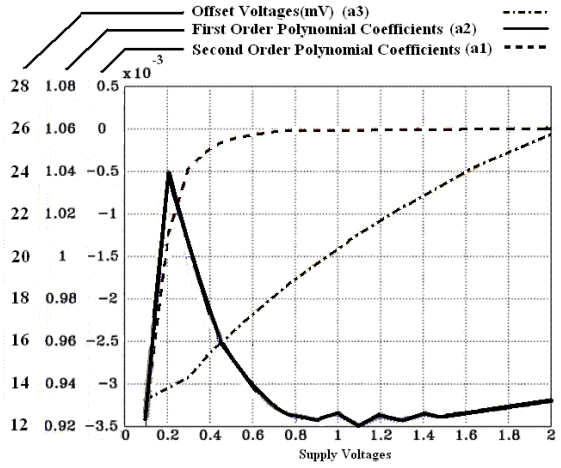

Figure 5. Polynomial coefficients of the CMFB output voltage

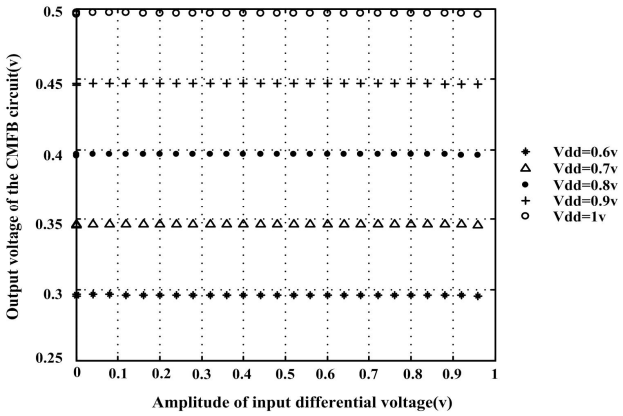

Figure 6. The CMFB response to the differential-mode signals

Ideally, a_2 should be zero and a_1 should be 1. According to Fig. 5, the absolute value of the coefficient a_2 starts to increase sharply for supply voltages below 0.4V while the coefficient a_1 is close to 1 for supply voltages above 0.1V. This means that the proposed circuit is able to operate with very low supply voltage (down to 0.1). However, its response to common mode voltage becomes non-linear for supply voltages below approximately 0.4V. The offset voltage of the output of the CMFB changes approximately 12mV when the supply voltage varies from 0.2V to 2V. This amount of offset is negligible compared to the output voltage of the circuit.

TABLE II.

PERFORMANCE PARAMETERS OF THE DESIGNED OPAMP

Property	Value
Gain	75db
Phase margin	62°
Unity gain frequency	20KHz
Average Power consumption with 50% duty cycle	50.5nW

The response of the CMFB circuit to the differential-mode signals is also of particular interest. Ideally, a CMFB should not respond to differential voltages. Fig. 6 shows the response of the proposed CMFB circuit to differential input voltages. The amplitude of the differential voltage is changes from 0V up to the supply voltage. As can be seen in this figure, the output of the CMFB circuit is relatively constant for all supply voltages.

The overall performance parameters of the opamp with the proposed CMFB are shown in Table II.

C. *The Preamplifier*

The designed front end has a preamplifier with a gain of 40dB. A SO-SC architecture is chosen for the realization of the preamplifier. This architecture is suitable for both low voltage and low power applications [1, 3, 4, 5, 6]. The schematic diagram of the preamplifier is depicted in Fig. 7.

D. *The SO-SC filter*

The 4th order Butterworth bandpass filter is realized by a SO-SC circuit. The schematic of the filter is shown in Fig. 8. The filter consists of two 2nd order bandpass blocks. The sampling frequency (f_S) is 1kHz. Reducing f_S decreases the power consumption and reduces the ratio of the maximum and minimum capacitors (C_{max}/C_{min}) in the circuit. On the other hand, increasing the sampling frequency helps increase the SNR. Therefore, we have made a compromise between SNR and power consumption in choosing f_S. The capacitor

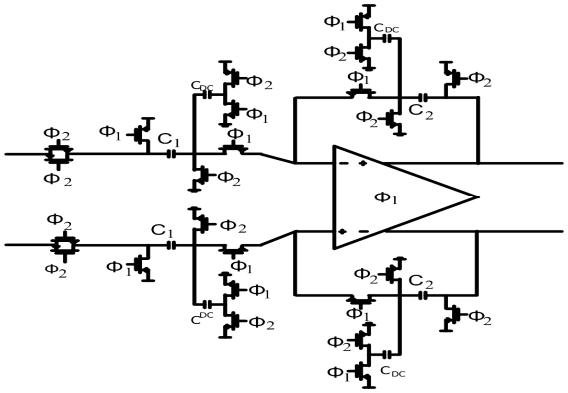

Figure 7. The schematic diagram of the preamplifier

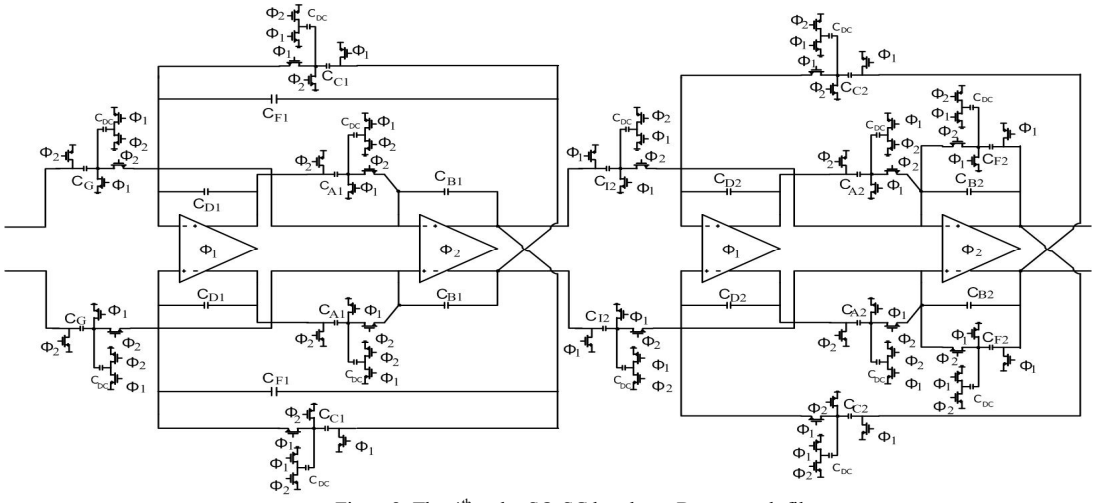

Figure8. The 4th order SO-SC bandpass Butterworth filter.

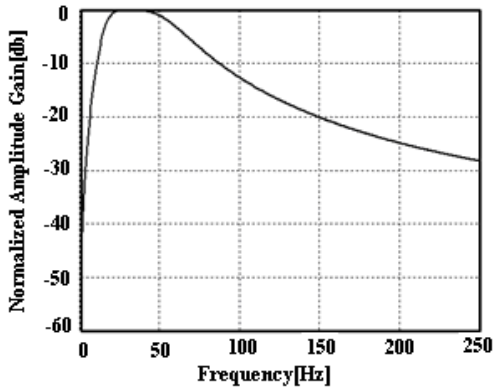

Figure 9. Frequency response of the 4th order SO-SC filter.

values for the SO-SC filter are given in Table. III and its frequency response is shown in Fig. 9.

IV. CONCLUSION

A 0.8-V analog pacemaker front-end, which includes a low power preamplifier and a 4th order SO-SC filter, is designed and simulated in 0.18µm CMOS technology. In order to reduce the power consumption, switched-opamp switched-capacitor (SO-SC) technique is used in the implementation of the circuit. A new CMFB circuit, which is suitable for very low voltage applications, is used in this circuit. The proposed CMFB has enabled us to use fully differential architecture. The overall power consumption of the circuit is approximately 420nW. The overall performance of the implemented front end is shown in Table IV.

TABLE III.
CAPACITOR SIZES FOR SO-SC FILTER

Capacitor	1st Cell	2nd Cell
A	200fF	210. 8fF
B	1.7956pF	296. 3fF
C	200fF	105. 4fF
D	897.8fF	296. 3fF
F	1. 5364pF	100fF
G	7. 5pF	-----
I	-----	400fF

TABLE IV.
PERFORMANCE PARAMETERS OF THE FRONT END

Technology	CMOS 0.18µm
Supply voltage	0.8V
Architecture	Fully differential SO-SC circuit
Bandwidth	20-60Hz
Gain	45dB
Clock frequency	1kHz
Total average current	525nA
SNDR	37.2dB

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