2004 IEEE International Workshop on Biomedical Circuits & Systems

USING DTMOS TECHNIQUE IN THE DESIGN OF COMMON MODE FEEDBACK IN A 0.8 V FOLDED CASCODE AMPLIFIER

Mohammad Maymandi-Nejad, Manoj Sachdev; Senior Member, IEEE

Electrical and computer Engineering, University of Waterloo, Waterloo, Canada
maymandi@vlsi.uwaterloo.ca, msachdev@ece.uwaterloo.ca

ABSTRACT

A continuous time common mode feedback (CMFB) technique for sub 1-V analog circuits using the bulk PMOS dynamic threshold (BP-DTMOS) technique is presented. The proposed method is used in a 0.8V folded cascode amplifier. The amplifier with embedded CMFB is implemented in 0.18 μm CMOS technology. The measurement data as well as simulation results are presented in this paper. The measurement results show that this technique improves the CMRR by 12 dB and helps reduce the common mode errors caused by process or environmental variations.

1. INTRODUCTION

The continuous trend toward smaller feature size for transistors in the CMOS technology, demands for lower supply voltages [1]. This is due to the very thin gate oxide in the advanced technologies. In addition, in many applications such as implantable biomedical devices, hearing aids [2], etc, the circuit should be operated with a miniature battery. In these applications, the volume and the weight of the battery is one of the primary concerns. Commercial, miniature batteries often provide a voltage in the range of 0.9 V to 1.5 V [3]. These issues force analog circuit designers to look for low-voltage, low-power circuit architectures. On the other hand, the supply voltage of a circuit directly affects the maximum signal swing, and therefore, the dynamic range (DR) and signal to noise ratio (SNR).

Fully differential architectures can help increase the DR and SNR of a circuit. In fully differential analog architectures, the common mode feedback (CMFB) plays an important role in bias stabilization [4, 5]. In case of sub 1-V circuits, the CMFB becomes even more critical. In an analog amplifier typically transistors are biased in the saturation region in order to provide adequate gain. However, in low voltage applications, the operating point of a transistor is not very far from the linear region. This has two consequences. First, the gain and the common mode rejection ratio (CMRR) of an amplifier are degraded. Secondly, any small perturbation from the designed values can cause the operating points of transistors to move towards the linear region. These perturbations can happen during the fabrication of the circuit or it can be due to environmental effects such as temperature variation. The effect of these perturbations and variations should be minimized by using suitable circuit techniques. Some of the fabrication variations can lead to common mode errors. Therefore, a CMFB circuit, which improves the CMRR of the amplifier, can help reduce the effects of fabrication variations.

The design of CMFB for low voltage circuits is nontrivial [6, 7]. There are several techniques to realize a CMFB circuit. These techniques can be divided into two categories, i.e. the continuous time CMFB techniques [4], and switched mode CMFB techniques [2, 8]. In this paper we will report the measurement results of a new continuous time CMFB technique which is suitable for low voltage circuits. In section 2, the proposed technique will be presented. The simulation results as well as the measurement results will be reported in sections 3 and 4 respectively. Finally, the conclusions will be drawn in section 5.

2. THE PROPOSED TECHNIQUE

Figure 1 illustrates the schematic of the proposed folded cascade amplifier with CMFB.

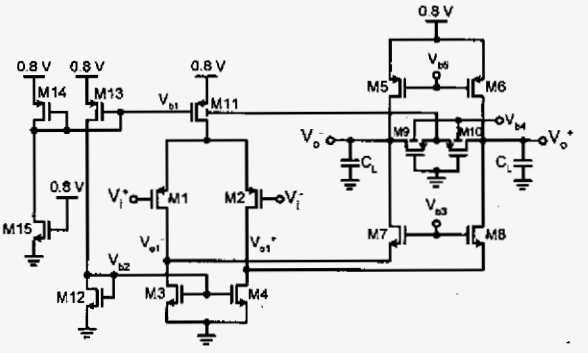


Figure 1. Schematic of the folded cascode amplifier with embedded CMFB.

The amplifier is designed to operate with a single power supply voltage of 0.8V. The input transistors (M1, M2) and the active load transistors (M3, M4) are biased in the saturation region. Therefore, it is necessary to adjust the current of the tail current source transistor M11 to twice that of the current passing through M3 or M4. Any variation in biasing voltages V_{b1} or V_{b2} causes a large voltage change at the output of the first stage (V_{o1}^+ and V_{o1}^-) and resulting in change at the output of the second stage (V_o^+ and V_o^-). Bias voltage variation

0-7803-8665-5/04/$20.00 ©2004 IEEE

changes operating points of transistors and may cause some of them to operate in the linear region which is not desirable. In order to compensate bias voltage variations often CMFB circuit techniques are used. Since the tail current transistor (M11) is a PMOS transistor it is possible to apply feedback voltage to its body to counter the biasing voltage variations. The CMFB circuit is depicted in Figure 2 separately. Two PMOS transistors (M9, M10) are employed to detect the common mode voltage. These two transistors act as two big resistors and are of the same size. The feedback voltage (V_f) is constant for differential voltages and changes only if the output common mode voltage changes. Feedback voltage (V_f) is applied to change the body voltage of the tail current source transistor M11. Bodies of M9 and M10 are not connected to V_{dd} and are biased at approximately 0.4 V. In the steady state, the source voltage of M9 and M10 is approximately 0.6 V. This forward biases the body of M9 and M10 by a voltage of approximately 0.2 V. Therefore, the threshold voltage of these transistors is reduced making them suitable for low voltage operation.

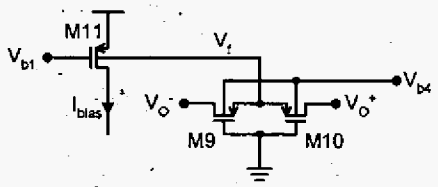


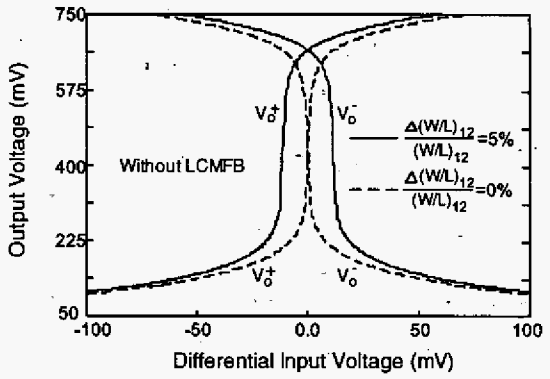
Figure 2. CMFB circuit.

Using the above mentioned circuit technique, a negative continuous common mode feedback mechanism is realized that is applied to the body of M11. This CMFB loop compensates any perturbation in V_{b1}, V_{b2} and V_{b5} by changing the body voltage of M11. Let us assume during the fabrication, the W/L ratio or the threshold voltage of transistor M12 is changed such that the biasing voltage V_{b2} is increased from its designed value. This will result in corresponding increased current in active load transistors (M3 and M4). Therefore, the output voltage of the first stage, as well as the output voltage of the second stage is lowered. These voltage variations are detected by the CMFB mechanisms and the body voltage of M11 is reduced. This, in turn, increases the tail current and causes the output voltages $\{(V_{o1}^+, V_{o1}^-)$, and $(V_o^+, V_o^-)\}$ to rise. This way the feedback compensates the perturbations of V_{b2}. Hence, the amplifier can tolerate larger parameter variations during fabrication. Furthermore, as will be seen latter, the CMFB technique also improves the CMRR of the amplifier which increases the stability of the circuit against any common mode error.

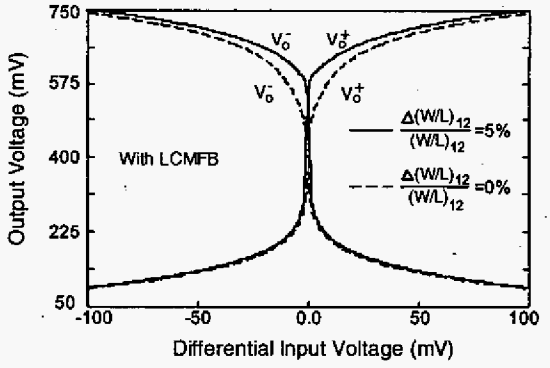
3. SIMULATION RESULTS

To verify the effectiveness of the proposed CMFB circuit against parametric variations, the circuit is simulated with and without the CMFB. The simulations are carried out for two different situations; (i) without any perturbations in biasing transistors, and (ii) with perturbations in biasing transistors.

Figure 3(a) shows the simulated dc transfer characteristic of the folded cascode amplifier without CMFB for the above cases. The dashed lines are for the ideal case (without any perturbation in W/L ratio of M12) and the solid lines are for the case of 5% perturbation in the W/L ratio of M12 which causes V_{b2} to change. Figure 3(b) shows the same simulation results for the amplifier when the CMFB is active. As can be seen, when the CMFB is active the change in the operating point is significantly less which shows the effectiveness of the proposed CMFB in reducing the impact of parametric perturbations on amplifier's performance.



(a)



(b)

Figure 3. The DC characteristic of the amplifier without (a) and with CMFB (b).

Figure 4 shows the percentage of voltage change at the output of the first stage (V_{o1}^+, V_{o1}^-) due to a change in V_{b2}. Clearly, the proposed CMFB is effective to reduce the impact of any source that causes common mode errors.

The feedback transistors of the proposed CMFB circuit should be sized such that not to load the output stage of the amplifier. The equivalent resistance of the feedback transistors M9 and M10 affects the amplifier's

differential mode and common mode gains. If the equivalent resistance of M9 and M10 is low, then it will degrade the differential gain of the amplifier. Therefore, the W/L ratio of these transistors should be as small as possible to keep the equivalent resistance as high as possible. On the other hand, if the equivalent resistance of M9 and M10 is very large, then the feedback gain will be reduced. This reduces the CMRR, and therefore, the effectiveness of the CMFB. Hence, in order to size the feedback transistors a designer should strike a compromise between the CMRR and the differential gain of the amplifier.

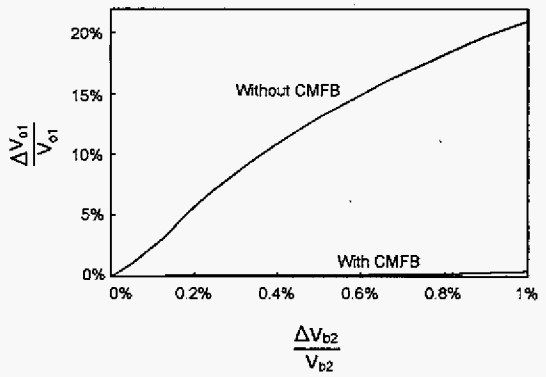


Figure 4. The percentage variation of V_{o1} versus percentage variation of V_{b2}.

Table 1 shows the simulation results of the amplifier for three different sizes of the feedback transistors. The amplifier's differential mode gain, common mode gain, and the CMRR are shown in this table. The biasing current of the amplifier is kept the same for all the three different sizes of the feedback transistor. As can be seen in this table, the differential gain of the amplifier decreases as the W/L ratio of the feedback transistors increases because by increasing the W/L ratio of M9 and M10, the equivalent resistance of these transistors decreases. This lowers the equivalent resistance between the two outputs and hence reduces the differential gain. Meanwhile, increasing the W/L ratio of M9 and M10 increases the CMRR which is due to the corresponding increase in the common mode feedback loop gain.

Stability is an important consideration in any feedback circuit. A folded cascode amplifier is inherently stable because the output node time constant is much larger than the time constant of the output of the first stage (V_{o1}^+ and V_{o1}^-). However, common mode requires additional stability consideration since there is a feedback loop. We utilized the small signal analysis to find the dominant poles of the amplifier for the common mode voltages. The dominant pole was still due to the load capacitance. However, the parasitic capacitance at the body of M11 is larger than the parasitic capacitances at the output of the first stage and contributes the second dominant pole. If the load capacitance is very small, then the second dominant pole (due to body capacitance of M11) can be noticeable and may cause instability.

Table 1. Effect of W/L of the feedback transistor on gain and CMRR of the amplifier.

M9, M10 W/L (□m)	Differential mode gain	Common mode gain	CMRR (dB) (@1 KHz)
0.25/20	394	2.0	45.89
0.6/20	390	1.6	47.46
0.95/20	370	1.4	48.45

4. MEASUREMENT RESULTS

The 0.8 V folded cascode amplifier with embedded CMFB is implemented in 0.18 μm CMOS technology. The die microphotograph is shown is Figure 5. For comparison purposes we implemented the amplifier with and without CMFB. The amplifier without CMFB occupies an area of approximately 4500 μm^2. The CMFB circuit required an additional area of approximately 10 μm by 60 μm which is 13% of the area of the amplifier. The two amplifiers are tested at room temperature with power supply voltage of 0.8 V. The load capacitance, including capacitances of the I/O pad, trace, and test equipment is estimated to be approximately 4 pf.

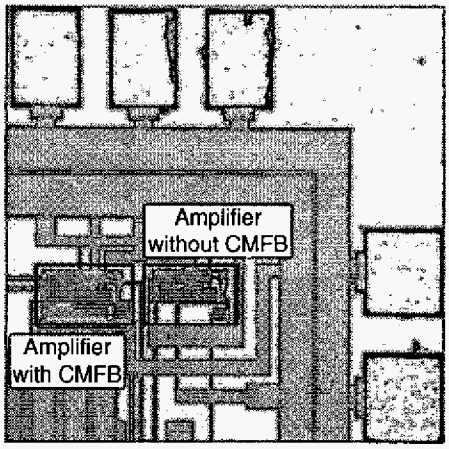


Figure 5. The die microphotograph showing part of the chip containing the two amplifiers.

Figure 6 shows the measured frequency response of the two amplifiers. As can be seen in this figure, the gain of the amplifier with CMFB is approximately 0.5 dB less than the gain of the amplifier without CMFB. This is expected since the CMFB transistors reduce the overall resistance at the output of the amplifier and consequently the differential gain decreases. The measured performance parameters of the two amplifiers as well as the post layout simulations results (for the amplifier with CMFB) are summarized in Table 2. As can be seen in this table, the implemented amplifier has an input referred offset voltage of 0.22 mV. Also, note that the

CMFB has improved the CMRR by approximately 12 dB. This shows the effectiveness of the proposed CMFB technique.

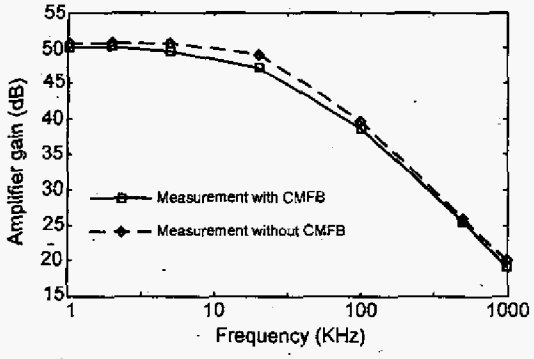


Figure 6. The frequency response of the amplifier with and without CMFB circuit.

Table 2. Performance parameters of amplifiers.

	Measurement with CMFB	Measurement without CMFB	Post layout with CMFB
DC diff. gain (dB)	50.1	50.6	52.1
Unity gain bandwidth (MHz)	9.1	10	11.2
CMRR (dB) (@ 1 KHz)	48.4	36.1	51.2
Input offset voltage	0.22 mV	0.22 mV	N/A

5. CONCLUSION

In this article, we proposed a new technique for the common mode feedback of a 0.8V folded cascode amplifier using DTMOS technique. The feedback is realized using the body of the PMOS transistors in bulk CMOS technology. This architecture is suitable for low voltage circuits. The proposed CMFB circuit improves the CMRR of the amplifier by approximately 12 dB. The design of the CMFB transistors is a compromise between differential gain and the CMRR. Compared to other CMFB techniques, the design of the proposed feedback technique is straight forward. Moreover, as long as the load capacitance is much larger than the body capacitance of the fed-back transistor (M11), the CMFB loop is stable. This condition is typically met and the CMFB stability is easily obtained.

6. REFERENCES

[1] "International Technology Roadmap for Semiconductor," *Semiconductor Industry Association*, 2001.

[2] F. Callias, F. H. Salchli, and D. Girard, "A Set of Four IC's in CMOS Technology for a Programmable Hearing Aid," *IEEE J. Solid State Circuits*, Vol. 20, pp. 301-302, April 1989.

[3] Energizer web site at "http//www.energizer.com"

[4] J. F. Duque-Carillo, "Control of Common Mode Component in CMOS Continuous Time Fully Differential Signal Processing," *Analog Integrated Circuits and Signal Processing, An International Journal, Kluwer Academic publisher*, Sept. 1993.

[5] M. Maymandi-Nejad, M. Sachdev, "Continuous time common mode Feedback Technique For Sub 1-V Analog circuits," *IEE Electronics Letters*, Vol. 38, No. 23, Nov. 2002.

[6] F. Maloberti, F. Francesoni, P. Malcovati, and O. J. A. P. Nys, "Design Considerations on Low-Voltage Low-Power Data Converters," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 42, no. 11, Nov. 1995.

[7] V. Peluso, P. Vancoreland, A. M. Marques, M. S. J. Steyaert, W. Sansen, "A 900-mV Low-Power Delta-Sigma A/D Converter with 77-dB Dynamic Range," *IEEE J. Solid State Circuits*, Vol. 33, no. 12, pp. 1887-1897, Dec. 1998.

[8] R. Castello, P. R. Gray, "A High Performance Micropower Switched Capacitor Filter," *IEEE J. Solid State Circuits*, Vol. SC-20, pp. 1122-1132, DEc. 1985.