

A 0.8V $\Delta\Sigma$ Modulator Using DTMOS Technique

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Abstract—A 0.8V second order $\Delta\Sigma$ modulator is designed in 0.18 μm bulk CMOS technology. Dynamic threshold MOSFET (DTMOS) technique is used to enhance the performance of the circuit building blocks at very low supply voltage. Schematic and post layout simulation results are provided. In case of the amplifier with the embedded CMFB, the measurement results are presented. The modulator can achieve a SNR of approximately 80dB with an oversampling ratio (OSR) of 200 and consumes a power of 460 μW .

I. INTRODUCTION

There has been a continuous trend toward smaller feature size for transistors in the CMOS technology. This trend demands for lower supply voltages [1] which are due to the very thin gate oxide in the advanced technologies. Moreover, in many applications such as implantable biomedical devices, hearing aids [2], etc, the circuit should be operated with a miniature battery. Commercial, miniature batteries often provide a voltage in the range of 0.9V to 1.5V [3]. These issues force analog circuit designers to look for low-voltage, low-power circuit architectures.

On the other hand, Analog to Digital Converters (ADC) are present in most of the applications where the IC is to interact with the physical world. In these cases the physical signal has to be converted to a digital data before any further processing. $\Delta\Sigma$ ADCs are very desirable in applications where the supply voltage is very low. This is due to the fact that $\Delta\Sigma$ modulators, which are the core of $\Delta\Sigma$ ADCs, can be implemented using switch capacitor (SC) circuit technique and SC circuits are very tolerant to non-idealities of the circuit.

In this paper a low voltage $\Delta\Sigma$ modulator is presented. The paper is organized as follows. In section II the architecture of the modulator will be presented. In section III the circuits of each block used in the modulator is discussed and the simulation and measurement results are presented. The overall performance of the $\Delta\Sigma$ modulator is discussed in section IV and, finally, conclusions are drawn in section V.

II. MODULATOR ARCHITECTURE

Figure 1 shows the architecture of the second order single loop $\Delta\Sigma$ modulator. It is basically consisted of two SC integrators and a 1-bit quantizer. The behavior of this modulator is well discussed in the literature [4] and we will not discuss it here.

Figure 2 shows the schematic of the second SC integrator that we have used in our design. It consists of an opamp, some MiM capacitors, and some MOS switches.

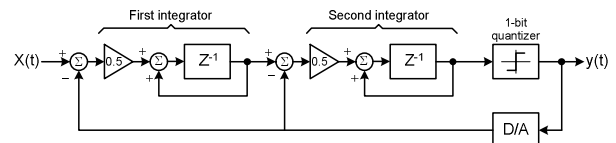


Figure 1. The architecture of the second order DS modulator.

Capacitors C_{cm} and the related switches are used to eliminate the output common mode voltage of the first integrator. The first integrator has the same architecture except it doesn't have the capacitors C_{cm} and the associated

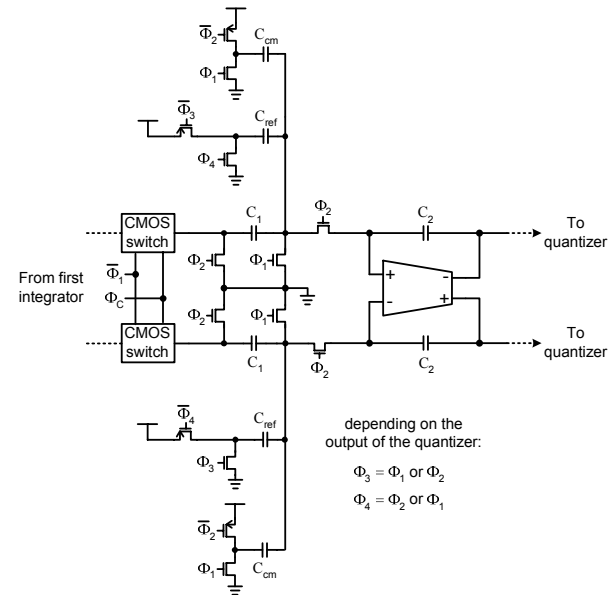


Figure 2. The second SC integrator.

switches. The CMOS switch block shown in Figure 2 is a rail to rail switch. The behavior of this switch will be explained in the next section.

III. MODULATOR BLOCKS

The modulator has two main blocks, i.e. the opamp, and the quantizer. In this section we discuss the circuit that we have designed for each of these blocks. Besides, there are some switches in the modulator. Most of these switches can

be implemented by an NMOS or PMOS transistor since the source of these transistors can be connected to either *gnd* or V_{dd} . Turning these switches on is not difficult since there is enough voltage headroom for driving the gate. However, at the output of the first integrator we need a switch which is neither connected to *gnd* nor to V_{dd} . This switch should be implemented by a CMOS gate. Turning this switch on is not very easy since the supply voltage is not large enough for rail to rail operation. There are techniques to solve this problem. The technique that we have used to overcome this problem is discussed in this section.

A. THE OPAMP

There are several parameters that should be considered in the design of the opamp in a $\Delta\Sigma$ modulator. The gain, bandwidth, and settling time of the opamp are of primary concern. When the supply voltage is large enough, it is not very difficult to meet the required opamp specifications. However, when the supply voltage is very low, designing a high gain opamp becomes a non-trivial task and the designer should be aware of the impact of each of the above mentioned parameters on the overall performance of the modulator [4].

Figure 3 shows the schematic of the opamp used in our

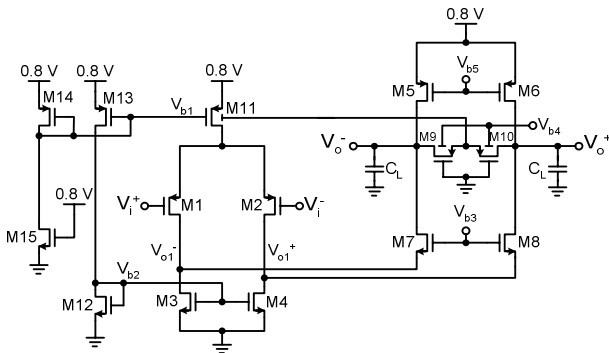


Figure 2 The schematic of the folded cascode amplifier with CMFB.

design. As can be seen the opamp is a low voltage folded cascode amplifier with a continuous time CMFB. The amplifier is designed to operate with a single power supply voltage of 0.8V. The input transistors (M1, M2) and the active load transistors (M3, M4) are biased in the saturation region. Therefore, it is necessary to adjust the current of the tail current source transistor M11 to twice that of the current passing through M3 or M4. Any variation in biasing voltages V_{b1} or V_{b2} causes a large voltage change at the output of the first stage (V_{o1}^+ and V_{o1}^-) and the second stage (V_{o2}^+ and V_{o2}^-). In order to compensate bias voltage variations often CMFB circuit techniques are used. Since the tail current transistor (M11) is a PMOS transistor it is possible to apply feedback voltage to its body to counter the biasing voltage variations. The CMFB circuit is depicted in Figure 4 separately. Two PMOS transistors (M9, M10) are employed to detect the common mode voltage. These two transistors act as two big resistors and are of the same size. The

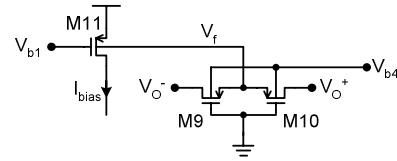


Figure 4. The CMFB circuit.

feedback voltage (V_f) is constant for differential voltages and changes only if the output common mode voltage changes. Feedback voltage (V_f) is applied to change the body voltage of the tail current source transistor M11. Bodies of M9 and M10 are biased at approximately 0. In the steady state, the source voltage of M9 and M10 is approximately 0.6V. This forward biases the body of M9 and M10 by a voltage of approximately 0.2 V. Therefore, the threshold voltage of these transistors is reduced, making them more suitable for low voltage operation.

The above amplifier is implemented in 0.18 μ m CMOS technology. In order to examine the effect of the CMFB two amplifiers, one with CMFB and one without CMFB, are fabricated in a test chip. The micrograph of part of the chip containing the two opamps is shown in Figure 5. The measured frequency response of the two opamps is shown in Figure 6. Table 1 compares the performance of the opamps obtained from measurement as well as the post layout simulations.

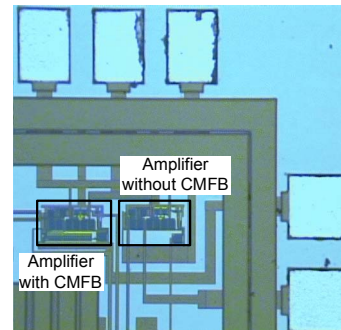


Figure 5. Die micrograph.

B. THE 1-BIT QUANTIZER

The other block in the $\Delta\Sigma$ modulator that will be discussed here is the 1-bit quantizer. We have designed a fully differential comparator with rail to rail input range to be used as 1-bit quantizer. In case of sub 1-V modulators not only the design of each block is not easy, but also the coupling of different blocks is a nontrivial task. The coupling problem rises from the fact that usually the acceptable common mode voltage at the input of the quantizer is does not overlap with that of the output of the preceding stage. For example the output common mode voltage of the folded cascode opamp is 0.4V while, depending upon the type of the input transistors used in the comparator, the input common mode voltage of the

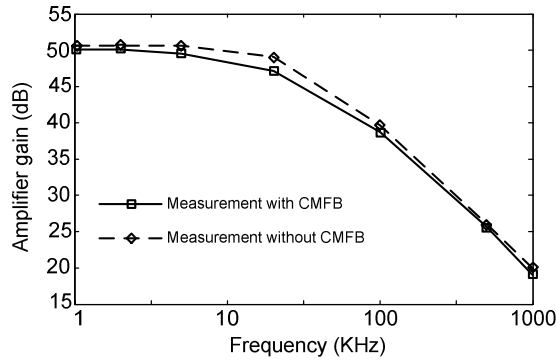


Figure 6. Frequency response of the amplifiers.

Table 1. Performance parameters of amplifiers.

	Measurement with CMFB	Measurement without CMFB	Post layout with CMFB
DC diff. gain (dB)	50.1	50.6	52.1
Unity gain bandwidth (MHz)	9.1	10	11.2
CMRR (dB) (@ 1 KHz)	48.4	36.1	51.2
Input offset voltage	0.22 mV	0.22 mv	N/A

comparator is either close to V_{dd} or gnd . In order to overcome this problem we have used the body of the PMOS input transistors of the comparator as the input.

Figure 7 shows the schematic of the quantizer. The gate terminals of the input PMOS transistors (M1 and M2) are connected to ground while the body contacts are used as the input. The comparator (quantizer) has two operational phases which are separated by the *Reset* signal. In case of a $\Delta\Sigma$ modulator the *Reset* is connected to the system clock. When the *Reset* is high, the comparator is in the tracking phase. In this phase the current through transistor M7 is divided between the two transistors M1 and M2. Depending upon the body voltage of these transistors their currents may be different. It is worth mentioning that in a track and latch comparator in the tracking phase; normally the two outputs are shorted to each other by a switch [5]. This method is not suitable for low voltage application, since it is not easy to turn on the switch that connects the two outputs. Therefore, we short the two outputs to the gnd in order to put the comparator at the metastable point. Transistors M5 and M6 are used to short the two outputs to gnd in the tracking phase. The operation of the quantizer can be explained as follows. When the *Reset* gets low (latching phase), the voltages at the two outputs start rising. After the output voltages reach a certain value (the switching threshold voltage of the comparator) the cross coupled transistors M3 and M4 form a positive feedback and, depending upon the initial currents of M1 and M2 which depends on the input

signal, one of the outputs goes to V_{dd} and the other one goes to gnd . When the two outputs reach their final values, they

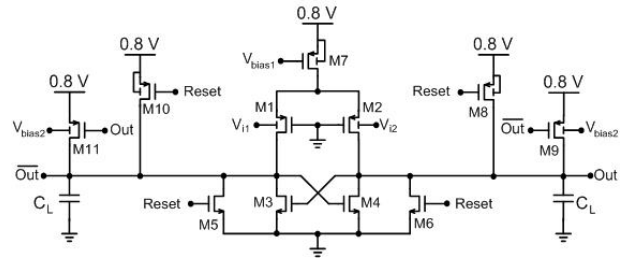


Figure 7. The schematic of the quantizer.

stay there until the *Reset* signal goes high again.

Figure 8 illustrates the transient response of the comparator with a capacitive load of 1 pF running at a frequency of 10 MHz. The transient response depicts two cases (i) $V_i=1$ mV, and (ii) $V_i=0.1$ mV. As can be seen, when the input has a larger value, the comparator response is faster. This is because the difference between the currents of M1 and M2 is larger. The larger current difference enables the quantizer to reach its switching threshold faster.

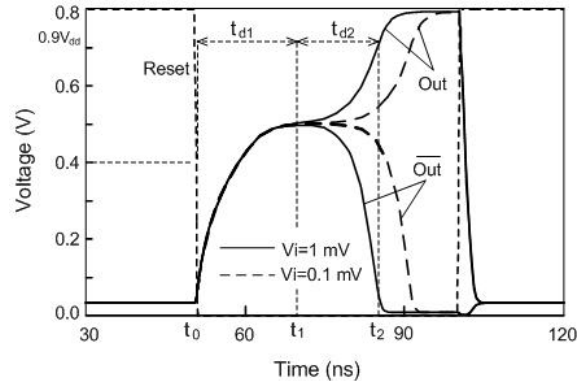


Figure 8. The transient response of the quantizer.

The delay response of the comparator in the latching phase can be divided into two time periods. In the first period, the two outputs take finite time to charge to the quantizer switching threshold (t_{d1}). During this time the positive feedback is not still triggered. The second period starts when the positive feedback is triggered and it takes time t_{d2} for the outputs to reach the final values. These two delay times (t_{d1} and t_{d2}) depend on the differential input voltage (V_i). It is clear that there is a relationship between the resolution and operation frequency. The higher the clock frequency the lower the resolution would be.

C. THE CMOS SWITCH

In the $\Delta\Sigma$ modulator there is a switch at the output of the first integrator. This switch should be able to pass rail to rail voltages. When the supply voltage is low there isn't enough

voltage headroom to drive the gate to have a rail to rail operation. To overcome this problem there are two basic approaches. One is using boot strap technique [5]. The boot strap technique is a suitable solution when there is a limitation on the maximum gate voltage. The other technique to drive CMOS switches in low voltage circuits is using a charge pump to increase the available voltage for driving the gate. This technique can be used when the technology allows the designer to use a higher voltage. In some battery operated applications, like bio-implantable circuits, the designer is limited to a certain low voltage dictated by the battery and not by the process. In these applications it is allowed to use a charge pump to generate a higher voltage to drive the gate.

Figure 9 shows the schematic of the circuit which is used for driving the switch. The main switch in this figure is implemented by the two transistors M_n and M_p . In this

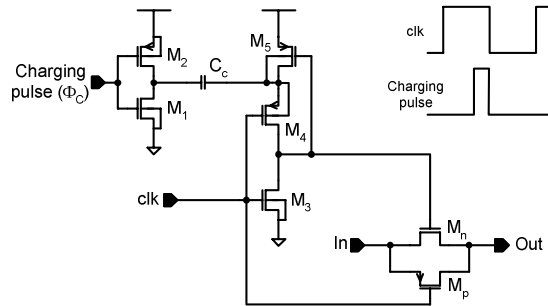


Figure 10. The in-band power spectrum of the modulator.

circuit when the clk signal is low the switch is on and vice versa. When clk signal is high, and the charging pulse is low capacitor C_C is discharged to zero. When the charging pulse rises to V_{dd} , capacitor C_C starts to charge and gains some charge before the charging pulse drops to zero. The amount of charge stored in the capacitor depends on the size of transistors M_1 and M_5 and the pulse duration. When clk becomes zero the switch is turned on and the voltage stored in the capacitor C_C is added to the V_{dd} and drives the gate of M_n . Therefore, the gate of M_5 receives a voltage higher than V_{dd} . The drawback of this technique is that transistor M_n experiences a voltage larger than V_{dd} . As mentioned earlier this is not a major issue in most battery operated circuits.

IV. THE $\Delta\Sigma$ MODULATOR

The second order single loop modulator shown in Figure 1 is designed in 0.18 μ m CMOS technology. The opamp and the quantizer discussed in the previous section are used in this modulator. The modulator's clock frequency is 8MHz and the signal bandwidth is 20kHz. This gives an oversampling ratio (OSR) of 200. The modulator is simulated with SPICE and the output bit stream is taken into Matlab to calculate the signal to noise ratio SNR. Figure 10 shows the in-band power spectrum of the modulator, obtained from post layout simulations. The SNR of the modulator is 79.1dB. The amplitude of the input signal is

80mV and its frequency is 2kHz. The power consumption of the modulator is approximately 460 μ W.

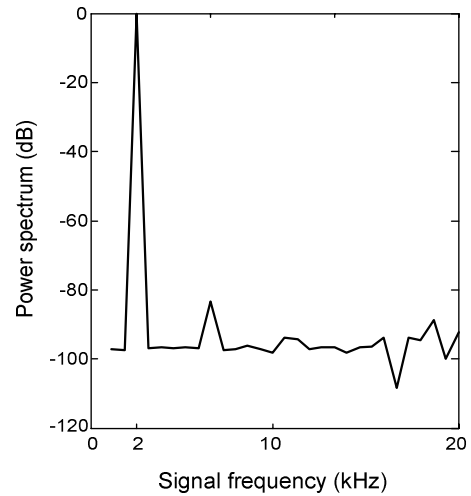


Figure 10. The in-band power spectrum of the modulator.

V. CONCLUSION

A 0.8V second order modulator is designed in 0.18 μ m CMOS technology. The post layout simulation results as well as the measurement results for the opamp are presented. DTMOS technique is used in the CMFB circuit of the opamp and the quantizer circuit. Using DTMOS technique is promising in low voltage analog circuits. The modulator achieves a SNR of approximately 80dB and consumes a power of 460 μ W at a supply voltage of 0.8V.

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