A Fully Digital ADC Using A New Delay Element With Enhanced Linearity

Hooman Farkhani and Mohammad Meymandi-Nejad
Electrical Eng. Dept., Faculty of Eng.
Ferdowsi University of Mashhad
Mashhad, Iran
E-mail: hooman_farkhani@yahoo.com, maymandi@um.ac.ir

Manoj Sachdev
Electrical and Computer Eng. Dept.
Faculty of Eng., University of Waterloo
Waterloo, Canada
E-mail: msachdev@uwaterloo.ca

Abstract— **Fully digital analog to digital converters (FD-ADC) have potential applications in very low power ICs and can be implemented in digital CMOS technology. In this paper the non-linearity of the delay element (DE), which is the main building block in an FD-ADC, is discussed and its impact on the overall performance of the ADC is addressed. It is shown that the non-linearity of the delay element should be within certain limits in order to achieve the best signal to noise plus distortion ratio (SNDR). Also, a new current starved delay element with enhanced linearity is proposed. Using the proposed DE, the SNDR of a 6-bit FD-ADC is improved by 7dB.**

I. Introduction

Rapid advances in CMOS technology have increased the performance of digital circuits [1]. This is due to smaller transistor geometry, especially thinner gate oxide, which consequently leads to lower threshold voltage. Meanwhile, due to reliability issues, the supply voltage of modern CMOS circuits has decreased. Lower supply voltages are not suitable for analog circuits due to reduced voltage headroom which leads to lower signal to noise ratio (SNR). On the other hand there are many applications where both analog and digital circuits are needed. In such cases it is preferred that the designer implement the analog circuit in the same digital CMOS technology without requiring any further processing steps. Besides, in many applications involving sensors, it is preferred to implement the entire circuit in digital domain due to increased reliability, self correcting capability, more resistance to environmental variations, and better noise performance of digital circuits [2].

An analog to digital converter (ADC) is a building block that is required in many applications, especially those having sensors. It is desirable to have fully digital ADCs since they can easily be implemented in the digital CMOS technology without requiring any special processing step. Compared to an analog ADC, a fully digital ADC (FD-ADC) is capable of operating with a lower supply voltage and potentially can be designed to have lower power consumption. Recently, researchers have proposed new architectures for FD-ADCs [2], [3]–[4]. In all these architectures delay elements play the main role in the digitization of the analog input. In fact, the amplitude variation of the input signal is converted to delay variations using delay elements and then the delay is digitized. Because the delay element is the main block in an FD-ADC, its behavior is critical in achieving good performance. Unfortunately, despite its detrimental role, the design issues of delay elements in FD-ADCs are not far fetched in the literature. In this paper we address the issue of nonlinearity in the behavior of delay elements and its impact on the performance of FD-ADCs. It will be shown that the excessive non-linearity that exists in the behavior of the current delay elements has a negative impact on the SNDR of the FD-ADC. A new DE with enhanced linearity is proposed in this paper. Using the proposed DE, the SNDR of FD-ADCs can be increased.

This paper is organized as the following. In section II we briefly review the common architecture of an FD-ADC and we discuss its shortcomings. In section III a new delay element is proposed which has a better performance in terms of linearity. In section IV the effect of the nonlinear behavior of DEs on the performance of the FD-ADC is examined. A FD-ADC is implemented using the proposed delay element and its performance is compared with existing FD-ADCs in section V. Finally conclusions are drawn in section VI.

II. The State of the Art Architecture of FD-ADCs

Watanabe et al [2] have proposed an architecture for FD-ADCs. The main building block of this architecture is a chain of delay elements (DE) forming a delay unit [5] as shown in Fig. 1-a. The rising edge of the start pulse P travels through the delay unit. As can be seen in Fig. 1-b, each of the delay elements is composed of two inverters. The input analog voltage V_{in} is used as the supply voltage of the inverters. It is well known that the delay of an inverter is a function of its supply voltage [1]. Hence the start pulse P experiences a delay, which is a function of V_{in}. Due to the delay of each DE, the rising edge of pulse P takes some time to reach the last DE and measurement of this delay can provide the digital data.

Measurement of the delay can be done in several ways. One simple technique is to use an N input latch and connect its inputs to the outputs of the DEs in the delay unit. The latch is then clocked with a reference clock pulse. By reading the outputs of the latch and using a thermometer decoder one can determine the total delay that the start pulse has experienced. Since the delay is a function of the analog input voltage, the value of V_{in} can be determined. In this way, an ADC with a resolution of $\log_2 N$ can be implemented. This technique is similar to a flash ADC, but the digitization is done based on the phase of a signal instead of its amplitude. Although, this technique is simple, the number of required DEs for an N-bit ADC is excessive.

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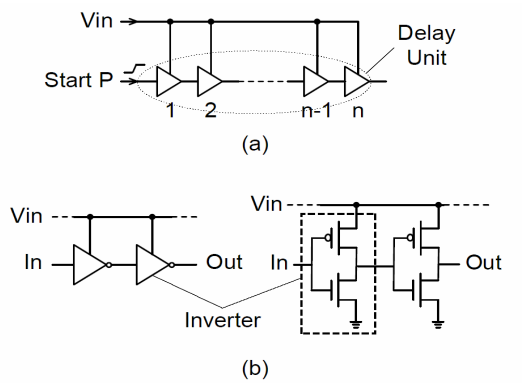

Fig. 1. a) A chain of N delay elements (DEs) forming a delay unit. b) The internal circuit of each DE.

In order to reduce the number of DEs, the architecture shown in Fig. 2 can be used [2]. In this architecture the number of delay elements is drastically reduced at the expense of a counter. As illustrated in Fig. 2, the output of the last DE is fed back to the input of the first one to form a delay loop. The counter counts the number of times that the start pulse travels through the delay loop. In the meantime the output of the DEs in the delay loop is latched. The digitized data is then obtained from the output of the two latches. In fact the latch placed at the output of the counter provides the most significant bits and the latch placed at the output of the DEs provides the least significant bits. This architecture is the basic topology for FD-ADCs [2], [3]–[4]. Despite its simplicity, this technique suffers from several drawbacks. In the following we discuss two main drawbacks of this architecture.

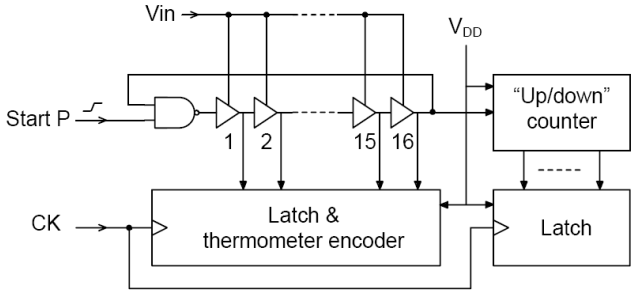

Fig. 2. The architecture of FD-ADC with reduced number of DEs

A. Non-linearity of delay elements

As mentioned above, in an FD-ADC the analog voltage is converted to delay by several DEs. Hence, the relationship between the delay and the input analog voltage plays a major role in accurate digitization of the voltage. Typically, in a delay element the relationship between delay and the controlling voltage is not linear. Fig. 3 shows the delay of the DE of Fig. 1-b versus supply voltage. As can be seen in this figure, the delay-voltage relationship is highly non-linear. This non-linearity has a negative impact on the performance of the FD-ADC. It will be shown later in this paper that the DE nonlinearity decreases the SNDR of the ADC.

Another point that is worth noting is that, according to Fig. 3, for supply voltages below approximately 0.5V the delay becomes excessively large. This is due to the fact that for supply voltages below 0.5V the transistors of the DE do not turn on. This rapid rise of delay with respect to supply voltage increases the nonlinearity of the DE and makes it not suitable for low voltage applications.

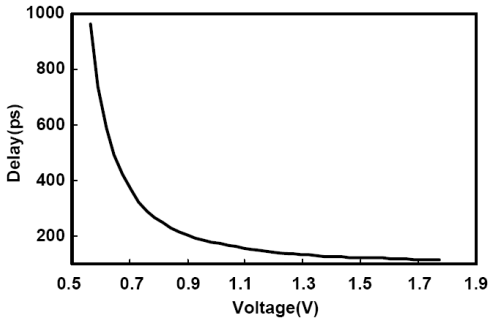

Fig. 3. Delay versus supply voltage of the delay element in Fig. 1-b.

B. Voltage variation at the output of the DE

Another drawback of the architecture shown in Fig. 2 is that the input voltage provides the supply voltage of the DEs. This has two negative consequences. First, it puts a huge load on V_{in}. The second drawback of this approach is that as the input voltage varies the voltage swing at the output of the delay elements changes. When V_{in} drops below V_{dd} the high level at the output of each of the DEs in the delay loop is no longer V_{dd} that causes two problems. First, it makes reading the output of the DEs more complicated. Secondly, it increases the leakage current in the succeeding stages connected to the output of DEs. To clarify this point, note that the output of each of the DEs in the delay loop of Fig. 2 is connected to the input of a latch. The latch can be implemented as shown in Fig. 4. The output of a DE is connected to the gate of transistors Q1 and Q5 in Fig. 4-b & c. If the output of the DE is lower than V_{dd}, transistors Q1 and Q5 will not turn off completely. This increases the leakage current of these transistors when they are supposed to be off and consequently the power consumption increases. The issue of power consumption will be revisited later in this paper.

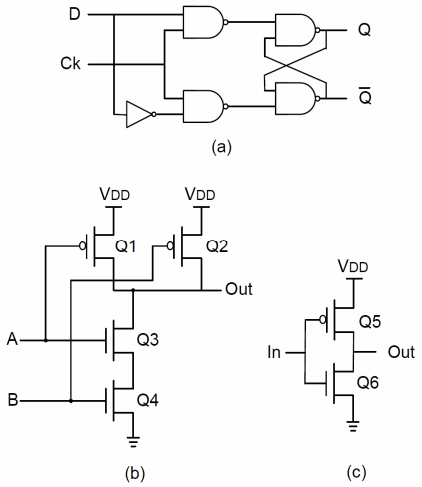

Fig. 4. (a) One stage of the latch used at output of each DE in Fig. 2, (b and c) and its internal circuitry.

III. The Proposed Delay Element

In order to solve the above-mentioned problems of the

existing circuit of FD-ADCs we propose a new delay element that provides a more linear relationship between delay and voltage. The proposed architecture is shown in Fig. 5. This delay element is composed of two inverters. The first inverter (made of Q1 and Q2) is an ordinary inverter. The second inverter (composed of Q3 to Q5) is a current starved inverter. A full discussion on current starved inverter can be found in [6]. The two inverters of the proposed DE are placed in parallel. Hence, the delay of this delay element is controlled by the delay of the two inverters. The delay of inverter 1 is fixed and the delay of inverter 2 is a function of the controlling voltage, which is V_{in} in this case. The reason for using inverter 1 with a fixed delay is to limit the maximum delay. This helps extend the linear region of the delay-voltage curve. The overall delay of the proposed delay element versus the controlling voltage is shown in Fig. 6. As shown in Fig. 6, for input voltages below 0.5V the delay becomes fixed and does not go to infinity (as opposed to that of Fig. 3). Therefore, the behavior of this delay element is more linear compared to a simple current starved inverter or the DE of Fig. 1-b. In order to extend the linear region of Fig. 6, the width (W) of transistors Q3 and Q4 should be much larger than that of Q5. This causes the on resistance of Q3 and Q4 to be much lower than Q5. In this way, the delay would become mainly a function of the current passing through Q5, and consequently a function of V_{in}.

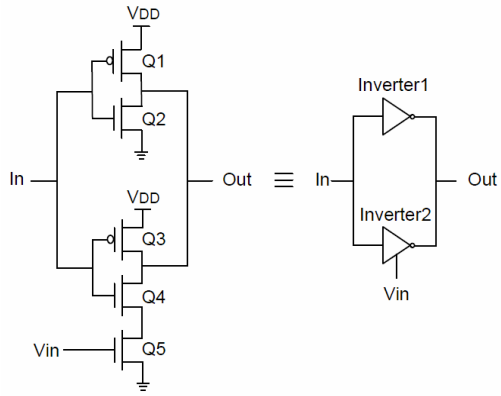

Fig. 5. The proposed delay element.

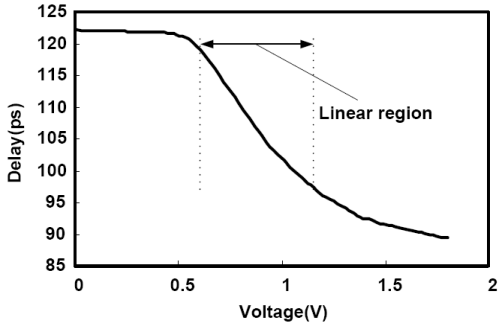

Fig. 6. The delay of the proposed delay element versus Vin.

The other advantage of the proposed DE is that the high and low levels of the output voltage are fixed and do not change with the controlling voltage. For the sake of comparison, the delay-voltage curve of the DE in Fig. 1-b and that of the proposed DE are shown in Fig. 7. The correlation coefficients (R) are obtained for the two curves in Fig. 7. In the case of DE in Fig. 1, R=0.8025 while for the case of the proposed DE R=0.9852. Clearly, the proposed DE has a superior performance in terms of linearity.

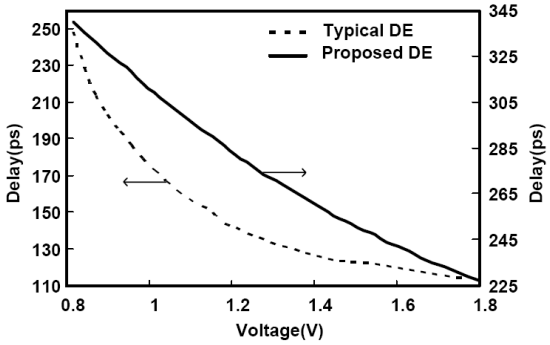

Fig. 7. The delay-voltage curve of the DE of Fig. 1-b and that of the proposed DE.

IV. Effect of Nonlinearity of the Delay Element on the Performance of FD-ADC

Since a DE is the main building block of an FD-ADC, it is critical to know what kind of relationship between the input voltage and the delay of a DE can provide the highest SNDR for an FD-ADC. Considering the architecture of Fig. 2 and assuming the pulse width of the start pulse P is T_P, then the output digital value (D_{OUT}) of the FD-ADC is obtained from the following equation in which T_D is the delay of each DE in the delay loop.

$$D_{OUT} = \frac{T_P}{T_D} \qquad (1)$$

Note that in the above equation T_D is a function of the input voltage. According to (1) in order to have a linear relationship between the input analog voltage (V_{in}) and the digital output data (D_{OUT}), T_D should be proportional to the inverse of V_{in}, i.e.:

$$T_D \propto \frac{1}{V_{in}} \qquad (2)$$

To examine the effect of nonlinearity of the DE on the performance of the FD-ADC of Fig. 2, an 6-bit FD-ADC is simulated in MATLAB with three different DEs, i.e.:

Case 1: Using the DE as the one shown in Fig. 1-b.

Case 2: Using the proposed DE (Fig. 5).

Case 3: Using a linear DE.

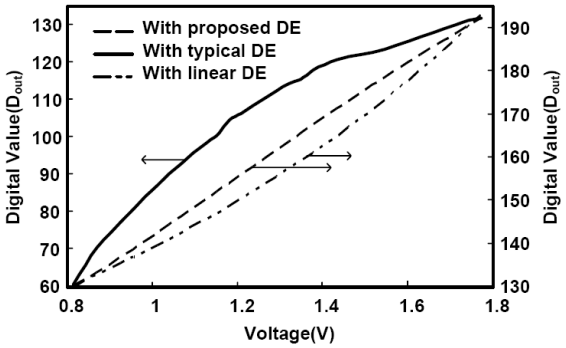

Fig. 8. D_{OUT} vs. V_{in} of the FD-ADC with three different DEs.

The output digital data (D_{OUT}) is obtained for the above three cases and the result is shown in Fig. 8. As can be seen, the best performance is obtained from the proposed DE with a delay-voltage relationship with certain amount of nonlinearity (Fig. 7). Even a DE with a linear delay-voltage relationship does not provide a linear relationship between the input analog voltage and output digital data of the FD-ADC. This fact is consistent with (2).

V. AN FD-ADC USING THE PROPOSED DE

In order to examine the impact of DE nonlinearity and to verify the results of Fig. 7, we have designed two FD-ADCs using the DE of Fig. 1-b and the proposed DE. The overall performances of the two FD-ADCs are compared in this section. The architecture of the implemented FD-ADCs is the same as Fig. 2. The number of delay elements in the delay loop is 16. The up-down counter is 4 bit and it counts on both falling and rising edges of the incoming pulse from the delay loop. The duration of the start pulse in our simulation is 44ns and the clock frequency is 20.83MHz. Both FD-ADCs are designed to provide a 6-bit digital data (6 bits is chosen to reduce the simulation time and it is possible to increase the number of bits). Fig. 9 shows the power spectrum of the two cases. As can be seen in this figure, the amplitude of the second harmonic is smaller in the case of the FD-ADC with the proposed DE. This is due to more linear behavior of the DE.

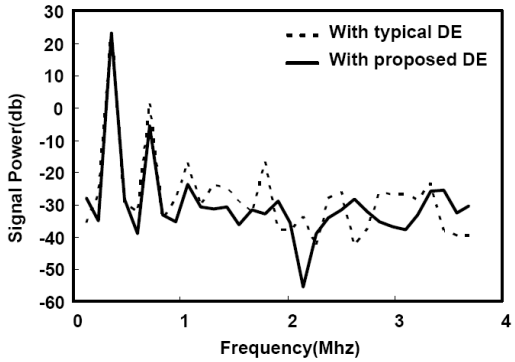

Fig. 9. The power spectrum of the 6 bit FD-ADC with DE of Fig. 1-b and with the proposed DE.

The ADC with the proposed delay element provides a SNDR of 28.38dB while the ADC with the delay element of Fig. 1-b provides a SNDR of 21.15dB. In order to calculate the SNDR we have used 64-points FFT. This enhancement of SNDR, and consequently the resolution of the ADC, is due to the fact that the behavior of the proposed DE approximates (2) more closely compared to the DE of Fig. 1-b.

In order to compare the power consumption of the FD-ADC with the proposed DE and with the DE of Fig. 1-b, the delay loop with 16 DEs and the latches at the outputs (Fig. 2) is simulated for different input voltage amplitudes and the total power consumption of the circuits with the two types of DEs are obtained. The result is illustrated in Fig. 10. As can be seen in this figure, for low input voltages the power consumption of circuit with the proposed DE is lower while for larger input voltages the circuit with the proposed DE consumes more power. This can be justified as the following. When the input voltage is lower than Vdd-|Vtp| the leakage current increases in the DE of Fig. 1-b. However, at larger input voltages the dynamic power consumption of the circuit with the proposed DE exceeds that of the circuit with DE of Fig. 1-b. Hence, depending on the input voltage range the proposed DE may have a superior performance in terms of power consumption.

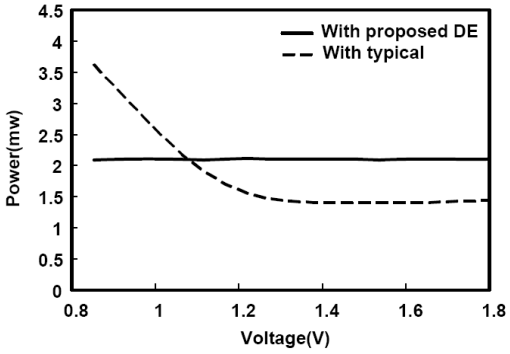

Fig. 10. The power consumption of the 16-bit delay loop with output latches for circuit with the proposed DE and the DE of Fig. 1-b at different input voltages.

VI. CONCLUSION

Fully digital analog to digital converters (FD-ADCs) have potential applications in very low voltage, low power circuits. Moreover, the implementation of such converters is fully compatible with the standard digital CMOS technology. However, the design issues of FD-ADCs are not explored in detail. Delay elements (DE) are the basic building block of FD-ADCs. Typically DEs have a highly nonlinear delay-voltage relationship. In this paper we addressed the issue of the linearity of the delay element (DE) used in the delay loop of the FD-ADC. Moreover, a new DE with an enhanced linearity is proposed. It is shown that using a DE with a delay-voltage relationship, which approximates (2) increases the SNDR and consequently the resolution of the FD-ADC. In the case of a 6-bit FD-ADC the enhanced linearity has led to more than 7dB enhancement of SNDR.

REFERENCES

[1] S. Y. Sedra and K. C. Smith, Microelectronic Circuits. Fourth Edition, Oxford University Press. Inc., 1998.

[2] T. Watanabe, T. Mizuno, and Y. Makino, "An All-Digital Analog-to-Digital Converter With 12-μV/LSB Using Moving-Average Filtering," IEEE J. of Solid-state Circuits, vol. 38, January 2003, pp. 120-125.

[3] M. A. Farahat , F. A. Farag, and H. A. Elsimary, "Only digital technology analog-to-digital converter circuit", Proceedings of the 46'Th International Midwest Symposium on Circuits and Systems, IEEE, Vol. 1, pp. 178-181, Dec. 2003.

[4] M. Keskin, "Rail-to-rail delay line for time analog-to-digital converters," U.S. Patent 7 106 239, Sep. 12, 2006.

[5] T. Watanabe, Y. Makino, Y. Ohtsuka, S. Akita, and T. Hattori, "A CMOS time-to-digital converter LSI with half-nanosecond resolution using a ring gate delay line," IEICE Trans. Electron., vol. E76-C, Dec. 1993, pp. 1774-1779.

[6] M. Maymandi-Nejad, M. Sachdev, "A digitally programmable delay element: design and analysis," IEEE transactions on very large scale integration (VLSI) systems, vol. 11, Issue 5, Oct. 2003, pp.871-878.