# Modeling and Optimization of a Solenoidal Integrated Inductor for RF ICs

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**ABSTRACT: A solenoidal structure for implementation of on-chip inductors is presented. An electromagnetic simulator is used to simulate several different-size inductors for up to 20 GHz. Additionally, artificial neural network models are developed for different inductor topologies to speed up inductors optimization process. Finally, it is demonstrated that the solenoidal inductor exhibits a better overall performance in comparison to the conventional multilayer spiral inductors demonstrating its potential for RF ICs.** © 2010 Wiley Periodicals, Inc. Int J RF and Microwave CAE 20: 182–189, 2010.

**Keywords:** on-chip inductor; artificial neural network; modeling; optimization

## I. INTRODUCTION

Implementation of integrated inductors has been a great challenge in designing RF circuits. A conventional bottleneck has been the lack of appropriate computer-aided design (CAD) tools for fast and accurate modeling of integrated inductors in RF circuits. Since on-chip inductors have a lot of parasitic effects, perfect models need to be developed for them to facilitate accurate circuit simulations. To formulate such models, several efforts have been made in the field of integrated inductors modeling. A number of circuit-level models have been proposed [1–7]. In addition, research has been carried out to improve the low quality factor of inductors [8–10].

Development of structures that implement low-area high-quality inductors can lead to an improvement in circuit performance and total chip area. Conventional methods mainly focus on spiral inductors on the most upper metal layer. This layer is used because of its high thickness and far distance from substrate. Unfortunately, inductors that are implemented with conventional methods reside in a large area, and are not thus suitable for creating over-10 nH inductors. However, lately, submicron technologies have increased the number of metal layers. In addition, the use of middle metal layers is becoming more common [11–13]. In this article, a small-area solenoidal inductor structure is introduced that exhibits a better quality factor compared to conventional topologies.

An inductor can be used as a load element or as a matching element. When the inductor acts as a load element, the goal is to maximize the multiplication of its inductance value by quality factor and self-resonant frequency (SRF), and also minimize its area. When the inductor acts as a matching element, the goal is to minimize its inductance error value as well as area, and also maximize its quality factor as well as SRF.

To achieve these optimizations, a distributed Pareto-based genetic algorithm (DPGA) is employed in this work. Since the evolutionary algorithms are computationally expensive, use of electromagnetic simulations during the optimization iterations make the process significantly demanding. To avoid this, an artificial neural network (ANN) is utilized to perform calculation of S-parameters in a speedy fashion replacing the time consuming electromagnetic simulations. The ANN is trained once, and then used during the optimization iterations. The operation speed of the ANN is much faster than that of the electromagnetic simulators.

This article is organized as follows: Section II describes the proposed inductor structure and associated parameters. Determination of optimum parameters for the proposed inductor is described in Section III. Development of the ANN models is explained in Section IV. Section V gives some sample inductors designed in our case studies with different constraints and center frequencies. Finally, the concluding remarks are given in Section VI.

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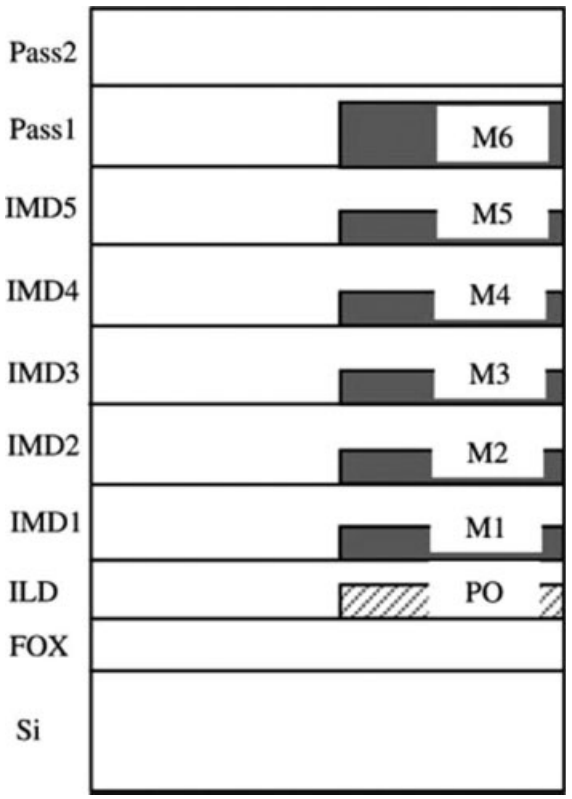


**Figure 1** TSMC 0.18 $\mu$m technology layers.

## II. PROPOSED INDUCTOR STRUCTURE

There are six metal layers available in the TSMC 0.18 $\mu$m CMOS technology. These layers are displayed in Figure 1. The thickness of the layers is given in Table I. Normally, the thickest layer, 6th layer, is employed for implementation of conventional single-layer spiral inductors. However, these inductors often reside in large areas and have low inductance values. Generally, instead of single-layer structures, multilayer spiral structures are employed when both a high inductance value and a small area are desired [11]. Although other metal layers have less thickness and it is limited the current handling and also have more series resistance and it degrade the quality factor. Figure 2a shows an example of a multilayer spiral inductor.

### *A. Structure*

A high-value small-area solenoidal inductor topology is introduced that utilizes multiple metal layers in CMOS technology. The inductor spreads over metal layers 1 to 6 and has one turn in each layer; the layers are connected in series. The proposed inductor is displayed in Figure 2(b).

Comparing the solenoidal inductor with the multilayer spiral inductor, because in this technology dielectric layers are thick enough, the proposed inductor exhibits a better performance from the viewpoints of total area, quality factor, and SRF. Although the proposed structure has a lower inductance value, yet it shows a higher quality factor over the same area. Therefore, it will be suitable for numerous applications.

**TABLE I The Thickness of Different Layers ($\mu$m)**

| Layer | FOX | ILD | IMD1–5 | Pass1 |
|---|---|---|---|---|
| Thickness | 0.35 | 0.75 | 1.38 | 2.5 |
| Layer | Pass2 | PO | M1–5 | M6 |
| Thickness | 0.75 | 0.2 | 0.53 | 2.34 |

### *B. Inductor Parameters*

In this article, we have used the following performance parameters for the inductors: inductance value, quality factor, resonant frequency and total area.

Figure 3a presents the equivalent circuit model of the inductor. However, we have considered the simplified equivalent circuit shown in Figure 3b to calculate the

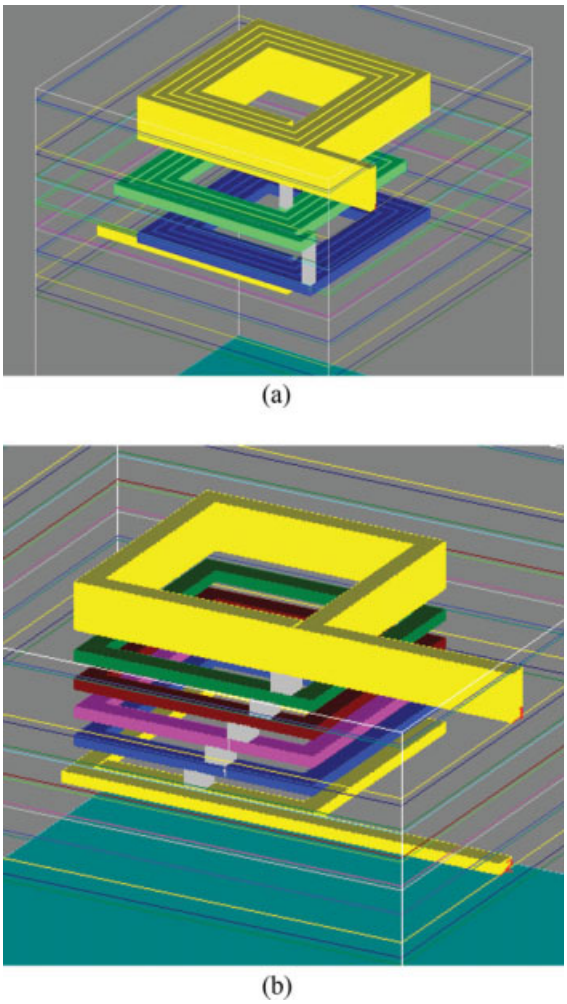


**Figure 2** (a) multilayer spiral, and (b) Solenoidal inductors. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

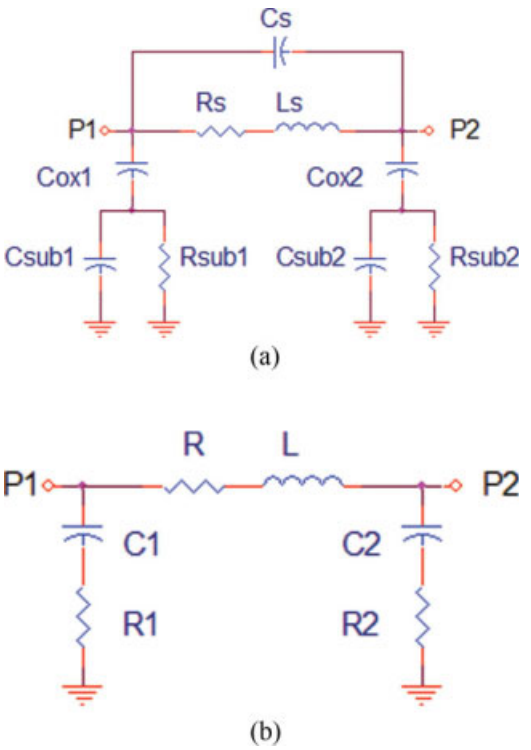


**Figure 3** (a) Equivalent circuit model of inductor. (b) Simplified equivalent circuit for calculating inductance value. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

inductance value. Therefore, the inductance value for a given frequency is determined by eq. (1) [14].

$$L = \frac{\mathrm{Im}(\frac{1}{Y_{21}})}{2\pi f} \tag{1}$$

Moreover, the quality factor can be generally expressed as:

$$Q = 2\pi . \frac{W_{\text{stored}}}{W_{\text{diss.}}}|_{\text{Per cycle}} \tag{2}$$

where $W_{\text{stored}}$ is the stored energy and $W_{\text{diss.}}$ is the dissipated energy in one operation cycle. According to eq. (2), two different expressions are derived for single-end and differential mode operations given in eqs. (3) and (4), respectively.

$$Q_s = \frac{-\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{3}$$

$$Q_d = \frac{\mathrm{Im}(Z_{\text{ind}})}{\mathrm{Re}(Z_{\text{ind}})} \tag{4}$$

Here, $Z_{\text{ind}}$ is the network two-port impedance and is calculated as follows:

$$Z_{\text{ind}} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \tag{5}$$

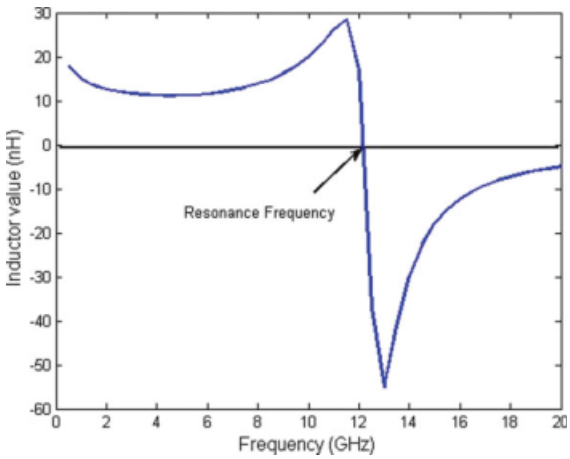


**Figure 4** The inductor value for solenoidal inductor ($W = 10$ $\mu$m, $2R = 80$ $\mu$m). [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

The SRF for an inductor can be viewed as the maximum frequency at which the inductor value is positive. When the frequency increases, the inductor value becomes negative, i.e., the inductor acts like a capacitor (see Fig. 4).

## III. DETERMINATION OF OPTIMUM PARAMETERS

If an inductor is modeled by a simple parallel RLC tank, the quality factor can be calculated as:

$$Q = \frac{R_{\text{p}}}{L\omega} \tag{6}$$

where $R_{\text{p}}$ and $L$ are equivalent parallel resistance and inductance, respectively.

Generally, an integrated inductor can be used as a load element in LNA, Mixer, and VCO circuits, or as a matching element in LNA circuits. In the former, the inductor acts like a LC-tank circuit at some specific frequencies. In this case, to maximize the gain, the equivalent parallel

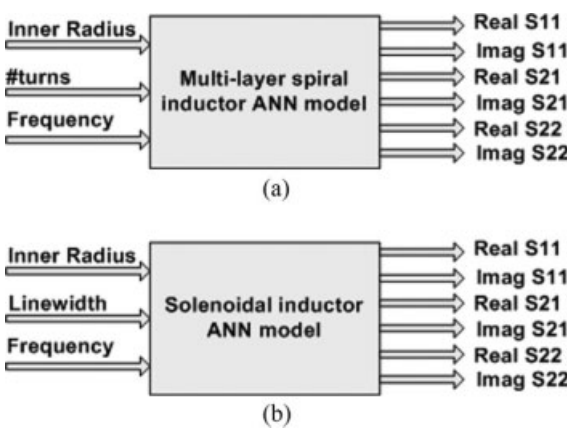


**Figure 5** (a) ANN model of multilayer spiral inductor. (b) ANN model of solenoidal inductor.

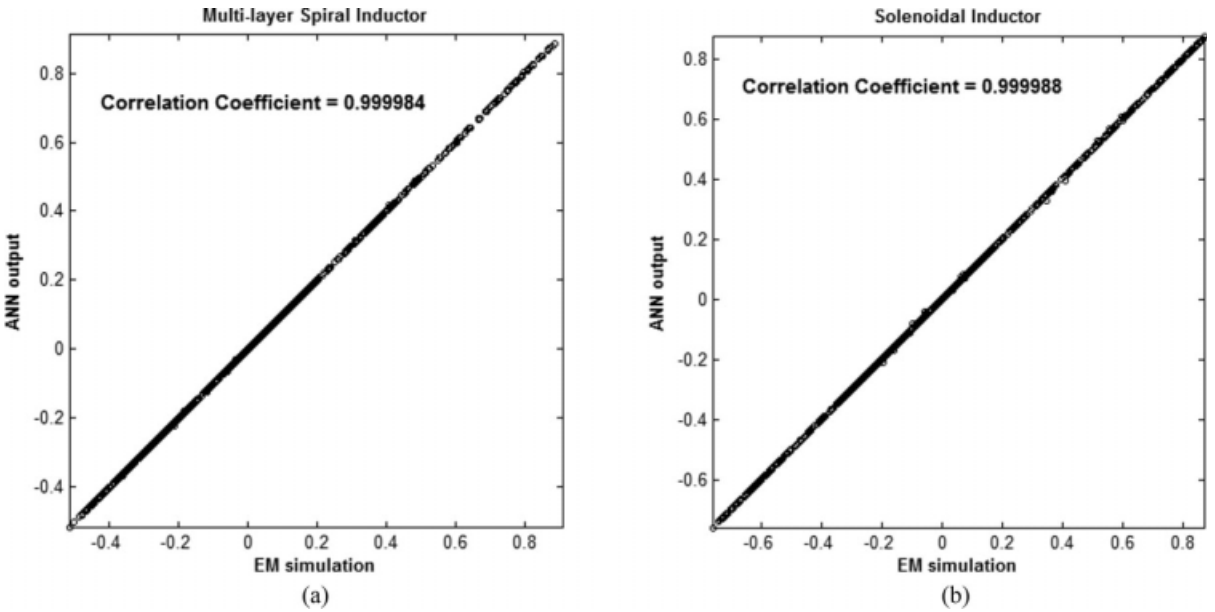


**Figure 6** Linear regression plot for: (a) multilayer spiral, and (b) solenoidal inductors, Linear regression plot for: (a) multilayer spiral, and (b) solenoidal inductors.

resistance of the inductor must be maximized. Therefore, according to eq. (6), the multiplication of inductance value and quality factor should be maximized [15]. Consequently, using both solenoidal and multilayer inductors seems to be reasonable. In the latter, on the other hand, the exact value of the inductor becomes significantly important. This value is not usually high. Thus, employing single-layer spiral inductors would be more suitable because of their high quality factor. In summary, the application of the inductor dictates the type of inductor to be used.

To determine the optimum inductor parameters through optimization, for an inductor acting as a load element, load inductor, the main goal is to maximize the multiplication of its inductance value by quality factor as well as SRF, and also minimize its area.

On the other hand, for an inductor acting as a matching element, matching inductor, the main goal is to minimize its inductance error value (Error $= L - L_{\text{desired}}$ ) as well as area, and also maximize its quality factor as well as SRF.

To achieve the described optimizations, a DPGA is employed in this work. However, since optimization algorithms are computationally expensive, the use of electromagnetic simulations during the optimization iterations makes the process significantly demanding.

To avoid this, an ANN is developed to perform the calculation of S-parameters replacing the time consuming electromagnetic simulations. The ANN is trained once, and then used during the optimization iterations. The operation speed of the ANN is much faster than that of the electromagnetic simulators.

## IV. INDUCTOR MODELING WITH THE AID OF ANN

In the context of modeling, electromagnetic simulators are computationally expensive. An alternative approach is to use equation-based models [16]. However, the drawbacks of equation-based modeling are the difficulty of the equation development for new architectures, and also possible low accuracy of the developed equations.

Investigations have focused on developing and employing ANN-based models. ANNs are capable of learning even nonlinear input-output relations. In addition, they can provide a smooth estimation even for discrete data [17]. When an ANN model is trained and its weights and biases are set, it can estimate the desired function. When the input value is applied to the trained ANN, the output will be accessible at a short time. Hence, the ANN would

**TABLE II Specifications of ANN Models**

| Total Training Time (min) | Training Epochs | Normalized Test Error | Normalized Training Error | ANN Structure | Type |
|---|---|---|---|---|---|
| 15 | 190 | 0.067% | 0.062% | 3-100-6 | Solenoidal |
| 15 | 399 | 0.048% | 0.044% | 3-100-6 | Spiral |

be significantly faster than an electromagnetic simulator. Furthermore, ANN models not only are more accurate than analytical-based models, but also are easy-to-develop for new components and technologies.

In this work, we develop two ANN models, one for the multilayer and one for the solenoidal inductors shown in Figure 2. Figure 5 shows block diagram description of the ANN models for the multilayer and the solenoidal inductors.

In RF circuit design, electrical characteristics of passive components are commonly presented in the form of S-parameters for ease of measuring. Accordingly, S-parameters are used as the output of our ANN models. Since inductors are passive two-port reciprocal networks for which S12 and S21 are equal, only S21 is included in our ANN models.

Obviously, the first step in preparation of an ANN model is a data acquisition process. In this work, the required training data is obtained through electromagnetic simulations using Sonnet-em in TSMC 0.18 $\mu$m CMOS process (see Fig. 1). Using the physical parameters of metal and dielectric layers such as thickness, electrical conductivity, and dielectric constant, standard S-parameters are extracted for the frequency of up to 20 GHz.

Two case studies were carried out. In the first case study, the multilayer inductor shown in Figure 2a was simulated. To decrease the interlayer parasitic capacitance, metal layers are used alternately, which are metal 2, 4, and 6. Several simulations were performed on different multilayer inductor samples with different number of turns, 2, 3, and 4 in each layer. Also, the inner radius ($R$) is varied between 60 and 200 $\mu$m in 20 $\mu$m steps. In this study, the line-width ($W$) and the spacing ($S$) were fixed at 10 $\mu$m and 1.5 $\mu$m, respectively. Finally, a total number of 24 simulations were executed to extract the S-parameters for up to 20 GHz. Similarly, our second case study corresponds to the solenoidal inductor shown in Figure 2b. Here, the line-width ($W$) is swept from 10 to 20 $\mu$m in 5$\mu$m steps. The variation of the inner radius ($R$) was similar to that of the first study.

Altogether, 960 training samples were obtained to develop each ANN model. The training samples were normalized to an interval $[-1, 1]$, and also, were divided to three sets titled "Train," "Validation," and "Test," using the percentages of 60%, 20% and 20%, respectively. While the network was being trained, the validation set was used to evaluate the generalization feature of the ANN model. Subsequently, the training process stopped if the validation error (the difference between a real value and athe ANN output value) was increasing. This helped to overcome the over-learning problem.

We used the Levenberg-Marquardt algorithm for training of the two ANN models that are multilayer perceptron (MLP) neural networks. Our ANN models are each composed of an input layer, a hidden layer with 100 neurons with a hyperbolic tangent as the activation function, and an output layer.

The models were tested using the test set which contained 192 patterns that were not included in the training set. To quantify the precision of the ANN models, a linear

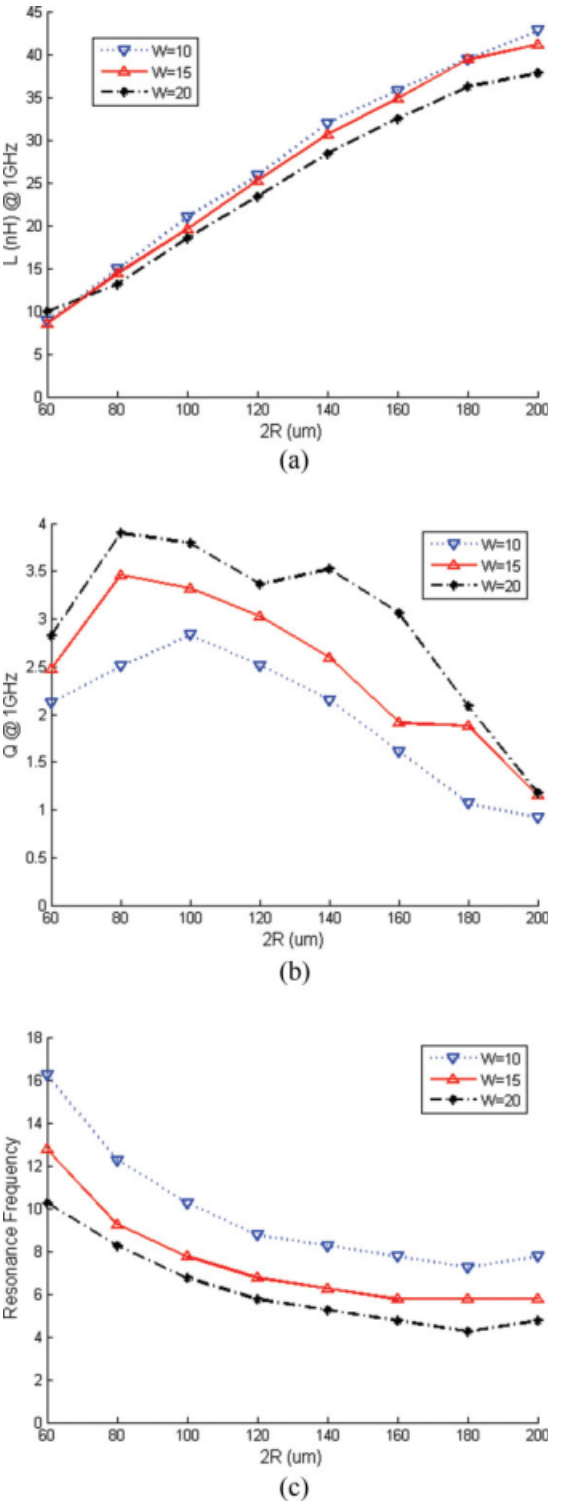


**Figure 7** Plots of performance parameters of solenoidal inductor for different line-width ($W$). (a) Inductance value. (b) Quality factor. (c) Resonant frequency. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

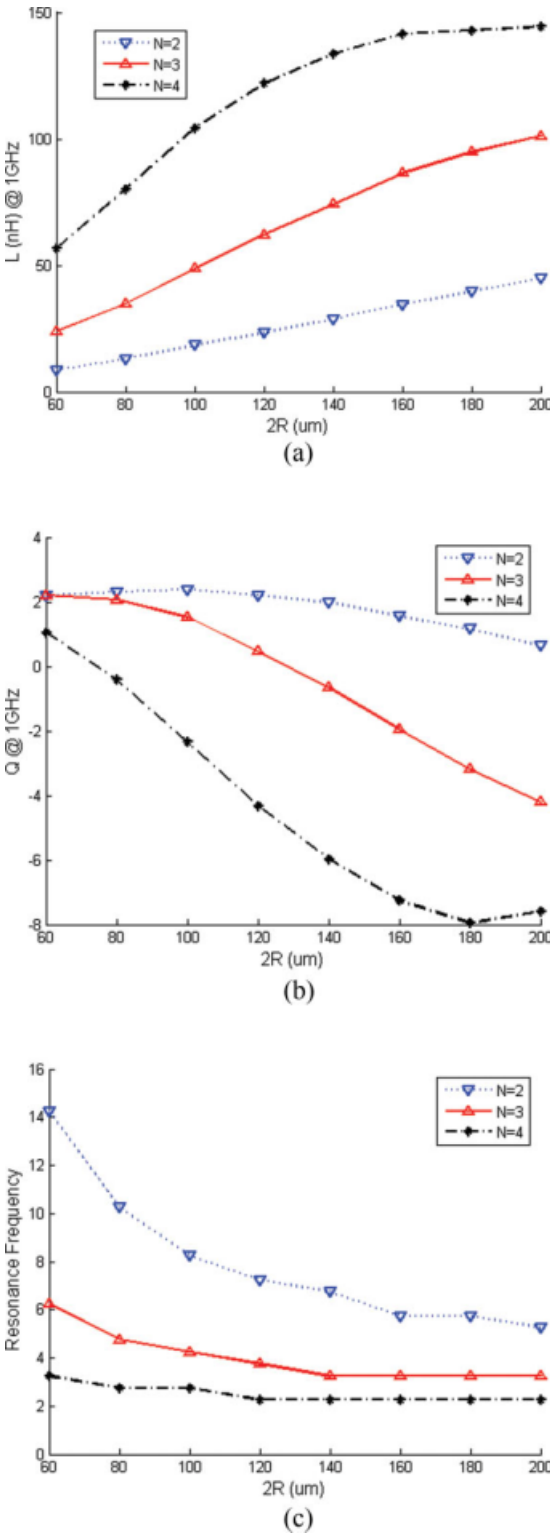


**Figure 8** Plots of performance parameters of multilayer spiral inductor for different number of turns ($N$). (a) Inductance value. (b) Quality factor. (c) Resonant frequency. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

regression between the ANN output and the EM-simulated values for the test data are plotted in Figure 6. Additionally, the normalized training and test errors of our ANN models along with other specifications are summarized in Table II.

The operation is executed on a system with a 2.66 GHz dual core processor and 2 GB of RAM.

By employing the developed ANN models, S-parameters are extracted for a desired range of frequencies, and hence, Y- and Z-parameters become obtainable. Then, the different performance parameters of the inductor can be derived using eqs. (1) and (4).

Figure 7 illustrates the plots of inductance value, quality factor and SRF, versus inductor inner radius (R) for a solenoidal inductor (case study 2).

The inductance value and the quality factor (Qd) are achieved at 1 GHz. Note that the figure is plotted for different values of line-width ($W$). According to the figure, while the inner radius ($R$) increases, the inductance value increases as well, but the SRF decreases. Similarly, when the line-width ($W$) increases, the quality factor increases due to a reduction in metal resistance. However, due to an increase in the effect of interlayer parasitic capacitors, the SRF decreases.

A similar figure (Fig. 8) is plotted for a multilayer spiral inductor (case study 1) for different number of turns in each metal layer. Considering the figure, the inductance value shows a linear dependence on inner radius ($R$). However, for high values of inner radius, the inductance value decreases due to a reduction in SRF and reaching the frequencies near 1 GHz.

A comparison between Figures 7 and 8 determines that, despite the higher inductance value of multilayer spiral inductors, solenoidal inductors demonstrate a better quality factor, SRF and total area.

## V. INDUCTOR OPTIMIZATION

The design methodology is illustrated in Figure 9. To reach an optimum solution, a synthesis tool based on genetic algorithm (GA) is used. Then, to avoid demanding EM simulations, the developed ANN models are incorporated to support the GA tool by offering estimations about the performance of real on-chip inductors.

Specifically, our multiobjective optimization tool is composed of a DPGA which offers optimum solutions of the Pareto front at the end [18]. One can select the best solutions from the final Pareto front.

In this study, DPGA design parameters are set to be the physical parameters of an inductor such as, $W$, $R$, and

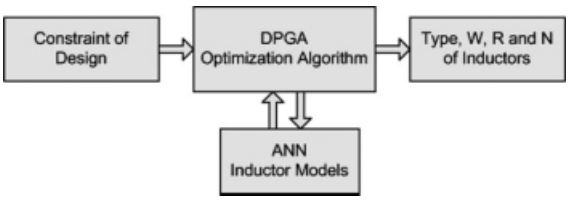


**Figure 9** Inductor design methodology.

**TABLE III Optimization Results for Different Constraints and Frequencies**

| Section | Frequency | Type | 2R ($\mu$m) | $W$ ($\mu$m) | $L$ (nH) | $Q$ | SRF (GHz) | Area (mm$^2$) | FOM |
|---|---|---|---|---|---|---|---|---|---|
| A | 2.4 GHz | Sol. | 80 | 15 | 12.2 | 2.95 | 9.25 | 0.0256 | 13,004 |
| | | | 70 | 10 | 9.77 | 3.27 | 14.25 | 0.0196 | 23,227 |
| | | Mul. | 65 | 2 | 8.55 | 2.67 | 13.25 | 0.0253 | 11,956 |
| | | | 75 | 2 | 10.65 | 2.42 | 10.75 | 0.0286 | 9687 |
| B | 1 GHz | Sol. | 80 | 10 | 15.09 | 3.44 | 9.25 | 0.0266 | 18,051 |
| | | Mul. | 76 | 2 | 15.00 | 2.38 | 9.75 | 0.0324 | 10,743 |
| | 2.4 GHz | Sol. | 93 | 15 | 14.99 | 1.98 | 8.25 | 0.0299 | 8189 |
| | | Mul. | 91 | 2 | 15.07 | 1.89 | 9.25 | 0.0342 | 7704 |
| | 5.2 GHz | Sol. | 89 | 10 | 15.06 | 3.19 | 11.25 | 0.0253 | 21,362 |
| | | Mul. | 84 | 2 | 14.97 | 1.72 | 9.75 | 0.0317 | 7919 |
| C | 1.8 GHz | Sol. | 91 | 20 | 15.83 | 3.61 | 7.25 | 0.0328 | 12,631 |
| | | Sol. | 60 | 10 | 8.42 | 3.04 | 16.25 | 0.0169 | 24,612 |
| | 2.4 GHz | Sol. | 87 | 20 | 14.03 | 2.61 | 7.75 | 0.0313 | 9067 |
| | | Sol. | 61 | 10 | 8.33 | 3.41 | 16.25 | 0.0172 | 26,836 |
| | 5.2 GHz | Sol. | 60 | 10 | 7.22 | 1.88 | 16.25 | 0.0169 | 13,052 |

$N$. The DPGA fitness function consists of inductance value, quality factor, SRF and total area.

In the following, to assess the performance of the solenoidal structure against that of the multilayer spiral structure, some synthesis samples are presented. To properly compare the results, a figure of merit (FoM) is defined as follows:

$$\mathrm{FoM} = \frac{L(nH).Q.SRF\,(\mathrm{GHz})}{\mathrm{Area}(\mathrm{mm}^2)} \tag{7}$$

In the first study, two optimization cycles are run for our two case studies at 2.4 GHz, for the load inductor.

Two of the best candidates from the final Pareto front of DPGA were selected and given in Table III, Section A. As can be observed from the table, the solenoidal structure shows a better FoM.

In the second study, matching inductors are designed for the value of 15 nH at different frequencies: 1, 2.4, and 5.2 GHz. The results are reported in Table III, Section B. Considering the table, yet, solenoidal structure is superior to the multilayer type, especially in high frequencies.

In the third study, to find out the optimum structure for load inductor, selecting the type of inductor is also applied to the optimization tool. The best solutions of DPGA are summarized in Table III, Section C. As results prove, the optimization process outcome indicates that the solenoidal architecture is the most optimum structure from different viewpoints. In other words, this structure is capable of offering a better inductance value, quality factor, and SRF over a lower area.

## VI. CONCLUSIONS

In this article, a vertical structure for implementing on-chip inductors was proposed. It was proved that this structure exhibits a more optimum performance in comparison with conventional multilayer spiral inductors. This comparison was carried out by taking advantage of evolutionary optimization.

Additionally, to speed up the optimization process and avoid EM simulations during the process, ANN models were developed for different inductor topologies which are our main contribution. Unquestionably, this modeling technique has not only played a leading role in fast modeling of the on-chip inductors. It can help design RF circuits rapidly and precisely. Specifically, when evolutionary algorithms are utilized as a core part of a synthesis tool, employing ANN models is essential to reduce the synthesis time considerably.

## REFERENCES

1. J. Lu, F. Huang, and Y. Chi, An analytical approach to parameter extraction for on-chip spiral inductors with double-π equivalent circuit, IEEE Radio Frequency Integrated Circuits (RFIC) Symp (2006), 221–224.
2. M. Kang, J. Gil, and H. Shin, A simple parameter extraction method of spiral on-chip inductors, IEEE Trans Electr Devices 52 (2005), 1976–1981.
3. J. Gil and H. Shin, A simple wide-band on-chip inductor model for silicon-based RF ICs, IEEE Trans Microwave Theory Tech 51 (2003), 2023–2028.
4. I.C.H. Lai and M. Fujishima, A new on-chip substrate-coupled inductor model implemented with scalable expressions, IEEE J Solid-State Circuits 41 (2006), 2491–2499.
5. F. Huang, J. Lu, N. Jiang, X. Zhang, W. Wu, and Y. Wang, Frequency-independent asymmetric double-π equivalent circuit for on-chip spiral inductors: Physics-based modeling and parameter extraction, IEEE J Solid-State Circuits 41 (2006), 2272–2283.
6. N. R. Das and A. Mitra, A new approach to the modeling of Si-RFIC inductor, Microwave Opt Technol Lett 48 (2006), 1095–1011.
7. H.-M. Hsu, Effective series-resistance model of spiral inductors, Microwave Opt Technol Lett 46 (2005), 107–109.
8. J. Shi, Y. Wen-Yan, and M. Jun-Fa, The enhancement of Q factor for patterned ground shield inductors at high temperatures, IEEE Trans Magn 42 (2006), 1873–1875.
9. B.-L. Ooi and D.-X. Xu, Detailed analysis of high-quality symmetrical octagonal spiral inductors on Si substrate, International Journal of RF and Microwave Computer-Aided-Engineering 15 (2005), 181–186.
10. C.-L. Chen, Effects of CMOS process fill patterns on spiral inductors, Microwave Opt Technol Lett 36 (2003), 462–465.

11. A. Zolfaghari, A. Chan, and B. Razavi, Stacked inductors and transformers in CMOS technology, IEEE J Solid-State Circuits 36 (2001), 626–628.
12. K. Yang, W.Y. Yin, J.L. Shi, K. Kang, J.F. Mao, and Y.P. Zhang, A study of on-chip stacked multi-loop spiral inductors, IEEE Trans Electron Devices 55 (2008), 3236–3245.
13. W.Y. Yin, J.Y. Xie, K. Kang, J.L. Shi, J.F. Mao, and X.W. Sun, Vertical topologies of miniature multi-spiral stacked inductors, IEEE Trans Microwave Theory Tech 56 (2008), 475–486.
14. A.M. Niknejad and R.G Meyer, Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's, IEEE J Solid-State Circuits 33 (1998), 1470–1481.
15. A. Zolfaghari, Low power CMOS design for wireless transceivers, Kluwer Academic Publications, Norwell, MA, 2003.
16. S.S. Mohan, M.M. Hershenson, S.P. Boyd, and T.H. Lee, Simple accurate expressions for planar spiral inductances, IEEE J Solid-State Circuits 34 (1999), 1419–1424.
17. S.K. Mandal, S. Sural, and A. Patra, ANN- and PSO-based synthesis of on-chip spiral inductors for RF ICs, IEEE Trans Computer-Aided Des Integrated Circuits Syst 27 (2008), 188–192.
18. A. Golmakani, K. Mafinejad, and A. Kouzani, A new method for optimization of analog integrated circuits using Pareto-based multiobjective genetic algorithm, Internatial Rev Modell Simulati (IREMOS) 2 (2009), 297–303.

## BIOGRAPHIES

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