Fourier Series in Kernel Machine

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Abstract: Kernel machine is a useful tool in Artificial Algorithm and in Pattern Analysis Field. In this paper, we propose Fourier series in kernel machine. In special case with an integral kernel, we prove that Kernel Fourier Series (KFS) is the same as conventional Fourier series. The KFS can be used as feature extractor. It produces frequency coefficient in term of time. KFS properties are presented and noise suppression is presented with selection of suitable kernel.

Keywords: Kernel machine, Fourier series, pattern recognition, artificial intelligence, noise suppression.

Automating the Design of Ultra-Low-Voltage, Low-Power Analog Integrated Circuits using Improved Non-dominated Sorting Genetic Algorithm

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Abstract: Recently, Pareto-based multi-objective optimization methods are widely used in optimizing several complex engineering problems. In this paper, we present a Non-dominated Sorting based global optimization algorithm combined with novel efficient constraint analysis to design ultra-low-voltage and low-power operational transconductance amplifiers (OTAs) for the application of LV, LP and medium speed biomedical analog to digital converters. Using highlevel simulation-based multi-objective GA, several feasible optimal designs are achieved for a circuit topology in a given technology, considering process and temperature variations. The presented approach has lead to the significant reduction of the design time (nearly, 12 times the time required for weighted sum GA approach). To illustrate the effectiveness of this approach, a 0.5-V DTMOS-based sub-threshold OTA has been designed in 0.18μm n-well CMOS process which consumes only 2.98μW power while having 95dB DC gain and 481 KHz GBW.

Keywords: Low-Voltage, Low-Power Integrated, Circuits, Computer-Aided Design, Non-dominated, Sorting Genetic Algorithm, Dynamic-Threshold MOS OTAs.

بسمه تعالی

دانشگاه یزد

گواهی ارائه مقاله

بدینوسیله گواهی می شود:

خانم سمانه بابائیان مشهدی در سومین کنگره مشترک سیستم های فازی و هوشمند ایران که در تاریخ ۲۴ تا ۲۶ تیرماه ۱۳۸۸ در دانشگاه یزد برگزار گردید شرکت کردند و مقاله خود را تحت عنوان:

Automating the Design of Ultra-Low-Voltage, Low-Power Analog Integrated Circuits Using Improved Non-dominated Sorting Genetic Algorithm

به صورت سخنرانی ارائه نمودند.

سید محمد صادق مدرس صدوق

دبیر سومین کنگره مشترک سیستم های فازی و هوشمند

Automating the Design of Ultra-Low-Voltage, Low-Power Analog Integrated Circuits using Improved Non-dominated Sorting Genetic Algorithm

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Abstract: *Recently, Pareto-based multi-objective optimization methods are widely used in optimizing several complex engineering problems. In this paper, we present a Non-dominated Sorting based global optimization algorithm combined with novel efficient Constraint analysis to design ultra-low-voltage and low-power operational Transconductance Amplifiers (OTAs) for the application of LV, LP and medium speed biomedical analog to digital converters. Using High-level simulation-based multi-objective GA, several feasible optimal designs are achieved for a circuit topology in a given technology, considering process and temperature variations. The presented approach has lead to the significant reduction of the design time (nearly, 12 times the time required for weighted sum GA approach). To illustrate the effectiveness of this approach, a 0.5-V DTMOS-based Sub-threshold OTA has been designed in 0.18µm n-well CMOS process which consumes only 2.98µW power while having 95dB DC gain and 481 KHz GBW.*

Keywords: Low-voltage, Low-power Integrated Circuits, Computer-Aided design, Non-dominated Sorting Genetic Algorithm, Dynamic-Threshold MOS OTAs

1. Introduction

Design of analog integrated circuits is a complex and tedious task especially due to the fact that many compromises should be made among different conflicting objectives. While designers can apply elaborate Computer-Aided-Design (CAD) techniques to automate digital circuitry, the absence of such aids in analog counterpart has made the analog design a bottleneck issue in the whole ASIC design [3]. Particularly, considering the advances made in fabrication technology and its trend toward nano-electronics with low-area, low-power and high speed, the complexity of the design of state-of-the-art integrated circuits has increased further, while no longer the conventional equations for the current of MOS transistors are accurate due to the short-channel effect and other second-order effects which have come to the scene by new technologies. Therefore, manual designs of RF or Ultra-Low-voltage, low-power analog circuits would involve in a process of trial and error as far as the design space in which to search for the optimal design becomes too large to be done manually which would be time-consuming and would finally lead to an ad hoc design. Hence, the role of a reliable CAD tool for circuit analysis and design is obvious, as far as it would provide us with optimal solutions which satisfy the requested performance of the system-level design, while taking the minimum design duration time (i.e., the reduction of the time-to-market of System on a chip (SOC) applications).

Up to now, much work has been done in field of circuit synthesis. In [3],[13] the performance space of circuits has been modelled. These models consider the vital functional characteristics of circuits while disregarding other details. They are faster than circuit-level simulations; however they are mostly appropriate for the system-level designs. In other works, Due to the great flexibility, acceptable accuracy and speed of GA and Hybrid GA algorithms, they have been widely used in design of many analog and mixed-signal circuits such as CMOS operational amplifiers [3], [4], Passive and active filters, and sigma-delta modulators. Nevertheless, in most of the previous

works, the variations of process and temperature hadn't been considered while all the expected aspects had been mostly combined into a single objective, each objective with a weighted coefficient relevant to the importance of that objective to the designer and finally one optimal design is presented. In contrast, Pareto-based Multi-objective algorithms are strong algorithms which have this ability to optimize several conflicting objectives independently, presenting several optimal solutions in the design space.

In this paper, we present high-level simulation-based, Pareto-based, multi-objective fast non-dominated sorting genetic algorithm (NSGA-II) combined with constraint analysis as a strong tool to design ultra-low voltage and low-power Operational Transconductance Amplifiers (OTAs) which are one of the basic building blocks in many analog applications. Several conflicting objectives such as increasing the DC gain, minimizing the power consumption, increasing the Bandwidth and minimizing the noise have been considered in optimization process.

The rest of the paper has been organized as follows, the concept of MOGA and NSGA-II is described in part 2. Part 3 discusses the optimization design procedure. The architecture of the designed OTA is presented in part 4. Simulation results are studied in part 5 and finally in part 6, conclusion is drawn.

2. Multi-objective Genetic Algorithm (MOGA)

Many engineering design optimization problems are generally composed of multiple objectives which are normally in conflict with each other and associated with constrained parameters. Therefore, optimizing the particular solution in respect to a single objective can result in unacceptable results with respect to the other objectives [2]. A reasonable solution to a multi-objective problem is to investigate a set of optimal solutions, each of which satisfies the objectives at an acceptable level without being dominated by any other solution. There are two general approaches of MOGAs, one approach is to combine all the objectives to form a single composite function such as Weighted sum method (WSGA). Each objective would have a weighted coefficient (w_k) as written in equation (1), where F_k is the k^{th} Objective of the problem and a_i is the i^{th} variable parameter.

$$f(a_i) = \sum_{k=1}^{n} w_k f_k(a_i) \quad (1)$$

$$\sum_{k=1}^{n} w_k = 1 \quad (2)$$

However, a problem of these approaches lies in the fact that mostly the appropriate selection of the weights for each objective is not simple. To overcome this problem, scaling amongst objectives is needed while small perturbations in the weights may totally result in different solutions. The second practical approaches are based on determining an entire Pareto optimal solution set, which are non-dominated to each other. While moving from one Pareto solution to another, there is always a certain amount of sacrifice in one objective(s) to achieve certain amount of gain in the other(s) [2]. Considering this property and resembling it to the circuit design where several compromises should be made, we have selected one of the most powerful elitist MOGAs, NSGA-II to be used in our CAD tool with the compatibility for the requirement of circuit design.

2.1 Modified Non-Dominated Sorting Genetic Algorithm (NSGA-II)

NSGA-II is the improved Non-dominated Sorting GA approach presented by Deb et al. in 2002 [1]. The optimization is based on the Non-domination principle and Crowding distance calculation.

The operation of NSGA-II is as follows. Note that the algorithm is going to minimize all the objectives, (for the objectives that should be maximized one shall multiply it by -1). Once the population in initialized, they are sorted based on non-dominated points principle into different fronts. The first front is the set of completely non-dominant individuals in the current population and the second front is dominated by the individuals in the first front and the other fronts are established the same way as mentioned. Equation (3) expresses the condition based on which sorting the population in different fronts is performed. In other words, we can say individual X is dominated over Y, if ever the conditions of equation (3) are satisfied.

$$\begin{cases} \forall i \in 1,2,...,k : f_i(x) \le f_i(y) \\ \exists\, j \in 1,2,....,k : f_j(x) < f_i(y) \end{cases} \quad (3)$$

Then, the individuals of each front are assigned a rank (fitness) value based on the front in which they belong to (Fig. 1.) For instance, the individuals in the first front are given a fitness value of 1; the same way will be for the other fronts. At first, the tournament selection, recombination and mutation operators are used to create a child population of size N. Then parents

and children are combined to form 2N population. Hence, elitism is ensured [1]. Then, the combined population is sorted according to non-domination. In addition, a new parameter called ***crowding distance*** is also calculated for each individual (x_i) from equation (4), where z_k is the k^{th} objective function and z_k^{min}, z_k^{max} are the minimum and maximum value of that objective in that front respectively (Fig.2). The crowding distance is a measure of how close an individual is to its neighbours. Large average crowding distance will result in better diversity in the population. Based on non-domination principle and calculating crowding distance, most optimal N population is selected to generate the next generation [1] and this cycle continues until the stopping criteria holds.

$$cd_k(x_{[i,k]}) = \frac{z_k(x_{[i+1,k]}) - z_k(x_{[i-1,k]})}{z_k^{max} - z_k^{min}}$$
$$cd(x) = \sum_k cd_k(x) \quad (4)$$

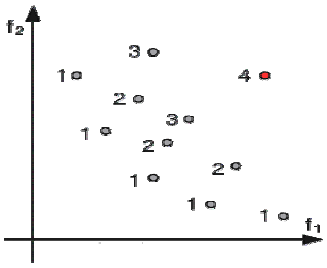

Fig. 1: The Pareto Non-dominated Fronts

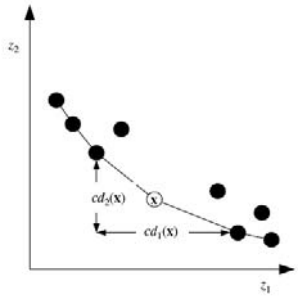

Fig. 2: Calculation of the crowding distance in each Pareto front

3. LV & LP OTA Design procedure using NSGA-II

According to the high capabilities of NSGA-II in optimizing multi-objective engineering problems, the fundamental principles of this approach has been used with a simulator-in-loop approach to design optimal LV, LP OTAs with conflicting objectives. Additional constraint analysis has been used in forming Pareto solutions to guarantee that the candidate solutions fulfill the requirements of the design in all process and temperature corners. Fig. 3 demonstrates the flow chart of the optimization process. Pareto-based Optimization scheme combined with constraint analysis has been implemented with Matlab 7.1, while the simulator for verification of objectives of OTA has been performed using HSpice with BSIM3v3 model of a standard 0.18-µm CMOS n-well process from TSMC.

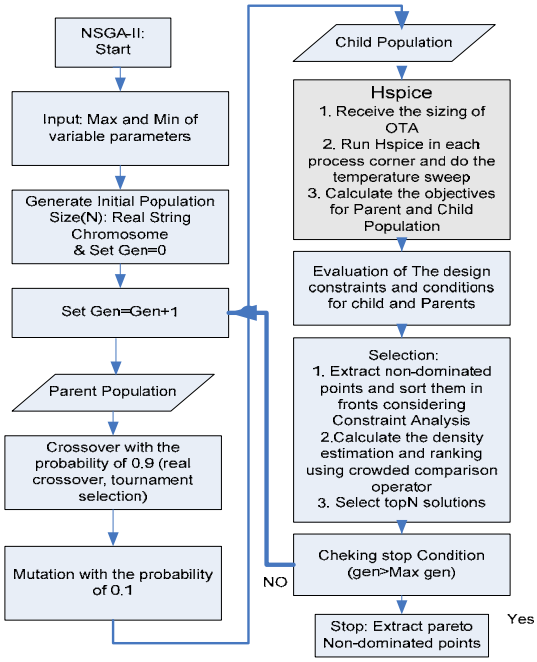

Fig. 3: The flow chart of the design Optimization of the OTA using NSGA-II

The written design tool performs as follows:

1. After selecting the appropriate topology for the design, the design parameters are determined to form the chromosome such as sizing of all transistors, independent current source and the elements of compensating scheme, etc. then the algorithm asks the user to give appropriate boundary for each parameter x ([Min value of x , Max value of x]). These boundaries actually determine the design space for the CAD tool.
2. A population of N individuals are formed, each of which is a candidate for the optimal design. This can be done randomly or initiatively according to the designer preference. This is obvious that if the first generation would be a strong one, the algorithm converges faster.
3. Each individual contains the design parameters which are entered as inputs to Hspice simulator. The design targets which are DC gain, Power consumption, UGBW, noise and THD are measured in each Process corner (TT, FF, FS, SF, SS) with temperature sweep from 0 degree to 90 degree. The results send back to the algorithm and the ***Constraint Analysis*** is done.

4. **Constraint Analysis:** We have prepared a novel analysis to form the Pareto fronts based on non-domination principle and according to the fitness of each individual in each process and temperature corner, which have been neglected in many analog CAD tools presented till now. We define some ***constraints*** for the design tool such as DC gain shouldn't have more than 15 dB variations from its nominal design in each Process and temperature corner, or at least 45 degree phasemargin should be achieved to insure stability of the design while having an acceptable speed, etc. The same constraints have been defined for each objective to teach the algorithm to choose the best optimal solutions.

5. Combining Constraint analysis and Non-domination Principle, Non-dominated designs are selected to be for the next generation. Crowding distance is also calculated to maintain the diversity of the designs and this cycle continues until the stopping criterion. Table.1 indicates the specifications of the written algorithm. Deb et al in [1] has suggested some applicable probability coefficients for mutation and crossover which has been applied to our algorithm as well.

6. Teaching the algorithm some of the *designers' experiences*: For avoiding mismatch errors in OTA, transistors with the same size have given the same width and length. Also, to avoid systematic offset voltage in design the essential relationship that should be made while determining transistor sizes are defined for the algorithm, equation 5.

Besides, a minimum value for current-source is determined to make sure that slew rate would not be degraded.

$$\frac{(w/L)_6}{(W/L)_{4a}} = 2\frac{(W/L)_7}{(w/L)_5 + 2(w/L)_9} \qquad (5)$$

7. Punishment definition: In order to guide the algorithm to select optimal designs, a penalty is defined such that if ever, one of the constraints is not satisfied, it should have less chance to participate in mating procedures, so a large value of fitness is given to that in order to be omitted from reasonable solutions, a minimal-found algorithm.

TABLE I: The specifications of NSGA-II

No. of Generation	400
Population Size	30
Selection type	Tournament
Crossover type, rate	SBX, 0.9
Mutation type, rate	Polynomial, 0.1
Stopping Criterion	No. of generation

4. The architecture of the proposed OTA

After writing a reliable optimization scheme, selecting an appropriate topology has a significant effect on final designs. In this paper, we have used Dynamic Threshold MOSFETs (DTMOS) introduced by [5], in which the bulk and gate of the OTA have been tied together, in order to dynamically change the threshold voltage, make it compatible to be used in LV and LP designs. The schematic of the proposed 0.5-V OTA is shown in Fig. 4. Input voltage has been applied to the PMOS (DTMOS) differential inputs. An average Threshold Voltage of -0.35V in PMOS DTMOS-based inputs has been achieved compared to -0.55V in regular PMOS devices in 0.18µm CMOS technology.

To provide the proposed OTA with rail-to-rail input/output swing, level-shifting approach has been used to avoid distortion in output signal while the input voltage reaches its minimum value.

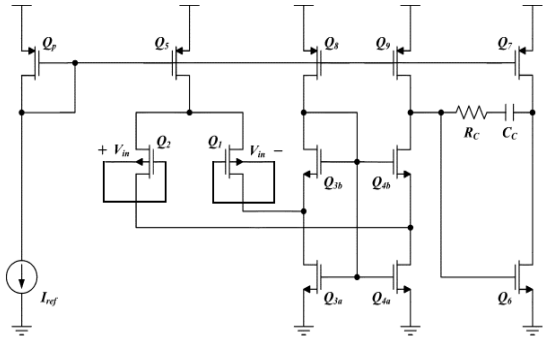

Fig. 4: The architecture of the proposed OTA

5. Simulation Results

The results of the optimization design include two phases. In the first phase, the written CAD tool is applied to the selected topology in order to determine optimal solutions for three-objective design criteria, which are increasing DC gain, increasing unity-gain bandwidth and minimizing the power consumption. 30 initial populations with 400 generations have been done. In addition, three, two-objective design problems have been performed the same way by this design tool, in order to view the results of the relationship between each two objectives. During the second phase, the specifications of one of the Pareto optimal design solutions is studied and reported in detail in part 5.2. Comparisons have been made between the designed OTA and other state-of-the-art OTAs.

5.1 NSGA-II Optimization Results

Fig. 5 illustrates the Pareto optimal solutions of a three-objective design problem among the feasible optimal design space after 400 populations. Maximum and Minimum values of current source has been given to the algorithm as Min: 100nA and Max: 1µA, in order to keep minimum power. From this figure, the great diversity among Pareto optimal non-dominated points is obvious; this is actually introduced by using the crowding comparison procedure which is used in the tournament selection and during the population reduction phase. Fig. 6 demonstrates the Pareto non-dominated solutions in different Process corners. As can be seen due to the constraint analysis, all the optimal designs are validate in all process corners satisfying the design requirements.

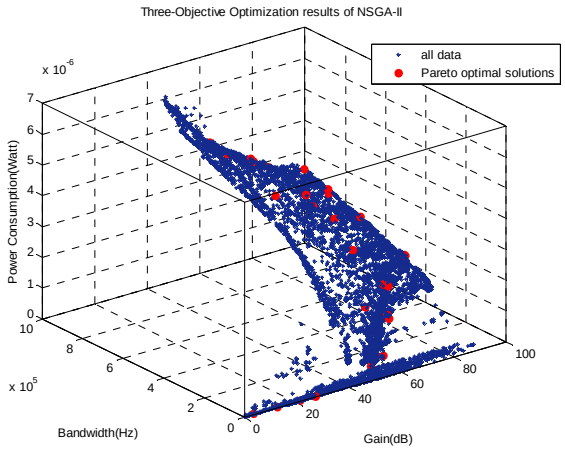

Fig. 5: Pareto optimal non-dominated solutions among other optimal design solutions in a three-objective optimization scheme @ TT corner and 25degree Temperature

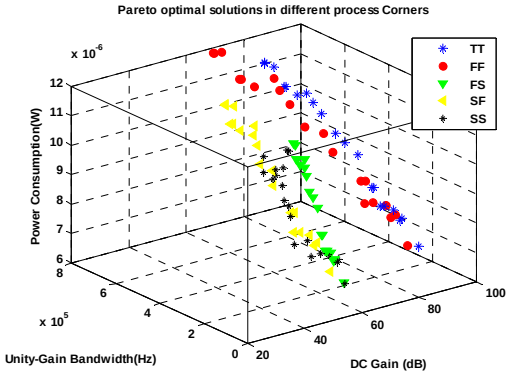

Fig. 6: Pareto optimal solutions in different Process Corners

Similar to what happens in nature; the MOGAs have this property that with the increase of the Number of generations the optimal results improve to fulfil the design aspects. This fact has been shown in Fig. 7 for 4 different generations. Fig. 8 also demonstrates the non-dominated solutions achieved in four different generations. It can be concluded that after more generations, better solutions with better fitness values can be achieved.

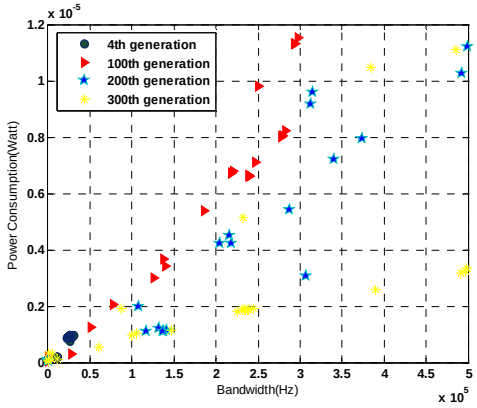

Fig. 7: Pareto optimal solutions for two-objectives of bandwidth and power consumption in different generations

One of the most interesting interpretations that one can have from obtained Pareto solutions is to understand the relationship between different objectives when the design parameters vary in the design space. For e.g. Fig. 8 indicates a direct relationship between Unity-gain bandwidth and Power Consumption. It can be concluded that the more Unity-gain Bandwidth, lead to the more power consumption. Hence, based on the design requirements, the designer can select each of the Pareto-optimal results.

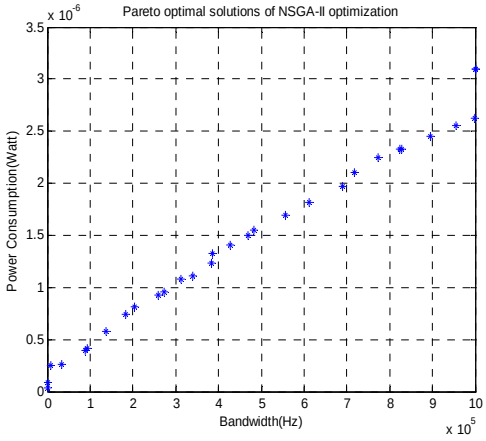

Fig. 8: Pareto optimal solutions for two-objectives of bandwidth and Power consumption in TT Process corner and nominal temperature

5.2 Hspice Simulation Results

The results of the optimization scheme lead to a set of optimal solutions. The parameter values for one of the Pareto optimal designs, is indicated in table 3. In compare with the design presented in [6] the achieved Pareto design has lead to better aspects (95.13dB gain, 481.3 kHz GBW with load capacitance of 10pF). Fig. 9 and Fig. 10 demonstrate the amplitude and phase Bode plot of the OTA output, 51 degree Phasemargin has been achieved. To have a comparison of the results achieved from our designed CAD tool with [6,5], the OTA performance benchmark indicator is illustrated in Table 2. Finally, it should be note that using high speed computers would have a profound effect on the speed of calculations while using Hybrid MOGAs would be another good alternative for future works.

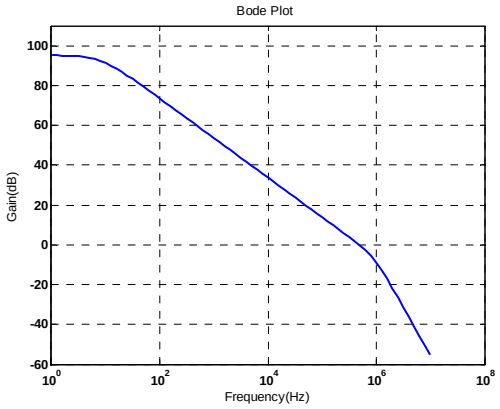

Fig. 9: The Bode plot of the gain of the OTA

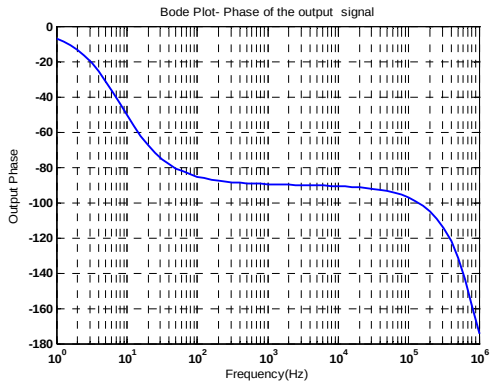

Fig. 10: The output phase of the OTA

6. Conclusions

In this paper, a fast elitist Pareto-Based non-dominated Sorting Genetic Algorithm combined with a novel Constraint Analysis has been presented in design of low voltage and low-power OTAs which are designed to satisfy the design aspects considering process and temperature variations. The results prove the effectiveness of the designed CAD tool in the applications of RF and Ultra-LV and LP analog/Mixed-signal design where the design space is too complicated to be done with the classical methods within a short time. Furthermore, the results also show that the sizing of robust analog/mixed-signal circuits can be achieved at lower computational effort than that required by traditional design methods, efficiently minimizing the time-to-market.

TABLE 2: Operational Amplifier performance Benchmark Indicator

Aspects	**This work**	**[6]**	**[5]**
CMOS Technology	0.18 µm	0.35µm	2.5 µm
Power Supply	0.5V	0.6V	0.9V
Unit gain Frequency	481.3 kHz	11.35 KHz	5.6 KHz
Open-loop gain	95.13 dB	69.4 dB	70 dB
Phasemargin	51 °	65.1 °	62 °
Signal swing	0 to 0.46	0 to 0.6	0.01 to 0.89
Slew Rate	70 V/ms	14.6 V/ms	-
CMRR @ 100Hz	67.67 dB	74.5 dB	26 dB
Power Consumption	2.98uW	550n	450nW
Input Voltage noise @ 1kHz	45.36 $nV/\sqrt{Hz}$	290 $nV/\sqrt{Hz}$	-
Offset Voltage	-	3 mV	2.6 mV

TABLE 3: The designed parameters for one of the Pareto non-dominated solutions

W1,L1	7.33E-04, 1um	W8,L8	4.00E-05,9um
W3a,L3a	5.77E-04,1um	Wp, W7,Lp,L7	2.64E-05,1um
W3b,L3b	3.30E-04,1um	C_c	2pF
W5,L5	6.65E-04,9um	R_c	73.1k
W6,L6	6.62E-04,1um	I_{ref}	130nA

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