A new low-phase noise direct-coupled CMOS LC-QVCO

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Abstract: A new LC quadrature voltage-controlled oscillator (LC-QVCO), made with direct coupling of two CMOS LC-VCOs, is presented. In the proposed circuit two identical cross-connected LC-VCOs are coupled together by directly connecting the bulk of the cross-connected transistors of one VCO to the bulk of the MOS varactors of the other VCO in such a way no extra devices are needed for coupling. Thus, no extra noise sources and power consumption are added to the core VCOs and results in high performance of QVCO. A Linear analysis of the circuit and the result of simulation in a $0.18\,\mu$m CMOS technology are presented. The same proposed coupling scheme can be used for multiphase signal generation as well. Simulation shows the proposed QVCO can operate with supply voltage as low as $0.5\,V$.

Keywords: low-noise, low-power, low-voltage, quadrature LC voltage-controlled oscillators (LC-QVCO), multiphase

Classification: Integrated circuits

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1 Introduction

Modern RF transceiver architectures increasingly require quadrature signals for modulation, demodulation and image rejection. The performances of these architectures are affected by phase noise and power consumption of their quadrature voltage-controlled oscillators (QVCO).

Some of the techniques used for quadrature signal generation are: use of RC-CR networks as delay elements, master-slave flip-flops as frequency divider and ring oscillators. These techniques suffer from poor phase accuracy, high power consumption plus speed limitation, and poor phase noise [1], respectively. Another widely used technique for quadrature signal generation is to couple two cross-connected LC-VCOs in such a way that they operate in quadrature. Due to the low phase noise and low power consumption of the LC oscillators, LC-QVCOs can satisfy the strict requirements of the modern communication systems.

In the first LC-QVCO proposed by Rofougaran [2], four extra transistors are placed in parallel with the cross-connected transistors as coupling devices. Andreani [3] proposed a modified version of the QVCO in [2], in which the coupling transistors are in series with the cross-connected transistors. This modified QVCO showed a significant phase noise improvement compared to that in [2], but the stacking of transistors in this topology limits the oscillation amplitude. Similarly the other LC-QVCOs proposed afterward by this group, used some sort of coupling elements, e.g. transistors, capacitors and transformers [6, 7, 8, 9, 10, 11], extra to the core VCOs, which leads to phase noise degradation, higher power consumption and more chip area. In this letter a low-phase noise, low-voltage and low-power LC-QVCO is presented in which no coupling elements extra to the core VCOs are used.

2 The proposed LC-QVCO

The proposed QVCO is shown in Fig. 1 (a) [4]. Each of the four cross-connected transistors M_{1-4} is placed in a separate well, as their bulks need to be connected to different potentials. It is seen in Fig. 1 (a) that no coupling devices extra to the two core LC-VCOs are used. Therefore no extra noise sources and power consumption are introduced and also, no extra chip area is consumed.

The main idea of the proposed circuit is to use the bulk of the MOS varactors, as well as the bulk of the cross-connected transistors, to couple the core VCOs. The bulk of M_{var3} and M_{var4} are connected "in-phase" to the bulk of the M_1 and M_2, and the bulk of the M_{var1} and M_{var2} are connected in an "anti-phase" manner to the bulk of M_3 and M_4, respectively. Here the gate-bulk capacitances of the MOS varactors, and the gate-bulk and the bulk-drain capacitances of the cross-connected transistors (see Fig. 1 (b)) play the role of the coupling devices between the two core VCOs and in this way, the need for any extra coupling elements is eliminated. It should be emphasized that while in strong inversion region of operation of a MOSFET the gate-bulk capacitance is negligible, it does have a much larger value when the MOSFET is off [5]. Simulation results confirm that the varactor MOSFETs M_{var1-4} operate in off region for a large portion of each cycle, wherein the gate-bulk capacitances are large enough that guarantee a strong coupling between the two core oscillators.

A linear analysis of the circuit operation is presented to show the outputs of the proposed circuit at nodes I^+ and Q^+, in Fig. 1 (a), are in quadrature. It is assumed that all the voltages have sinusoidal waveform (in a sensible
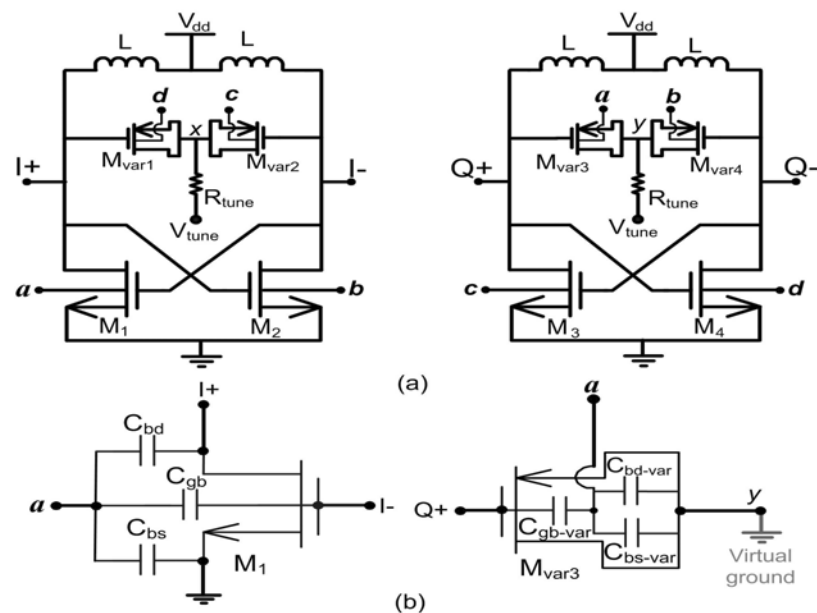

Fig. 1. Proposed LC-QVCO (a) Schematic of the proposed LC-QVCO, (b) Intrinsic capacitances of the MOS varactor and cross-connected transistors that provide coupling.

quality factor). Because of the symmetry of the circuit, the oscillation amplitude at each of the 4 output nodes I^+, I^-, Q^+ and Q^- are the same, and there is 180° phase difference between I^+ and I^-, and also between Q^+ and Q^-. The potential at nodes I^+ and Q^+ are shown in phasor form as V and $Ve^{j\varphi}$, respectively, in which φ is the phase difference between the potentials of I^+ and Q^+. By applying KCL in nodes a and c in Fig. 1 and simplifying them, equations (1) and (2) are obtained (nodes x and y are considered ac ground):

$$
\begin{aligned}
&j\omega(V_a - V)C_{bd} + j\omega(V_a + V)C_{gb} + j\omega V_a C_{bs} + \\
&j\omega V_a(C_{bd-\mathrm{var}} + C_{bs-\mathrm{var}}) + j\omega(V_a - Ve^{j\varphi})C_{gb-\mathrm{var}} = 0
\end{aligned}
\tag{1}
$$

$$
\begin{aligned}
&j\omega(V_c - Ve^{j\varphi})C_{bd} + j\omega(V_c + Ve^{j\varphi})C_{gb} + j\omega V_c C_{bs} + \\
&j\omega V_c(C_{bd-\mathrm{var}} + C_{bs-\mathrm{var}}) + j\omega(V_c + V)C_{gb-\mathrm{var}} = 0
\end{aligned}
\tag{2}
$$

where V_a and V_c are the voltages at the nodes a and c, and C_{bd}, C_{bs} and C_{gb} are intrinsic bulk-drain, bulk-source and gate-bulk capacitances of the transistors, respectively. Relations (1) and (2) can be rewritten as following:

$$
\begin{aligned}
&j\omega V_a(C_{bd} + C_{gb} + C_{bs} + C_{bd-\mathrm{var}} + C_{bs-\mathrm{var}} + C_{gb-\mathrm{var}}) = \\
&j\omega V(C_{bd} - C_{gb-} + (\cos\varphi + j\sin\varphi)C_{gb-\mathrm{var}})
\end{aligned}
\tag{3}
$$

$$
\begin{aligned}
&j\omega V_c(C_{bd} + C_{gb} + C_{bs} + C_{bd-\mathrm{var}} + C_{bs-\mathrm{var}} + C_{gb-\mathrm{var}}) = \\
&j\omega V((\cos\varphi + j\sin\varphi)(C_{bd} - C_{gb}) - C_{gb-\mathrm{var}})
\end{aligned}
\tag{4}
$$

Due to symmetry of the proposed circuit, the amplitude of the voltage at the bulk of all transistors, i.e. voltages at nodes a, b, c and d, are the same. Therefore, $|V_a| = |V_c|$, implying that the absolute value of the left side of (3) is equal to the absolute value of the left side of (4). Some further manipulations of (3) and (4) results in (5):

$$
\begin{aligned}
&\sqrt{(C_{bd} - C_{gb} + C_{gb-\mathrm{var}}\cos\varphi)^2 + (C_{gb-\mathrm{var}}\sin\varphi)^2} = \\
&\sqrt{(C_{gb-\mathrm{var}} + (C_{gb} - C_{bd})\cos\varphi)^2 + ((C_{gb} - C_{bd})\sin\varphi)^2}
\end{aligned}
\tag{5}
$$

Solving (5) to obtain φ, leads to:

$$
4((C_{bd} - C_{gb})C_{gb-\mathrm{var}})\cos\varphi = 0
\tag{6}
$$

which results in:

$$
\varphi = k\pi + \frac{\pi}{2} \quad k = 0, 1, 2, \ldots
\tag{7}
$$

meaning that outputs are in quadrature.

It should be mentioned that although the above analysis was based on sinusoidal waveforms, simulation shows that for non-sinusoidal waveforms (resulted from a low quality factor LC tank, for example) the outputs are in quadrature as well. Simulation of the circuit for a wide range of variations of the circuit parameters generated quadrature outputs, which shows that the proposed QVCO is robust.

3 Simulation results and comparisons

Here, the simulation results of the proposed QVCO are presented and compared with simulation results of some previously reported QVCOs.

The proposed QVCO was simulated in a commercial $0.18\,\mu$m CMOS technology with parameter values shown in Fig. 2 (b). Fig. 2 (a) shows the quadrature outputs of QVCO. The oscillation frequency can be varied from 4.3 to 4.7 GHz by changing the V_{tune} from 0 to 1.8 volt. The total power consumption is 9.8 mW.

The simulated phase noise of the proposed QVCO and [2] and [8] are compared in Fig. 2 (c) in which the phase noise of proposed QVCO shows an improvement of 22 dB and 5 dB, compared with the QVCOs of [2] and [8], respectively. For a more complete and fair comparison, a Figure of Merit (FoM) such as the one proposed in [8] can be used:

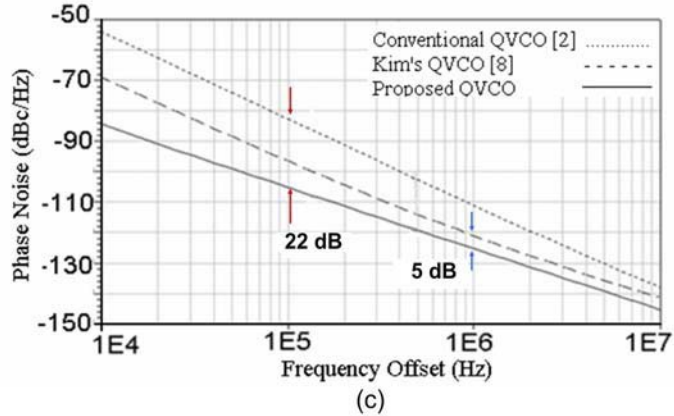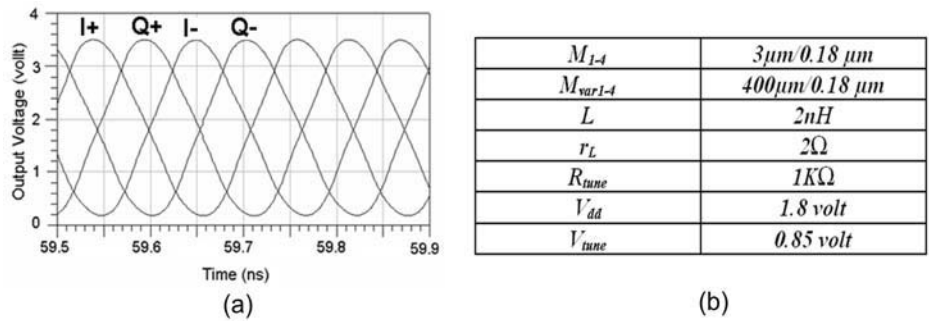$$FOM = 10\log\left(PN\left(\frac{\Delta f}{f_{osc}}\right)^2 P_{QVCO}\right) \tag{8}$$

where $PN(\Delta f)$ is the phase noise at the offset frequency Δf, f_{osc} is the centre frequency and P_{QVCO} is the total power consumption in milliwatts. Fig. 2 (d) shows FoM of some previous works and that of the proposed QVCO (note we tried to use the simulation results not measurements in comparisons).

Simulation showed that different versions of the core VCOs, i.e. with their cross-connected transistors being NMOS-only, PMOS-only or complementary, and also VCOs with or without a tail current source, all can be used to implement QVCO by utilizing the proposed coupling method. It should also be noticed that using the P-type (N-type) for both cross-connected and varactor MOSFETs, makes it possible to use a single-well technology with P-type (N-type) substrate, and use of the more expensive more complicated triple-well technology is not essential for implementation of the proposed coupling method.

As shown in Fig 1 (a), in proposed QVCO there is no stack of transistors and there is only one transistor between power supply and ground. Therefore it is compatible with low-voltage applications. Simulations show that the supply voltage can be lowered to near the threshold voltage of MOS transistors. To guarantee the correct operation of proposed QVCO in very low voltages (e.g. $V_{dd} = 0.5v$) it is necessary to choose MOS transistor, M_{1-4}, large enough to compensate the losses of resonance circuit. The proposed QVCO was redesigned and simulated with $V_{dd} = 0.5$ volt and the output voltage waveforms and phase noise have been depicted in Fig. 2 (e) and 2 (f), respectively. As shown in Fig. 2 (f), the phase noise of the QVCO is -108 dBc/Hz ($@f_{osc} = 3.9$ GHz) while the power consumption is as low as 0.9 mW.

4 Effect of back gate resistance

Parasitic elements such as back gate resistance and gate resistance can strongly influence the performance of RF ICs. The available SPICE models of CMOS, like BSIM3 and EKV, do not include parasitic components

M_{1-4}	$3\mu m/0.18\,\mu m$
M_{var1-4}	$400\mu m/0.18\,\mu m$
L	$2nH$
r_L	2Ω
R_{tune}	$1K\Omega$
V_{dd}	$1.8\ volt$
V_{tune}	$0.85\ volt$

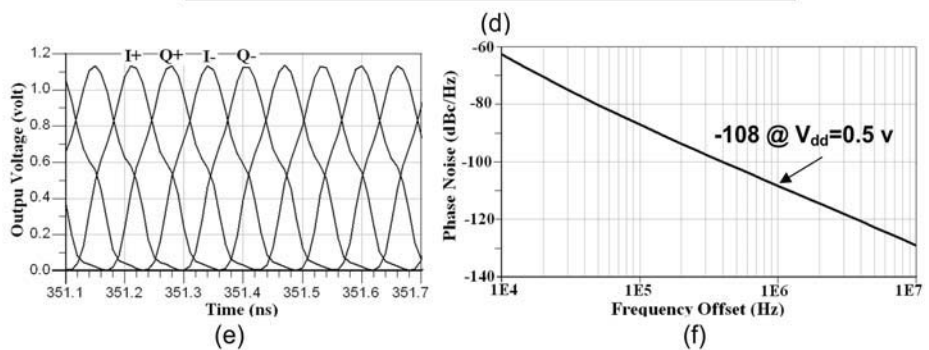| CMOS QVCO	Technology [μm]	Frequency [GHz]	Power [mW]	Phase-noise [dBc/Hz]	FOM [dBc]
[2]	1	0.9	30	-85 [@100KHz]	-149.31
[3]	0.25	1.8	20	-143 [@3MHz]	-185.5
[6]	0.35	1.8	50	-140 [@3MHz]	-178.5
[7]	0.18	6	6.8	-106 [@3MHz]	-173.24
[8]	0.18	1.1	5.4	-120 [@1MHz]	-173.5
This work	0.18	4.54	9.8	-125.3 [@1MHz]	-188.5

Fig. 2. (a) Output voltage waveforms, (b) circuit parameter values, (c) phase noise simulation results of conventional, Kim's and proposed QVCOs, (d) Figure of Merit of previous works and proposed QVCO, (e) and (f) output voltage waveforms and phase noise of proposed QVCO with power supply 0.5 volt ($V_{dd} = 0.5\,V$).

perfectly. One of the good equivalent circuits of MOSFET for RF has been proposed in [12], in which the core transistor model is the normal BSIM3v3 model without source/drain junction capacitance and gate-bulk capacitance. In this model, the aforesaid capacitances were added externally to the core transistor as well as back gate resistance and gate resistance.

To consider the effect of the back gate resistance on phase noise and power consumption in proposed QVCO, all MOS transistors are replaced with proposed equivalent circuit in [12] and simulation was done again (the value of parasitic elements can be calculated with proposed expressions in [12]). Fortunately, the simulation results didn't introduce any degradation of phase noise but the power consumption increased by less than 1 mW (i.e. the power changed from 9.8 mW to 10.6 mW).

5 Multiphase VCO using proposed coupling method

Since the proposed method requires no additional noisy and lossy elements for coupling VCOs, generalizing this method (Fig. 3 (a)) to generate multi-phase signals can reduce the phase noise, power consumption and chip area significantly.
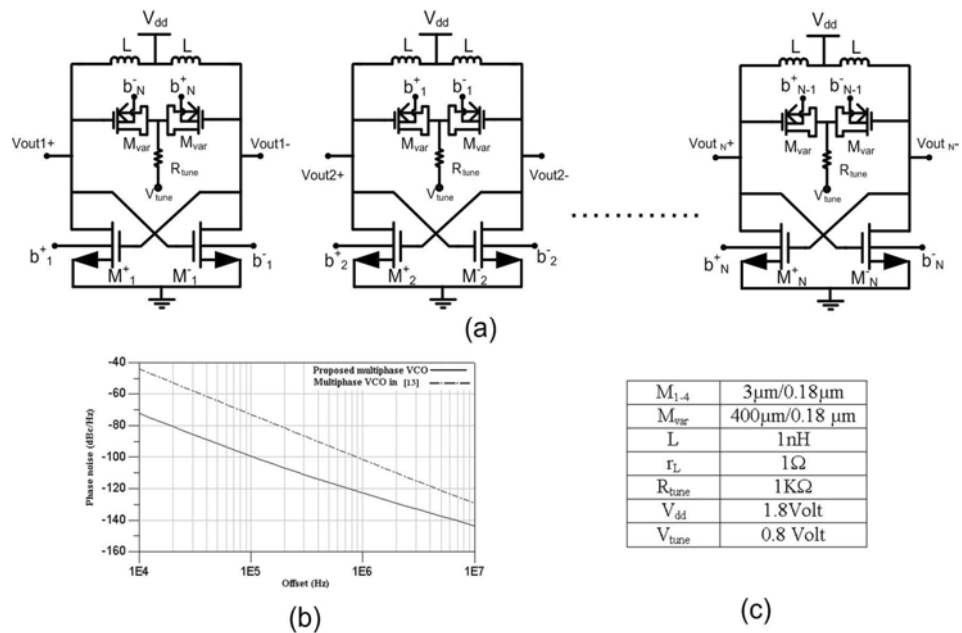

Fig. 3. (a) Schematic of proposed multiphase LC-VCO, (b) simulated phase noise of proposed multiphase VCO and [13] for 4 stages (N = 4), (c) circuit parameter values.

Simulation showed that the same coupling method can also be used to generate multiphase signals by generalizing the "in-phase anti-phase" scheme of connection to several identical core VCOs [13]. In a case study a multiphase VCO with four (N = 4) stages was designed and simulated with circuit parameters in Fig. 3 (c). The phase noise of proposed circuit and that of [13]

was depicted in Fig. 3 (b) in which a good improvement can be observed.

It is noticeable that the QVCOs and multiphase VCOs that utilize the proposed method can operate with voltage supply as low as 0.5 volt. So it can be used for very low voltage applications.

6   Conclusion

In this letter a new method of coupling of identical CMOS LC-VCOs for generating quadrature and multiphase signals was proposed in which VCOs were directly connected to each other via the bulk of the cross-connected transistors and MOS varactors. Therefore, no extra elements were needed for coupling, which led to a better phase noise and lower power consumption. The coupling elements in this method are the intrinsic capacitances of the MOS varactor and the cross-connected transistors. A comparison of the performance of the proposed circuit with those of some previously reported QVCOs was presented. The same coupling scheme can be used for multiphase signal generation as well. Simulation showed that this QVCO can operate with supply voltage as low as 0.5 V.