High Gain CMOS UWB LNA Employing Thermal Noise Cancellation

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Abstract—**This paper presents a 3.1-10.6 GHz CMOS LNA designed with a 0.18 µm CMOS technology. In this amplifier, cancellation of two important noise sources in the amplifier, plus increasing effective transconductance of the input stage, reduce the noise figure (NF) of the amplifier. Noise canceling LNAs suffer from relatively low power gain. In contrast, this paper presents an ultra-wideband LNA with higher gain which also has better noise figure and lower power consumption achieved by utilizing gm-boosting technique and a modified form of noise-canceling technique. Also, bridged-shunt-series and asymmetric T-coil peaking techniques are employed to extend the bandwidth of the amplifier. The optimum values of all elements are determined using genetic algorithms. The proposed LNA achieves 17.5±1 dB power gain and 2.25 dB average noise figure in the frequency range of 3.1-10.6 GHz, with 10.6 mW power drawn from a 1.8 V supply. Within the target band, input and output return losses are respectively less than -17 dB and -12 dB.**

Keywords- **Low noise amplifier (LNA), ultra wideband (UWB), noise-canceling, gm-boosting, asymmetric T-coil peaking, bridged-shunt-series peaking, genetic algorithm.**

I. INTRODUCTION

In the recent years, ultra wideband (UWB) systems have become one of the topics of interest in the wireless communications. UWB systems are capable of transmitting data over a wide spectrum of frequency bands with low power and high data rates [1]. They have good properties such as large transmission capacity, fine time and range resolution, less multi-path fading effect and easier material penetration [1]. Some possible applications are high data-rate wireless communication systems, high-accuracy positioning and locating radars, and ground-penetrating radars [1].

A critical block in the UWB receivers is the low-noise amplifier (LNA). UWB LNA must meet several stringent requirements such as broad-band input matching, sufficient gain, low noise figure (NF), low power consumption and small chip area. Several topologies have been proposed to implement ultra wideband LNA [2-10]. Inductive source degeneration technique which resulted in good input matching and also a good noise figure in narrow-band LNAs [14] has also been used in the LNA in [2], in which the input impedance of the LNA is embedded into a multi-section reactive network in order to form a band pass filter at input. This topology provides wideband input matching, but usually does not have good noise figure at high frequencies. In addition, it needs large number of high-Q inductors and thus, occupy large chip area. In [3] a common-gate (CG) configuration was used which resulted in a wideband input matching and good reverse isolation, and therefore good stability. However, the NF of the CG LNA is considerably larger than that of the common-source or cascode LNAs [3,4]. The NF performance of a UWB CG LNA can be improved by employing gm-boosting technique [4,11], but this topology usually does not have enough gain. Shunt feedback is another popular bandwidth-extending approach [5]. The resistive shunt-feedback-based amplifiers provide good wideband matching, flat gain and reduced NF, but they suffer from large power dissipation and instability problem.

Distributed amplifiers (DA) are well known for their ability to increase the gain-bandwidth product [6,15,16]. DAs normally provide flat gain, very wide bandwidth with lower boundary as low as several MHz and upper boundary as large as several tens of GHz and have a good linearity and input and output matching [15-16]. However, DAs usually provide only moderate gain, occupy significant chip area and consume large power [15-16]. Furthermore, the noise figure minimization has seldom been addressed for the distributed topologies. Recently, the design of low-power distributed amplifier by biasing the transistors in moderate inversion has been proposed [7], but most of these designs do not provide enough gain and bandwidth.

In [8] a feed-forward noise canceling technique was used which effectively lowers the noise figure within the targeted band while occupying small chip area and consuming reasonably low power. In this technique thermal noise of the input transistor and noise of its biasing circuitry, and also the distortion of the input transistor, are sensed and canceled by a feed-forward configuration [8]. Not only feed-forward eliminates concern for potential instability that could be caused by a feed-back loop (negative feedback), but also by canceling the effect of the input transistor noise at output, both input matching and noise performance can be optimized simultaneously without any trade-off between them. However, the noise canceling requirement restricts the gain of the latter stage in the circuit [9-10] and thus, decreases freedom for controlling gain of the amplifier. Therefore, the gain of this configuration is not sufficiently high [9-10].

In this paper an ultra wideband LNA is proposed in which both the gm-boosting and the noise canceling techniques are

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used, however, by modifying the noise canceling strategy, it was possible to achieve a better noise performance and a higher gain at lower power consumption in comparison with some recently published noise canceling LNAs.

The paper is organized as follows. In section II principles of circuit design are described and in section III simulation results are presented. A summary of the important results are given in section IV.

II. DESCRIPTION OF THE PROPOSED LNA CIRCUIT

Schematic of the proposed LNA is shown in Fig.1. The design of the circuit incorporates the input transistor noise canceling technique and the gm-boosting technique which were introduced in [9] and [4,11], respectively. It consists of a common-gate input stage (M1), a common-source second stage (M2, M3 and M5) and an output buffer (M4 and M6). Wideband input matching is provided by proper selection of the dimensions of the input devices that form a fourth order band pass filter at the input port, as will be explained shortly. Asymmetric T-coil peaking and bridged-shunt-series peaking techniques were employed to provide the desirable bandwidth [12]. The inductors L9 and L10 in the output stage are used to provide wideband 50Ω output matching using the bridged-shunt-series peaking technique. Transistors M5 and M6 act as current sources and capacitors C2 and C3 provide ac grounds over the targeted band. The common-source stage is designed based on canceling the noise of M1 [9], but in comparison to the circuit in [9], an extra inductance L7, which has mutual inductance with L6, is introduced for the purpose of noise reduction, as will be explained next.

The basic structure of the proposed circuit is adopted from the LNA in [9]. The motivation for this circuit came from the observation that to cancel the noise of M1, the dimensions of M2 and M3 need to have specific values dictated by circuit topology [9], which do not necessarily coincide with the dimension values of M2 and M3 which result in the highest overall gain of the LNA. It is also observed that according to the Fig. 11 in [9], after canceling the noise of M1, the dominant source of noise at the output originates from M3 in Fig. 3 of [9]. Therefore, the question is raised that whether it is possible

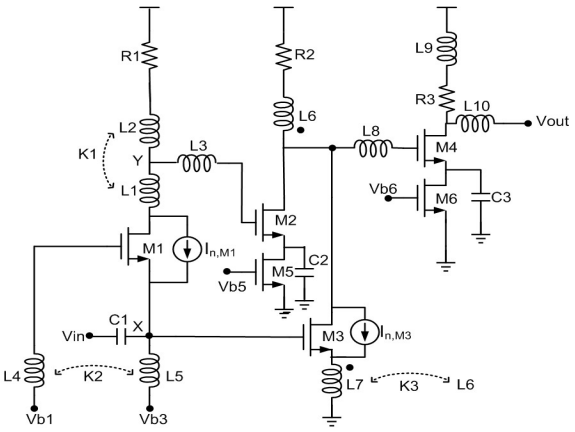

Figure 1. The proposed UWB LNA

to get a better performance from the LNA by choosing M2 and M3 dimensions different (slightly) from what is demanded by the complete cancellation of the noise of M1, in such a way to obtain an overall higher gain. Naturally, the overall noise figure would deteriorate, as the noise of M1 is not completely canceled with the new values of M2 and M3 dimensions, but this may be compensated by canceling the other important source of noise, i.e. M3's, by some other means, i.e., insertion of an inductor L7 at the source of M3, which has the proper sign and value of mutual inductance with L6. This idea is demonstrated in Fig. 2.

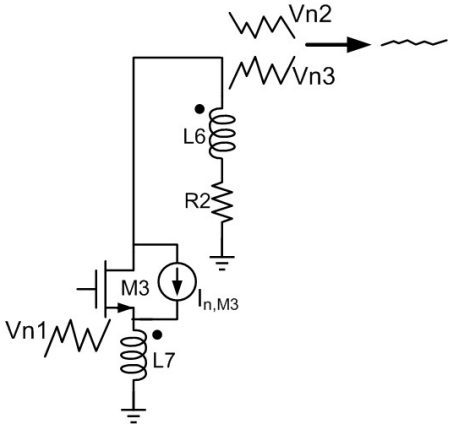

Figure 2. The employed Mechanism for noise canceling of M3.

In Fig.2 the thermal noise of M3 is modeled with $I_{n,M3}$. This current source generates two correlated noise voltages Vn1 and Vn2 at drain and source of M3, respectively, with opposite phases. On the other hand, the mutual inductance between L6 and L7 causes that Vn3 at drain of M3 to be in the opposite phase of Vn2. These two correlated noise voltages, Vn2 and Vn3, can cancel each other at drain of M3. Therefore, noise effect of M3 is canceled at the output node. Since L6 is already present for bandwidth extension, the intertwined inductor L7 does not increase the chip area much [17].

Insertion of L7 does also have the undesirable effect of decreasing the gain of the second stage. However, simulation results show that the gain improvement resulted from modifying the dimensions of M2 and M3 is dominant.

The noise contribution of M3 to the total output noise of the amplifier is shown in Fig.3 for two different situations: the case that M3's noise is canceled (i.e. L7 is inserted and all circuit parameter were optimized), and the case that M3's noise is not canceled (i.e. L7 is removed and other elements are optimized for the best performance). As shown in Fig. 3, in the proposed LNA, the noise contribution of M3 to the total output noise is less than 1% for the whole frequency range of 3.1-10.6 GHz, which means that the effect of the noise current of M3 ($I_{n,M3}$) at the output node is significantly reduced.

After canceling the noise of M1 and M3, the noise figure of the LNA is essentially determined by noise of R1 and M2, therefore, noise figure of the proposed LNA is given by (1-3):

$$F_{M2} = \frac{4kTg_{m2}\gamma/\alpha}{kTR_s(g_{m1}R_1g_{m2}+g_{m3})^2} \quad (1)$$

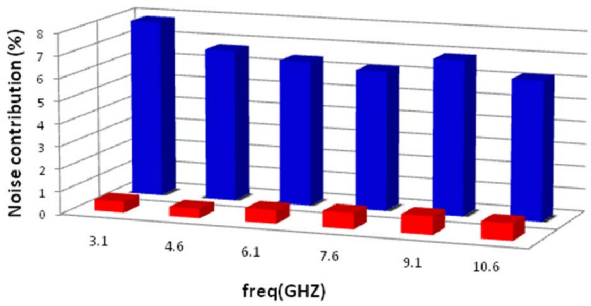

Figure 3. Simulated noise contribution of M3 to the total output noise with and without canceling the noise of M3 (i.e. with and without L7).

$$F_{R1} = \frac{4kTR_1 g_{m2}^2}{kTR_s (g_{m1} R_1 g_{m2} + g_{m3})^2} \quad (2)$$

$$NF = F_{R1} + F_{M2} \quad (3)$$

Relations (1) and (2) are adopted from [9] with elimination of the effect of the noise caused by M3 taken into account. These relations provide insight for sizing circuit component. According to (1) and (2) in order to minimize the contribution of R1 and M2 at the LNA's output noise, the value of R1 should be maximized. Increasing R1, at the same time, leads to reduction of biasing gate voltage of M2 and makes its noise performance worse [9]. With the help of an optimization tool (to be explained later), value of R1 was determined as 190 Ω, which provides both an acceptable noise performance and a suitable biasing voltage for gate of M2.

By using a gm-boosting scheme wherein inverting amplification is introduced between the source and gate terminals of M1, the power consumption and noise factor of UWB LNA can be significantly reduced [4]. In this paper, to implement enough inverse gain from source to gate, an on-chip transformer was used (L4, L5) [11]. Since L5 is already present for biasing, this intertwined transformer needs only a slight increase in chip area [17]. By employing the gm-boosting technique in the proposed LNA, the effective transconductance of M1, gm_1, was boosted to $2gm_1$ [11]. In Fig. 4 the NF and S21 of the proposed LNA are compared with those of two

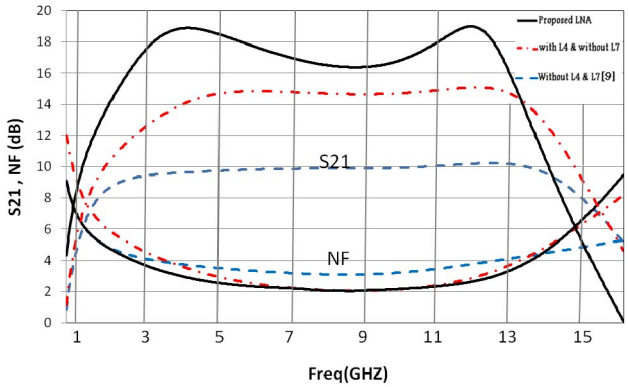

Figure 4. Simulated NF and S21 of the proposed LNA in three different Situations.

different modified versions of the circuit: the case in which L7 is removed but L4 is present, and the case in which both L7 and L4 are removed (in both cases other elements are optimized for the best performance). As can be seen in the Figure, there was an increase of at least 6 dB in the gain and about 1 dB improvement in NF of the proposed LNA (solid line) compared with the simulated results of the circuit proposed in [9] (dashed line). Also, there is an improvement of at least about 2 dB in gain compared with the case in which both gm-boosting and noise canceling for M1 only are employed (dash-dot line). The variation of the gain of the proposed LNA within the target band of 3.1-10.6 GHz is relatively small.

Small signal approximate equivalent of the input circuit is shown in Fig. 5. At the LNA's input, the equivalent impedance of the gm-boosting stage [11] is combined with the inductor L7 and the intrinsic capacitances of M3 to form a fourth order band pass filter. This structure can provide good input matching in a very wide bandwidth [2]. The LC filter is designed so that it suppresses signals outside the UWB standard.

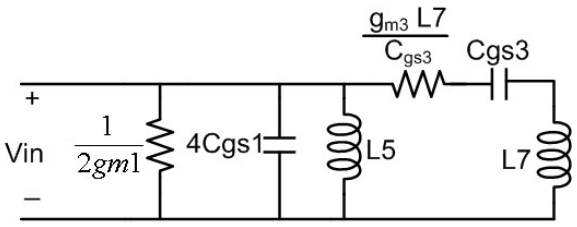

Figure 5. Schematic of the LNA's input network.

In the proposed LNA, the numbers of independent variables were large enough that raise the circuit complexity to a level which is difficult to optimize manually. Therefore, an automated technique was used to optimize circuit performance. The proposed CAD was based on the multi objective genetic algorithms. The simulations involved 24 independent variables to be optimized. The optimization targets were: bandwidth, average power gain, average NF, power consumption, and input reflection coefficient. Hspice RF was used to evaluate the performance of the solutions that generated by optimization tool in each iteration. The procedure was able to provide significant performance improvement at the end of optimization. The final circuit parameter values are shown in table I.

TABLE I. DESIGN VALUES OF THE PROPOSED LNA.

$(W/L)_1$ (43.5/0.18)	$(W/L)_2$ (22.3/0.18)	$(W/L)_3$ (41.6/0.18)	$(W/L)_4$ (68.2/0.18)	V_{b1} 1.06v	V_{b3} 0.47v
I_{M5} 2.1 mA	I_{M6} 2.83 mA	R1 190 Ω	R2 130 Ω	R3 80 Ω	L1 6n
L2 5.5n	L3 0.8n	L4 5.8n	L5 5.9n	L6 3.5n	L7 2.8n
L8 0.4n	L9 0.3n	L10 0.3n	K1 0.85	K2 0.87	K3 0.79

III. SIMULATION RESULTS

The proposed UWB LNA is designed with a commercial 0.18 µm RF CMOS technology and Hspice RF was used for simulations. All inductors are on-chip with spiral shape and capacitors are metal-insulator-metal type. Simulated S parameters and Noise Figure are shown in Figures 4 and 6. A power gain S21 of 17.5±1 dB in the frequency range of 3.1-10.6 GHz is obtained. Input reflection coefficient S11 is below -17 dB. Output matching S22 is below -12 dB and the reverse isolation S12 is less than -40 dB over the entire 7.5 GHz bandwidth. The minimum NF of 1.95 dB occurs at 9.5 GHz. The noise figure is below 3.3 dB with the average value of 2.25 dB in the frequency range of 3.1 to 10.6 GHz. The LNA consumes 10.6 mW with a 1.8V supply voltage.

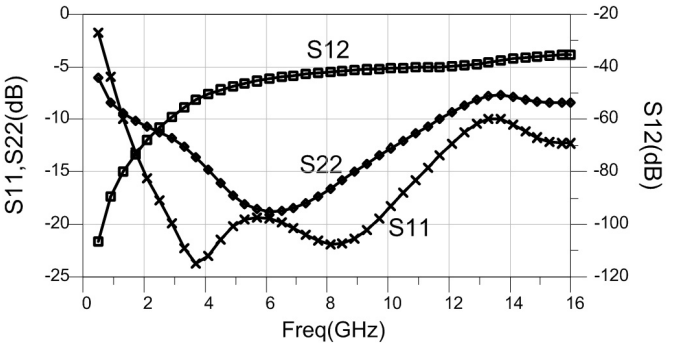

Figure 6. Simulated S12 and S22 of the proposed LNA.

The parameter µ [13] being greater than 1 guaranties that the LNA is unconditionally stable. Simulation results of the proposed LNA show that in the frequency range of 3.1-10.6 GHz, µ>4.5.

For a wideband application, a constant group-delay is desired in order to minimize the phase distortion. Group-delay of the proposed LNA is 92±28 ps across the entire band. Therefore, the amplifier has reasonable group delay [2,18].

Due to the low power of their input signals [1], UWB LNAs seldom suffer from gain compression. However, the IIP3 can be an important parameter of linearity in UWB LNAs, as strong narrow-band interferers can exist in the reception band. As shown in Fig.7, at 6 GHz the input third-order intercept point (IIP3) is -16 dBm, where a two-tone test is performed with 10 MHz spacing. Linearity characteristic of the UWB LNA is attributed to the last stage of the LNA and can be improved at the expense of higher power consumption.

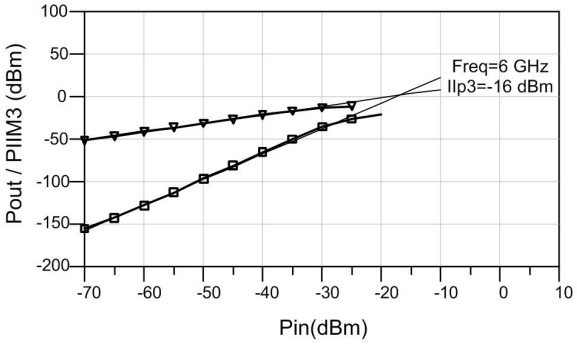

Figure 7. Simulated IIP3 of the proposed LNA.

Today's antenna design techniques can easily reject interferers using notch filters and as such, relaxes the requirement for the linearity of the UWB LNA [2]. Therefore, the IIP3 of the proposed LNA is not of great concern in the design of UWB and the relatively low value of the IIP3 of the proposed LNA can be acceptable.

Table II summarizes the performance of the proposed UWB LNA and makes a comparison of the circuit with the *simulation results* of the recently published LNAs. It is seen that the proposed LNA exhibits superior gain and noise figure compared with some previous published works.

IV. CONCLUSION

A 3.1-10.6 GHz UWB LNA designed in 0.18 µm CMOS process is presented. Combination of noise canceling and gm-boosting techniques were employed to improve the noise performance of the proposed LNA, so that a good NF is obtained within the whole range of 3.1-10.6 GHz. Desirable ultra broadband gain and noise performance is achieved by asymmetric T-coil peaking and bridged-shunt-series techniques.

In the proposed LNA, three mechanisms (i.e. noise canceling of M1, noise canceling of M3, and gm-boosting) were used to control noise performance of the amplifier, therefore the restriction placed on the dimensions of M2 and M3 demanded by the complete noise canceling of M1, is relaxed and they can be designed to provide a higher gain. As a result, the proposed LNA, exhibits superior power gain compared with previous noise canceling LNA. In order to have the best performance, values of all elements were optimized using genetic algorithms. The specifications of the optimized circuit are shown in Table II.

TABLE II. SUMMARY OF LNA PERFORMANCE AND ITS COMPARISON WITH SOME PREVOUSE PUBLISHED DESIGNS.

Ref	Topology	Technology	BW (GHz)	NF (dB)	$S21_{max}$ (dB)	S11 (dB)	Power (mW)	IIP3 (dBm)
[2]	L-degenerated	0.18µm CMOS	3.1-10.6	3.1-6	17	<-8	11.9	-7 @ 6 GHZ
[3]	CG	0.18µm CMOS	3.1-10.6	3.1-5.7	17.5	<-9	33.2	--
[6]	Distributed	0.18µm CMOS	2-11	4.2-5.7	12.5	<-17	19.6	--
[9]	Noise-Canceling	0.18µm CMOS	3.1-10.6	3.8-4.3	11	<-11	20	-6.2 @ 6 GHZ
[17]	Noise-Canceling	0.18µm CMOS	3.5-10.4	3.3-4	17	<-10.5	12.9	--
This work	Noise-Canceling	0.18µm CMOS	3.1-10.6	1.95-3.3	18.5	<-17	10.6	-16 @ 6 GHZ

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