Linearity Enhancement in Digital-to-Analog Converters Using a Modified Decoding Architecture

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***Abstract*— In this paper, a novel architecture for implementation of segmented Digital-to-Analog Converters (DACs) has been proposed. In this architecture, the array of unit elements has been divided into four similar sub-arrays and binary to thermometry conversion is performed in three control levels. The proposed control levels are connected to the sub-arrays in different sequences, thus different analog outputs according to the random mismatch distribution of sub-arrays is achieved. This architecture in addition to an extra multiplexer provides the possibility to test the chip after its fabrication in different sequences and the most linear one based on static linearity metric (INL-Yield) or dynamic performance (SFDR) be selected. Monte-Carlo simulations for an 8-bit unary DAC has shown that in the proposed architecture the probability of achieving a more linear DAC is much more than conventional one. Hence, preserving the required linear output, the mismatch of the unary elements could be increased i.e. the area of the unary array and the whole chip could be decreased.**

I. INTRODUCTION

Segmented architectures are widely used in high-speed and high-accuracy digital-to-analog converters (DAC's) [1], [4]–[10]. Fig.1 shows a segmented current steering DAC (CS DAC) in which the least significant bits (LSB's) are realized using a binary-weighted array and the most significant bits (MSB's) are thermometer decoded (and implemented with a unary array). Increasing the number of thermometry bits guarantees the monotonocity**,** reduces the glitch energy (caused by timing mismatch error of the switches while the input code is changing), reduces the Total Harmonic Distortion and increases the linearity of the converter [1].

One of the most important parameters introducing the performance of DACs is the yield of integral nonlinearity (INL-Yield) which is the percentage of devices that meet defined INL_{max} specification to maintain the monotonicity feature of the converter. Production tolerances, which can result in random mismatch and systematic errors, are among the main reasons for lower yields in CS DACs. Process variations such as the gate oxide thickness, the threshold voltage or the voltage drop along the ground line are resources of systematic errors. Various switching scheme techniques exist to minimize the impact of these errors. In a CS DAC, the switching scheme determines the interconnections between the outputs of the thermometer decoder/latch and the control terminals of the switches in the current matrix.

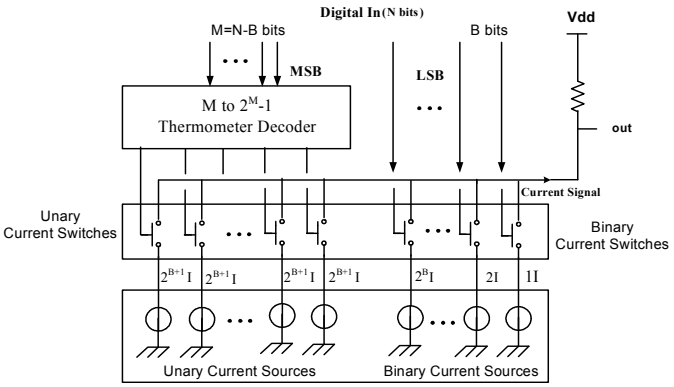

Figure 1. simplified structure of an N-bit CS DAC

On the other hand, the random errors are determined by the inherent matching properties of the technology used. In CS DACs, the random errors of the current sources are modeled as independent normally distributed random variables with mean I and variance σ_I^2. The ratio between the current deviation and current mean value (σ_I/I) is referred to as the relative matching (σ_{rel}). Based on the maximum permitted value of this deviation to meet the desired INL-Yield [2], the minimum area of the unit current source transistor (W.L) is determined which is proportional to σ_{rel}^{-2} [3]. Not only the linearity of the converter depends on the random mismatch but also it depends on its distribution outline which has an important role in determining the amplitude of the spurious frequencies and consequently the Spurious-Free Dynamic Range (SFDR) in the converter.

Calibration techniques can correct for element mismatch, paying with additional resources and affecting in some way the D/A conversion process [4]. Dynamic element matching (DEM) techniques change the distribution of the errors in such a way to improve the linearity and utilize randomization so that the matching errors become signal independent [5]. However these techniques cause the converter to become very complicated. An alternative approach that alters the distribution of the mismatch errors is re-mapping

(programming) of thermometer switching sequence with large memory blocks [6] but at a price of doubling the converter area. Using redundancy in the binary-to-thermometer decoder [7] which generates two different switching sequences is another approach to reach a linear characteristic. This technique requires redundant elements and complicates hardware resources.

In this paper a novel structure for conversion of binary-to-thermometry process is proposed. Using this structure, changing the random mismatch distribution of the unary array, without using described complicated techniques is possible. This new decoding architecture in addition to an extra multiplexer provides the facility to test the chip after its fabrication in different configurations so that the best structure based on the INL or the dynamic performance (SFDR) can be selected.

The paper is organized as follows. After a review of the conventional decoding structure in section II, the proposed architecture and its design considerations will be described in section III. Simulation results are given in section IV followed by the conclusions in section V.

II. CONVENTIONAL ROW-COLUMN DECODING ARCHTECTURE

The row-column binary to thermometry decoder was proposed for the first time in [8] and followed by a few variations e.g. in [9]. The digital inputs are first decoded into thermometer-coded signals used to drive the row and column lines. Then a trivial logic circuit in each individual cell determines whether to turn the current source at a given position on or off. Fig. 2 shows a 10 bit CS DAC architecture which its 8 MSB bits are decoded based on this structure [1]. In this architecture, if the previous row is high and either the current column strobe or the current row strobe is high, then the current source should source current through the positive output terminal. To have a correct decoding operation, the first signal of the first row is connected to the V_{DD} and the second signal of the last row is connected to the ground. So the unit cell array includes some turned-on rows regardless of the columns, one row with some turned-on and some turned-off cells and the other rows are completely turned-off. This decoding architecture is simple and area efficient.

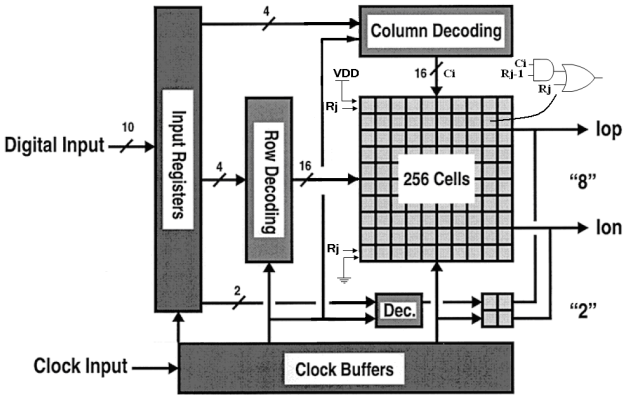

Figure 2. A 10 bit DAC with row-column decoding architecture [1].

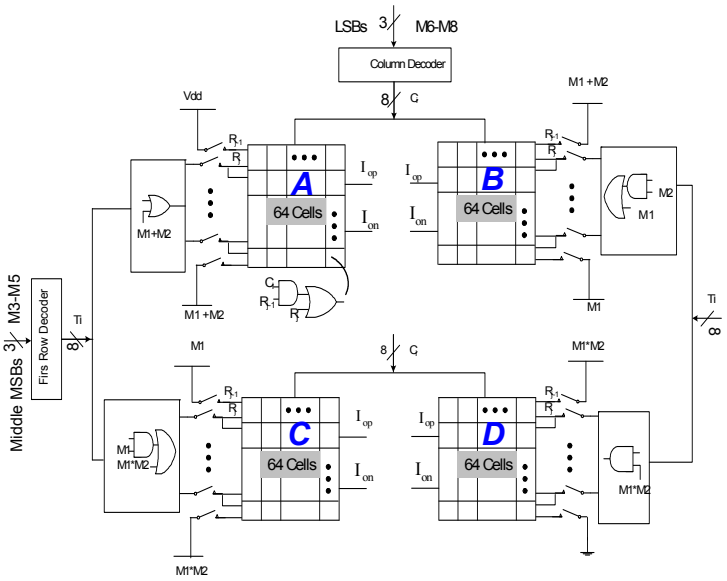

Figure 3. An 8-bit unary DAC using the proposed decoding architecture.

III. PROPOSED DECODING ARCHITECTURE

A. *Multi output characteristics using the proposed binary-to-thermometer decoder*

In conventional decoding architecture, only one output characteristic can be expected based on the distribution of random mismatch error in unary array. Fig. 3 shows the proposed architecture realizing an 8-bit unary DAC in three control levels with the capability of generating different output characteristics with minimum possible complexity. The main idea in this structure is the division of the unit element array into four equivalent sub-arrays and selecting each of these sub-arrays by a function of two MSB bits (M1, M2).

As it can be seen in Figure 3, the unit cell array (with a dimension of 16*16) is divided into 4 equivalent sub-arrays (with a dimension of 8*8) and 3-input decoders (instead of 4-input decoders in conventional one) with an extra control level are used. In order to select each of these sub-arrays, two MSB bits (M1, M2) are used. Each row signal in sub-arrays is a function of the proposed control levels and thermometry coded of middle MSBs (M3-M5). In this Figure decoding action in the first control level is performed by the two MSB bits and according to their values, sub-arrays will be selected. After selecting the desired sub-arrays, the decoding action in the second and the third control level, is performed similar to the conventional row-column decoding (see Figure 2) by two 3*7 decoder (instead of two 4*15 decoders). The difference is that, the signals of the first and the last rows of the sub-arrays are realized using a function of the most significant bits, as can be seen in the Figure 3.

In order to have a better understanding of this architecture, the primary control levels which select the sub-arrays according to the two most significant bits (M1, M2) have been shown in Figure 4. According to this configuration, full scale output is divided into 4 sections and according to the significance of the input digital bit, one or more of these levels will be selected.

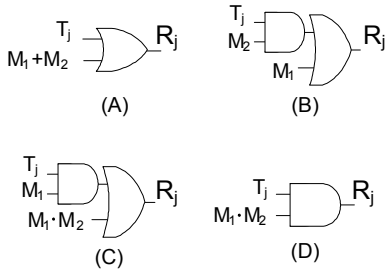

Figure 4. Primary control levels as a function of two first MSB bits.

As shown in Figure 4 by changing the first two MSB bits from 00 to 11 (in a binary sequence) the control levels and consequently sub-arrays A to D are activated respectively. For instance, if the value of the input digital word is in 3/4 the output full scale, (M1=1, M2=0), two sub-arrays (A, B) will become completely turned on independent of the LSB bits (M3-M8), and the third sub-array will be turned on based on the value of LSB bits, so the logical function C in Figure 4 is realized.

As for each extra input bit in the binary-to-thermometer decoder the number of utilized gates is doubled, in the proposed architecture (which utilizes 3 input instead of 4 input decoders besides proposed control levels in Figure 4), without increasing the total number of decoder gates, the distribution of random mismatch error in unary array could be easily changed as discussed below.

B. Changing the random mismatch distribution of unary elements in the proposed architecture

As the sub-arrays in the proposed structure are completely similar, there is not any restriction to connect the proposed control levels to the specified sub-arrays. The intermediate row switches between the sub-arrays and the proposed control levels has been drawn for this reason. Controlling of these interface connections is possible through a multiplexer (outside the converter). So the proposed control levels can be connected to each of the sub-arrays in different sequences i.e. different output characteristics could be examined based on the distribution of the unary array random mismatch error and totally 24 (=4!) different output transfer characteristics could be extracted. The only extra unit is a digital multiplexer which could obtain different sequence alterations and its size depends on number of possible selection for changing the sub-array sequences.

After the chip is fabricated, different connections between the sub-arrays and the control levels (which have been predicted during the design procedure) are tested and the best of them, based on the static (INL-Yield) or dynamic (SFDR) output characteristics will be selected. Since realizing the possibility to test all different 24 combinations is too complicated to be acceptable, just some restricted possible combinations (4 or 8 combinations) can be considered during the design procedure. As simulation results show, by increasing the number of interconnections between the intermediate control levels and the sub-arrays which mentioned as index interface, the probability of linearity enhancement in the converter much more increases.

IV. SIMULATION RESULTS

To demonstrate the effectiveness of the proposed structure in improving the DAC linearity, an 8-bit unary DAC (the floor-plan of which is shown in Figure 3) is simulated using MATLAB. The random mismatch distribution of the DAC unit elements is modeled as independent random Gaussian functions. The resulting maximum INL error and SFDR is investigated as a function of the standard deviation of the unit elements.

Fig. 5 shows the distribution of INL_{max} in conventional and the proposed DAC architectures (with 4, 8 and 12 index interface between sub-arrays and control levels) resulted from a Monte-Carlo simulation with 1000 statistical runs. The relative mismatch of unit elements is σ_{rel}=3.5% (0.035). In each simulation, a new random error distribution (through 16*16 unary array with σ_{rel}=3.5%) has been generated and the value of INL_{max} in that case has been chosen as the worst INL. As can be seen in Figure 5, in conventional structure, when only one connection between the control levels and the sub-arrays is used, only 665 samples of 1000 samples have an |INL|<0.5LSB (Figure 5.a).

In the performed simulations, by setting up the possibility of 2, 4, 8, 12 and 24 index interface between the proposed control levels and the sub-arrays, the maximum value of the INL-Yield in the best condition (the least INL_{max} in one of the selected combinations) reached to 78%, 89%, 93%, 96% and 98% respectively. For instance, when the number of selectable combinations (index patterns) is 4, the INL-Yield based on the least resulted INL_{max} in each case reached to more than 89% (Figure 5.b). It is noticeable that these 4 combinations have been selected completely randomly, and selecting another 4 combinations may lead to other results.

Fig. 6 shows the INL-Yield simulation results versus different unit element standard deviation to reach the |INL|<0.5LSB (with 4, 12 and 23 index interface between sub-arrays and control levels). According to this Figure, in the structures with more interface index between sub-arrays and control levels, a desired INL-Yield can be reached while having a larger standard deviation. Since σ_{rel} is inversely proportional to the square root of the current source transistor area [3], a considerable reduction in the current source transistor area will be possible.

On the other hand, according to (1), by increasing the unary-weighted random mismatch, the value of SFDR decreases [10].

$$SFDR \approx 20\log\left(\frac{3\pi}{4}\right) + 3 \cdot N - 20\log\left(\frac{\sigma_I}{I}\right) \qquad (1)$$

Figure 7 shows the SFDR characteristic versus σ_{rel} in the mentioned converter according to (1) and the simulation results in the conventional structure and the proposed structure with four possible connections between sub-arrays and the control levels. According to this figure, by changing the unary-weighted random mismatch distribution, the spurious harmonic amplitude also changes and the probability of reaching to a higher SFDR increases.

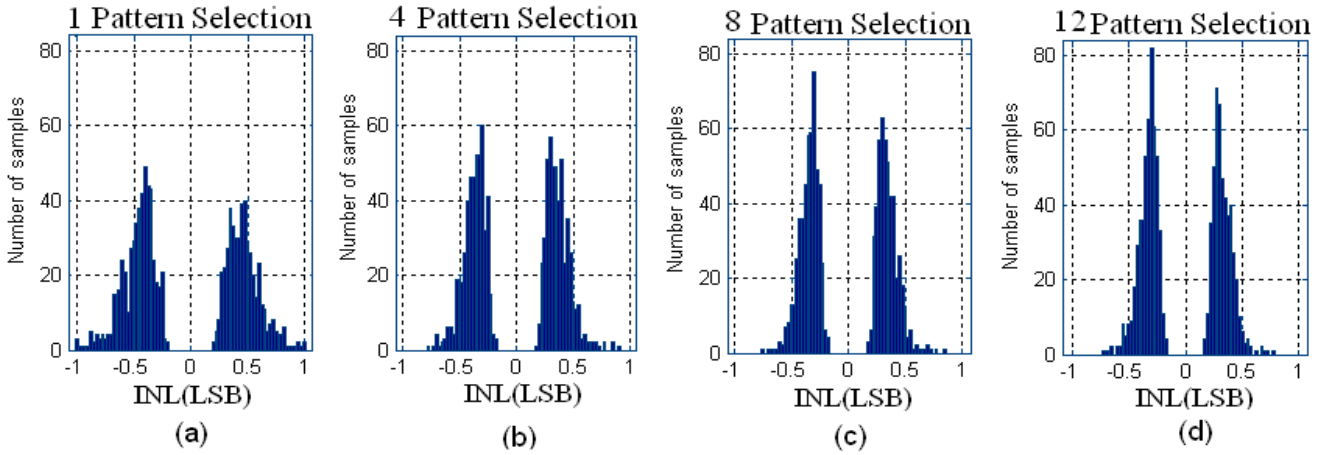

Figure 5. INL distribution in 1000 simulations for (a) conventional row-column, and the proposed decoding architecture with index interface of (b) 4, (c) 8 and (d) 12 between sub-arrays and control levels.

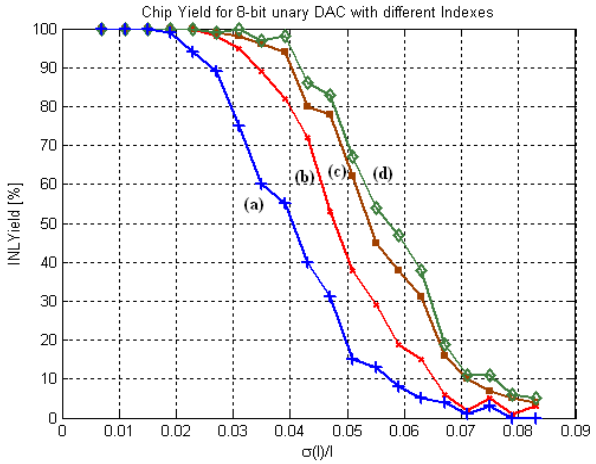

Figure 6. INL-Yield vs. standardd deviation: (a) conventional, the poposed decoding architecture with (b) 4 (c) 12 and (d) 23 index interface.

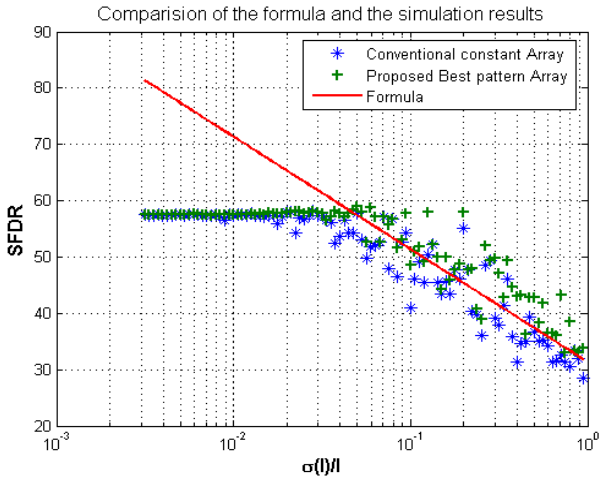

Figure 7. SFDR vs. sigma(I)/I in formula, conventional and the proposed architecture with 4 pattern interface between sub-arrays and control levels.

V. CONCLUSION

In this paper a novel decoding architecture to realize the DAC MSB thermometry section was proposed. Based on this architecture the mismatch error distribution of the unit elements can be simply changed and different output characteristics can be produced without any extra unit element. Using the proposed structure, an 8-bit unary CS DAC was simulated. The Monte Carlo simulation results show that using the proposed architecture considerably increases the probability of linearity enhancement in such a way that a larger mismatch for unary-weighted elements is permitted thus decreasing the chip area.

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