Low-Dropout Voltage Reference: An Approach to Buffered Architectures with Low Sensitivity

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Abstract— **A modified circuit topology for bandgap references capable of providing very high load current with output which has small sensitivity against temperature variations is presented. Employing a proportional-to-absolute-temperature (PTAT) current source and a complementary-to-absolute-temperature (CTAT) voltage source in a novel closed-loop configuration, the output voltage can be tuned over a wide range of voltages lower or higher than Silicon bandgap voltage of 1.2V. These features make the configuration a promising competitor for low-dropout regulators. Low-power and low-voltage design considerations of the circuit offering many advantages are addressed. With different specifications, two design examples in 0.18-μm standard CMOS technology are reported. Thanks to a modified amplifier topology, the 0.9V and 1.3V bandgap references have fast stable operation for the load currents ranging from 0*m*A to 100*m*A with load capacitors as low as 10*p*F and no equivalent series resistance (*ESR*). Simulated values of the temperature coefficient for both design cases are smaller than 37ppm/^{0}C.**

I. INTRODUCTION

Bandgap references, insensitive to process, voltage and temperature variations are the basic building blocks in numerous analog, digital, and mixed-signal applications [1]. For many technical applications such as analog signal processing units, a voltage reference with low output-impedance is essentially needed to steer noise away from sensitive nodes and, at the same time, to providing large AC and DC load currents [2]. With no output buffer in series, a sub-bandgap reference able to sink and source up to 5mA load current is proposed [2]. The operation of the circuit is based on a BiCMOS error amplifier in which its input-referred offset must be proportional-to-absolute-temperature (PTAT). In CMOS technology, the configuration can be realized using lateral bipolar junction transistors (BJTs). However, full-CMOS circuit realizations are of more interest.. The circuit configuration in [2], from another point of view, is not convenient for accurate applications as its temperature compensation type is first-order. This in turn makes the output to be independent of temperature only at an assigned temperature.

Many techniques have been proposed thus far to devise a bandgap reference with high order temperature-compensation. However, most of them cannot provide any current, some cannot be designed for sub-bandgap voltages, and some have implementation issues like pre-regulated output requirement and/or precisely-matched current mirrors. The topology in [3] offers tunable output along with low-output-impedance. However, parasitic BJTs are required and temperature sensitivity is relatively high. The architecture in [4] can be designed to consume low power in low-voltage environment. Furthermore, the output is completely compensated in terms of temperature. However, serious issues are associated with this structure some of which are fixed reference output with worse standard deviation and high impedance, difficult trimming after fabrication, the need for different threshold voltages, and additional circuitry for mobility compensation. Some of these drawbacks can be solved using the switched-capacitor architecture proposed in [5]. Nevertheless, the need for non-overlapping clock phases makes it inappropriate for some applications. Low- and high-magnitude switching spikes of the clock signal appearing in the output voltage are also a source of error. In this paper, in a standard CMOS technology with no additional signal or parasitic devices required, a new architecture employing a PTAT current source and a complementary-to-absolute-temperature (CTAT) voltage source in a closed-loop configuration will be presented. The circuit has a small dropout voltage and can operate with line voltages close to the output reference voltage. To guarantee a fast transient response under the large variations of load current and line voltage, a low-power high-performance amplifier is proposed. The amplifier enables the structure to provide large load currents.

II. THE PROPOSED ARCHITECTURE: OPERATION

Fig. 1 shows the proposed schematic combining all the interesting features previously highlighted. In this architecture, the negative input terminal of the error amplifier is biased via a simple complementary-to-absolute-temperature (CTAT) voltage source. In order to directly compensate for the temperature dependence of the output voltage, a PTAT current source is also added. Again assuming a high DC gain for the amplifier, the output voltage can be calculated from

$$V_{out} = (1+\frac{R_2}{R_1})V_{CTAT} + R_2 I_{PTAT} \quad . \qquad (1)$$

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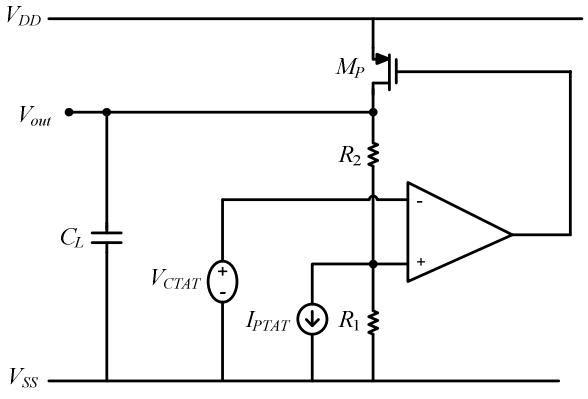


Figure 1. Proposed implementation for a buffered voltage reference

Hence, if carefully designed, a buffered yet tunable voltage reference with minor sensitivity against temperature variations is realized. For this output voltage, in order to have a Zero-Temperature Coefficient (ZTC), the derivative of (2) against temperature must become equal to zero; i.e.

$$(1+\frac{R_2}{R_1})\frac{\partial}{\partial T}V_{CTAT}+R_2\frac{\partial}{\partial T}I_{PTAT}=0$$
$$\Rightarrow \frac{\partial}{\partial T}V_{CTAT}=-(R_1\,\|\,R_2)\frac{\partial}{\partial T}I_{PTAT}. \quad (2)$$

If (3) holds at all temperatures, the output will not be a function of temperature. Therefore, while the value of $R_1\|R_2$ determines the temperature dependence of the output voltage, the ratio of R_2/R_1 can be used to set its absolute value. Another advantage of the proposed architecture is the small dropout voltage; i.e. similar to an LDO, the difference between V_{DD} and V_{out} can be kept as low as a couple of hundred millivolts even if the load current is increased to several milliamps.

Subsequent section is dedicated to a possible implementation of the building blocks illustrated in Fig. 1.

III. The Proposed Architecture: Implementation

To completely compensate for the temperature sensitivity of the reference output, two fundamental temperature-related parameters have been chosen which have complementary behavior. One good candidate to implement the CTAT voltage reference of Fig. 2 is the threshold voltage of MOS transistor. With good approximation, this parameter decreases linearly with temperature as

$$V_{TH}(T)=V_{TH}(T_0)-\alpha(T-T_0), \quad (3)$$

where T is the absolute temperature and T_0 is the temperature where α has been evaluated. On the other hand, to generate a PTAT current, a circuit that employs the difference between two base-emitter voltages of bipolar transistors can be used (note that V_{BE1}-V_{BE2} α $V_T = kT/q$) [2]. However, in order to make the implementation fully compatible with CMOS technology, we have used an approach based on MOS devices operating in weak inversion.

A. CTAT voltage generator block

The circuit shown in Fig. 2 generates a threshold-referenced output voltage [6]. To gain more insight into the operation of this circuit, suppose that V_{DD} increases. When this happens, V_{out} is also pulled up via M_{C4}, which is operating in source follower configuration. However, M_{C3} with now a higher gate input (V_C) has a complementary effect on the V_{out} Hence, two V_{DD}-dependent forces with different signs should be appeared in mathematical representation of V_{out}. Depending on the value of V_{DD}, the four devices in Fig. 2 experience different regions of operation. When V_{DD} is large enough to maintain M_{C2} and M_{C3} in strong inversion i.e. when $V_{DD} > 2.V_{TH} + 2.V_{DS(sat)}$ ($V_{DS(sat)}$ is the overdrive voltage), M_{C1} is triode whereas all other devices are saturated. Under these circumstances, denoting γ as the ratio of $(W/L)_{C3}/(W/L)_{C4}$ and utilizing the conventional MOS I-V equations, it can be shown that if

$$\sqrt{\gamma}=\frac{1}{1-1/\sqrt{1+(W/L)_{C2}/(W/L)_{C1}}}, \quad (4)$$

V_{out} will be completely independent of V_{DD} and is given by

$$V_{out}=\sqrt{\gamma}V_{TH}. \quad (5)$$

A CTAT voltage source based on the threshold voltage devices thus is generated. Since an operating point with no current flow is not stable in Fig. 2, a start-up circuit is not required here.

B. PTAT current generator block

PTAT current sources can be implemented using BJT devices. A good alternative based on MOS devices is depicted in Fig. 3. The basic idea comes from the bandgap reference reported in [7]. In this circuit, M_{P3} and M_{P4} operate in sub-threshold region. As a result, they consume small power consumption in a low-voltage environment. M_{P1} and

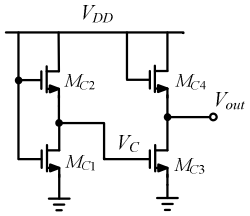


Figure 2. The employed CTAT voltage generator based on V_{TH}

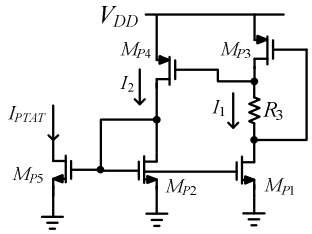


Figure 3. The employed PTAT current source based on peaking current mirror approach

M_{P2} construct a current mirror which leaves the configuration a self-biased topology. To produce a PTAT current, the circuit should be designed so that I_2 is at its peaking value [7]. This occurs when I_1 and I_2 are related by

$$I_2 = I_1 \frac{(W/L)_{P4}}{(W/L)_{P3}} e^{-1}, \quad (6)$$

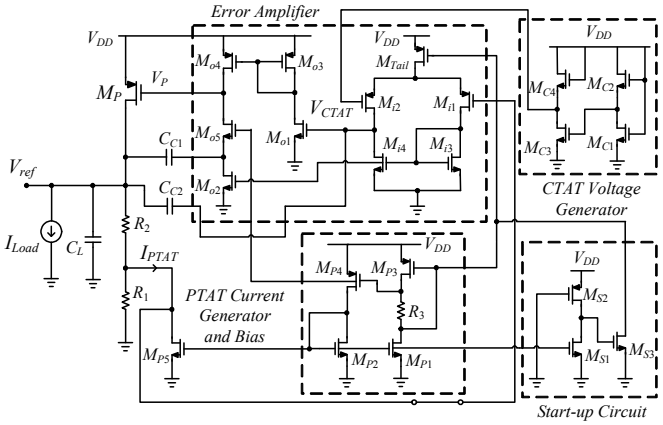
which is satisfied by properly sizing the aspect ratios. As a particular case, setting $(W/L)_{P1} = (W/L)_{P2}$ and $(W/L)_{P4}/(W/L)_{P3} = e$ will satisfy this condition. When this happens, all currents will be PTAT and I_1 is derived as

$$I_1 = \frac{nV_T}{R_3}, \quad (7)$$

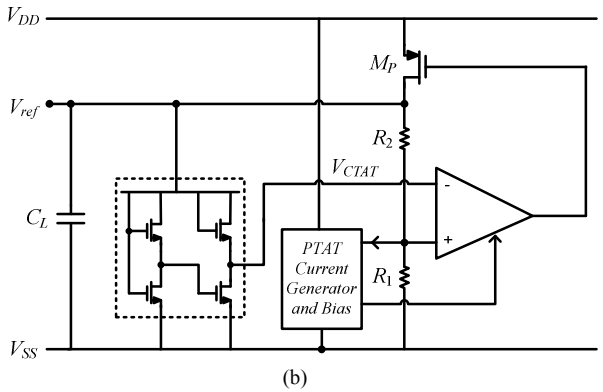
where n is the sub-threshold slope parameter. As it is seen, R_3 defines the absolute value of I_1 and eventually total power consumption.

C. Operation and design challenges

A possible implementation of the proposed circuit of Fig. 1 has been shown in Fig. 4a. The circuit benefits from a modified error amplifier with stable operation over a wide range of load current. The feedback loop controls the current of M_P which isolates V_{DD} from V_{ref} and, at the same time, provides the required load current. The reference output voltage is sensed through the resistive divider network. An appropriate error signal thus is generated to be amplified via the error amplifier.



(a)



(b)

Figure 4. Proposed circuit configuration (a) Complete schematics (b) Supplying the CTAT voltage generator from the reference output

In addition to transient behavior improvement, the two compensation capacitors in this circuit (C_{C1} and C_{C2}) serve to prevent instability during different load conditions. These capacitors along with M_{o1}, M_{o3}, M_{o4} and M_{o5} enhance the ac stability of the feedback loop by moving one pole to lower frequencies and the rest to higher frequencies. The PTAT current and CTAT voltage produced in Fig. 4a have the potential to completely cancel out each others. Assuming that M_{P2} and M_{P5} are identical (Fig. 3), if (5) and (7) are replaced into (1) and opamp and CTAT generator combined offset (V_{OS}) is included into the result, one can obtain

$$V_{ref} = (1+\frac{R_2}{R_1})\sqrt{\gamma}V_{TH} + \frac{R_2}{R_3}nV_T + (1+\frac{R_2}{R_1})V_{OS}. \quad (8)$$

If V_{OS} is assumed to be independent of temperature, (2) will still remain the condition to have ZTC. As a consequence, if

$$\frac{R_3}{R_1 \| R_2} = \frac{n.k}{q} \cdot \frac{1}{\alpha\sqrt{\gamma}}. \quad (9)$$

then (8) will be simplified into

$$V_{ref} = V_{ZTC} = (1+\frac{R_2}{R_1})\sqrt{\gamma}(V_{TH}(T_0) + \alpha T_0 + V_{OS}). \quad (10)$$

which is completely temperature-independent for any range of temperature. This is without any additional circuitry for mobility compensation as of the case of [4]. As an additional advantage, while R_3 and γ can help satisfying condition (9) for any reference value, the ratio R_2/R_1 adjusts the absolute value of buffered V_{ZTC} to be smaller, equal or larger than the silicon bandgap voltage. Equation (10), however, is an ideal case assuming V_{OS} and the gain of error amplifier to be temperature-independent, simplified transistor characteristics and the approximation used in model (3). Similar to other trimmable configurations, after fabricating the circuit, to minimize the temperature coefficient and to adjust the absolute value of the reference, trimming can be performed on either R_3 and R_2 or R_3 and R_1. Although the employed CTAT voltage generator can be optimized to reach an almost independent supply output (equation (5)), this may not be an optimized case in terms of temperature and process variation. The circuit should therefore be optimized to meet an acceptable performance for these parameters in minimum power consumption. Under these circumstances, to make the power supply of this unit unchanged, a proper circuit-level configuration is to supply the core of V_{CTAT} from the regulated V_{ref}, as shown in Fig. 4b.

IV. Design Examples

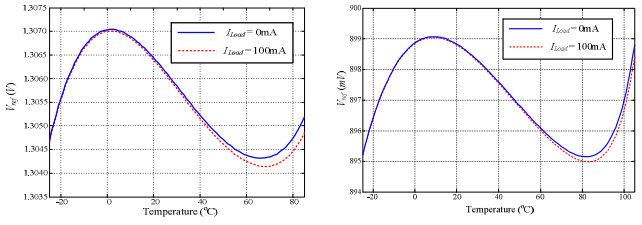
To show that the proposed bandgap reference can be flexibly designed for a wide range of specifications, two reference-voltage circuits are designed: first, a sub-bandgap reference with 0.9V output and 1.1-V minimum supply

voltage and second, a reference with 1.3V output and 1.5V minimum supply voltage. With small load capacitors, both designs are able to provide up to 100mA load current with stable operation at entire range of the output current. As there are different building blocks having contribution on the performance of Fig. 4b, the optimization process is divided into three steps: First, considering the value of reference output required, the CTAT voltage generator unit is optimized based on temperature performance, process variation, power consumption and line regulation. Considering the number of objective functions in this circuit, it is recommended to contribute both W and L of the devices into the optimization process. Second, with the optimized CTAT generator in hand, the PTAT current generator block, R_1 and R_2 can be optimized in configuration of Fig. 4b but with ideal error amplifier. The objective functions that should be considered in this step are the output absolute value, power consumption, area, temperature sensitivity and robustness against process variations. The third and final step involves with the values of C_{C1} and C_{C2} along with the device aspect ratios of error amplifier. The most important goal of this optimization step is to minimize the sensitivity of the output voltage to large load current and line voltage transient changes. Power consumption and area are of less concern here.

The two designs were simulated in 0.18μm standard CMOS process. Fig. 5 shows the output curves against temperature and I_{Load}. Table I summarizes the performance of the two configurations. Both designs consume less than 50μA of quiescent current. For the range of T = [-25°C, 85°C], output temperature coefficient is about 25ppm/°C for the 1.3V design and 36ppm/°C for the 0.9V design. For such a high drive capability, the simulated values of temperature coefficient are meaningfully small. Fig. 5 shows that the temperature compensation of the circuit is currently second order. However, higher orders of temperature compensation are achievable by means of advanced optimization methods. Monte-Carlo simulation of the output absolute values along with temperature coefficients reveals the tolerance of the circuit in presence of local mismatches. The results for 1000 iteration are illustrated in Fig. 6.

V. CONCLUSIONS

A new circuit architecture for buffered bandgap references with low sensitivity against temperature variations is proposed in this paper. The circuit offers a wide tuning range and, with respect to a regulator (an LDO in series with a bandgap reference), its trimming is easy.

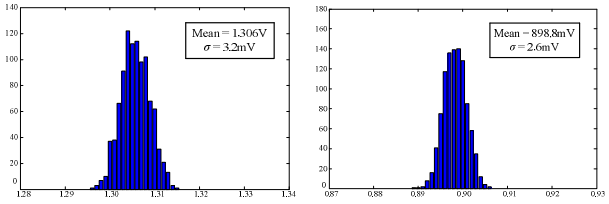


(a) (b)

Figure 5. Reference voltages against temperature
(a) 1.3V design (b) 0.9V design

TABLE I. DEVICE SIZES AND ELEMENT VALUES OF THE TWO DESIGNS

Technology		0.18μm Standard CMOS Technology	
Maximum Load Current		100 mA	
Average Output		1.308V	898.6mV
Minimum Supply		1.5V	1.1V
Load Capacitor		10 pF	50 pF
Total Compensation Capacitor		100 pF	130 pF
Average Quiescent Current		40.3μA	38.7μA
PSR @ 100*Hz*		-36dB	-55dB
Temperature Coefficient [-25 °C, 85 °C]	I_{Load} = 0 mA	24.8ppm/°C	35.7 ppm/°C
	I_{Load} = 100 mA	25.5ppm/°C	37 ppm/°C
DC Load Regulation (Dropout, I_{Load} = 0-100 mA)		11 μV/mA	60 μV/mA
DC Line Regulation	I_{Load} =0 mA I_{Load} = 100 mA	(V_{DD} = 1.5-2.5V) 12.5mV/V 12.1mV/V	(V_{DD} = 1.1-2.1V) 15.6 mV/V 15.5 mV/V
Transient Settling Time	**Load** 0.1% error (0mA –100mA)	(V_{DD} = 1.5V) 1.67μs + 1μs -	(V_{DD} = 1.1V) 1.74μs + 4.48μs -
	Line 1% error (0mA)	(V_{DD} = 1.5-2V) 27.2μs + 25.3μs -	(V_{DD} = 1.1-1.6V) 4μs + 3.65μs -



(a) (b)

Figure 6. Monte-Carlo simulation for I_{Load} = 100mA and T = 25°C
(a) 1.3V design (b) 0.9V design

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