

# Capacitor Scaling for Low-Power Design of Cyclic Analog-to-Digital Converters

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**Abstract**—In this paper, in order to reduce the power consumption of a cyclic ADC, for different cycles in digitizing an analog input sample, the values of the capacitors are scaled down. The power consumption of the operational amplifier is adaptively reduced as well. In order to demonstrate the effectiveness of the proposed technique, a 1.8V 12-bit 104kS/s ADC has been designed in a 0.18 $\mu$ m CMOS technology using the modified structure and compared with conventional implementation. HSpice simulations show that applying the technique has reduced the power consumption of the ADC with a factor of more than 2.1.

## I. INTRODUCTION

Cyclic (or algorithmic) analog-to-digital converters (ADCs) are used in moderate-to-high-accuracy and low-to-moderate-frequency applications, especially where low power consumption and low area occupation is required [1-3]. In a cyclic ADC, the residue signal is cyclic, thus only one stage is needed, and  $N$  periods are required to convert an  $N$ -bit digital code [4]. In these ADCs, noise and accuracy requirements decrease from the most-significant bit (MSB) to the least-significant bit (LSB) cycle, but the invested energy per cycle is “conventionally” constant. In [3], a two-stage cyclic ADC with amplifier- and capacitor- sharing technique is proposed. Although power saving is achieved, but the proposed technique has been used just in two-stage ADC architecture. In this paper, a novel architecture for a cyclic ADC based on capacitor scaling is proposed. Although the technique is well known for pipelined ADCs, no circuit implementation had been proposed for cyclic ADCs. For any sample of the input signal, since the first cycle determines the MSB, the second cycle, the second MSB and so on, there is no need to dissipate similar power in all cycles. We gradually decrease the power consumption by decreasing the amount of the capacitors used in each cycle and adaptively decreasing the bias current of the operational amplifier. Hence, the power consumption of the ADC considerably reduces. This technique can be applied to both single- and two-stage cyclic ADC implementations.

The rest of the paper is organized as follows. Section II introduces the conventional cyclic ADCs and explains a switched-capacitor (SC) implementation with 4-capacitor architectures commonly used in these ADCs. The proposed capacitor-scaling structure is presented in section III. The proposed circuit architecture and design considerations are

addressed in Section IV. Section V shows the simulation results followed by Section VI concluding the paper.

## II. BACKGROUND

In a cyclic ADC, the input signal is first sampled; then the sample is digitized to a very few bits using a coarse sub-ADC. Based on those bits, the residual signal is mapped back to the full-scale range using a multiplying digital-to-analog converter (MDAC). The output is fed back again to the same stage continuing the sub-A/D and multiplying D/A conversions. It continues for a definite number of cycles based on the ADC resolution.

The main power-consuming parts are the operational amplifier used in the MDAC and the comparator(s) used in the sub-ADC.

Although 6-capacitor architectures have been conventionally employed in cyclic ADCs [1], area-efficient 4-capacitor architecture has been reported in [2]. Although the proposed capacitor-scaling technique can be implemented in any SC architecture, we have implemented it in a 4-capacitor SC residue stage reported in [2] and depicted in Fig. 1. The circuit and the way it works will be briefly explained here.

During the first phase, the differential input signal is sampled by capacitors  $C_1$  to  $C_4$  (the differential input signal range is from  $-V_{ref}$  to  $+V_{ref}$ ). At this time, the input signal is also applied to the input of the sub-ADC to obtain the MSB. In the following phase, switching in a DAC is controlled by the MSB and top plates of capacitors  $C_1$  and  $C_3$  are connected to the DAC output. After this operation, the first analog residue at the amplifier output is obtained as follows

$$V_{res1} = 2V_{in} - V_{DAC0} \quad (1)$$

Here, the output of the sub-ADC (in the previous phase) is used to select the DAC output voltage,  $V_{DAC0}$ , such that  $V_{DAC0} = V_{ref+}$ ,  $V_{CM}$ ,  $V_{ref-}$  when the sub-ADC output is 00, 01, 10, respectively. At the end of this phase, the sub-ADC determines the second significant bit. In the sampling phase of the second cycle, the amplifier output is sampled across  $C_1$  and  $C_3$ . Subsequently the amplification happens in the same manner as the previous cycle. In this operation, the reference voltage generated by the DAC is subtracted from the 1<sup>st</sup> residue which is multiplied by two to create the 2<sup>nd</sup> residue voltage at the amplifier output.

$$V_{res2} = 2V_{res1} - V_{DAC1} \quad (2)$$

In order to obtain  $N$ -bit resolution, this procedure is repeated for  $N$  times [2].

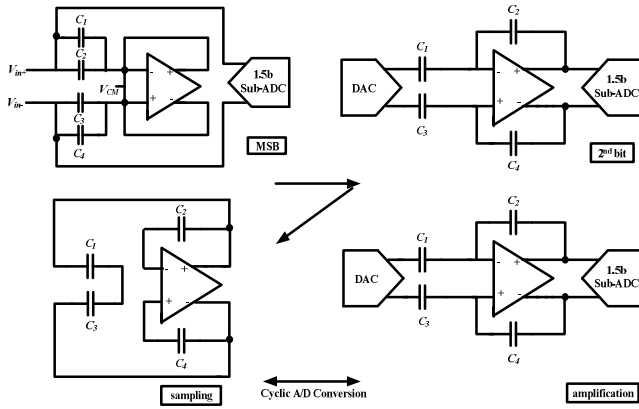


Fig. 1 Phase diagram of a 4-capacitor cyclic ADC

In a cyclic ADC, the power consumption of the operational amplifier is proportional to the size of the capacitors. The size of the unit capacitors is determined either by the required value of  $kT/C$  noise or by the required matching. Typically, for resolutions of 11 bits or higher, if the value imposed by matching is higher than that needed for  $kT/C$  noise, the capacitor size is determined by  $kT/C$  noise requirement while the matching is satisfied using calibration. Low power efficiency is the main problem with the conventional structures of cyclic ADCs; this is mainly because despite the fact that  $kT/C$  noise and accuracy requirement reduces from MSB to LSB, the same analog circuitry is repeatedly employed in all cycles. In the following section, we propose a capacitor-scaling technique in addition to adaptive biasing of the opamp to reduce the power consumption of the opamp.

### III. THE PROPOSED LOW-POWER CYCLIC ADC

#### A. Proposed Architecture

We propose a modified architecture where the effective capacitance of all capacitors is reduced in two steps while the current consumption of the opamp is adaptively scaled down. For each capacitor, we propose using the capacitor array (CA) depicted in Fig. 2.

A suggestive architecture to implement the capacitor scaling technique in cyclic ADC along with the required clocks is demonstrated in Fig. 3. The architecture is similar to the structure of the 4-capacitor cyclic ADC of [2] where each capacitor is replaced with a CA. Nevertheless, the idea can be readily applied to any other cyclic ADC architecture.

Fig. 4 shows the phase diagrams illustrating the operation of the proposed ADC. Through the first conversion cycle for each sample, all switches of CAs are on and thus the capacitance of CA is  $C_{k,u}$ . During the second cycle, by disconnecting  $\phi_1$ , the effective capacitance is set equal to

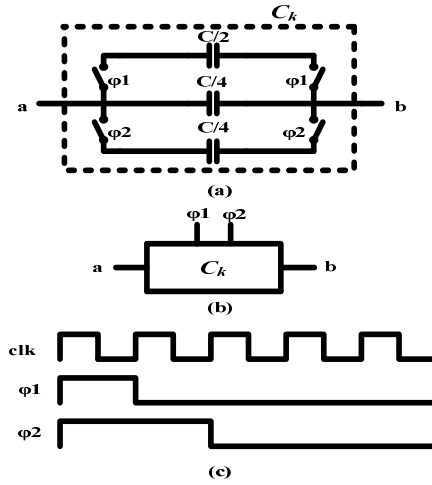


Fig. 2 (a) Capacitor Array (CA), (b) its symbol and (c) timing diagram

$C_{k,u}/2$  and for the rest of the cycles, by disconnecting all  $\phi_1$ 's and  $\phi_2$ 's, it is reduced to  $C_{k,u}/4$  (see also Fig.2). Since the current consumption of the opamp, is adaptively scaled down with the value of the unit capacitor (controlled using the same control signal of  $\phi_2$ ), considerable power is saved. The values of the unit capacitor as well as the current consumption of the opamp in different cycles are summarized in Table. I where  $I_p$  is the required value for the opamp current based on proposed design.

TABLE I. THE VALUES OF THE UNIT CAPACITOR AND THE CURRENT CONSUMPTION OF THE OPAMP

Cycle #	1	2	3	4 to $N$
Unit Capacitor	$C$	$C/2$	$C/4$	$C/4$
Opamp Current	$I_p$	$I_p$	$I_p/2$	$I_p/2$

#### B. Advantages

The maximum total capacitance that needs to be driven by the opamp is seen during the sampling phase of the second cycle (see 2<sup>nd</sup> cycle in Fig. 4). So, the current consumption of the opamp should satisfy the requirement of this cycle. In the proposed architecture, by scaling down the capacitors by a factor of 2 in this cycle the maximum capacitive load of the opamp has been reduced by a factor of 2 (and approximately is equal to the load capacitance of the first cycle) and thus the requirement for the current consumption of the opamp is  $I_{p1}=I_{p2}=I_p$  which is less than  $I_{conv}$  (the current consumption of the conventional circuit). One more time, scaling down the capacitors in the third cycle, reduces the capacitive load of the opamp by a factor of 2; thus the power consumption is reduced by another factor of 2. Therefore, the power consumption of the opamp is reduced by a power-reduction factor (PRF) of

$$PRF = \frac{P_{proposed}}{P_{conventional}} = \frac{I_p}{I_{conv}} \frac{1+1+(N-2)/2}{N} = \frac{I_p}{I_{conv}} \frac{N+2}{2N} \quad (3)$$

For a 12-bit instance, the opamp would consume  $(7/12)I_p/I_{conv}$  times smaller current (corresponding to more than 42% power saving).

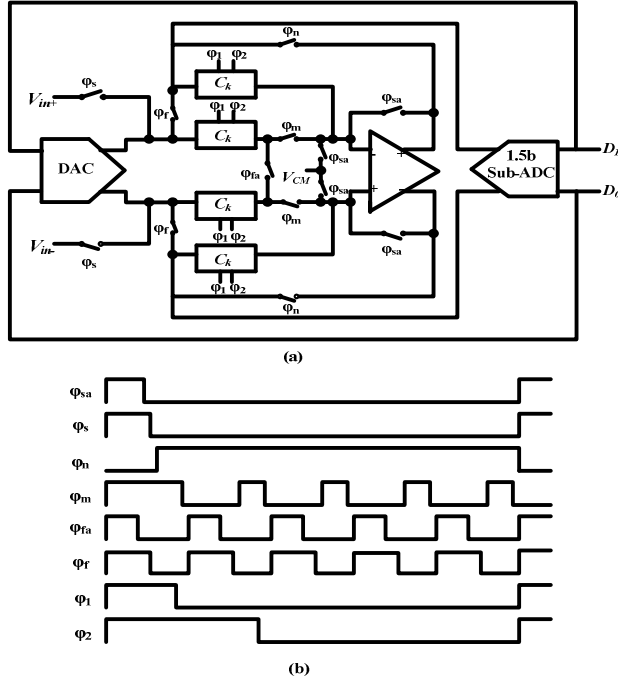


Fig. 3 (a) Schematic of the proposed cyclic ADC and (b) its timing diagram

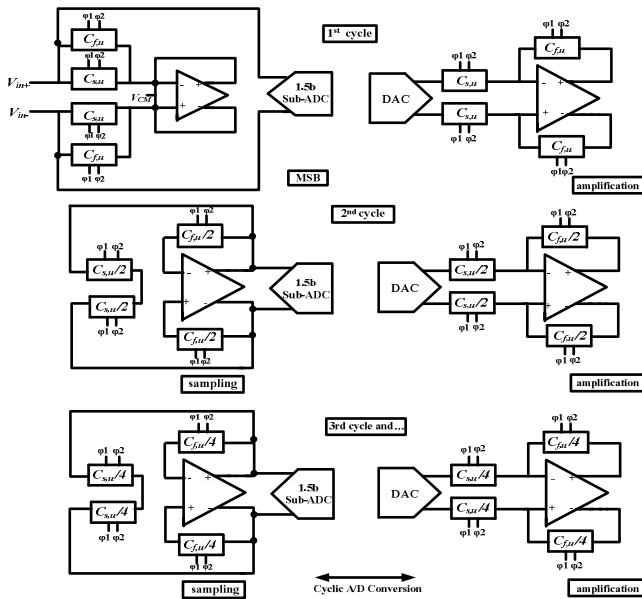


Fig. 4 Schematic of the proposed cyclic ADC in different cycles of operation

#### IV. CIRCUIT IMPLEMENTATION OF THE ADC

In this section, practical implementation considerations of an ADC with the proposed architecture are addressed. The proposed ADC includes one opamp, two comparators, four capacitor arrays and several switches.

#### A. Dynamic Comparator

The comparators form the core of the sub-ADC. Thanks to using redundant-signed digit (RSD) digital correction algorithm, the ADC can tolerate a comparator offset voltage as high as  $\pm V_{ref}/4$ . This allows the use of dynamic comparators reducing the power consumption considerably. Hence, we employ commonly-used ‘Lewis-Gray’ dynamic comparator of [5] in our design.

#### B. Adaptively Biased Opamp

Fig. 5 shows the employed two-stage fully-differential opamp and its adaptive biasing used in this study. Although not shown in this Figure, since SC common-mode feedback circuit (CMFB) increases capacitor loads of the opamp and high-resistivity resistors have been available, a continuous-time CMFB circuit was used. The simulated opamp gain is 86dB, more than sufficient for a 12-bit resolution.

As discussed in the previous section, the value of the bias current of the opamp is halved in the third cycle. The bias circuit implementing this current scaling technique is depicted in Fig. 5(b). When the control signal  $\phi_2$  (the same control signal used to scale down capacitors in the third cycle of the modified ADC), goes low,  $M_{sw}$  is turned off and the currents in all branches are halved. At this time cascode-compensation capacitors in the opamp are also halved.

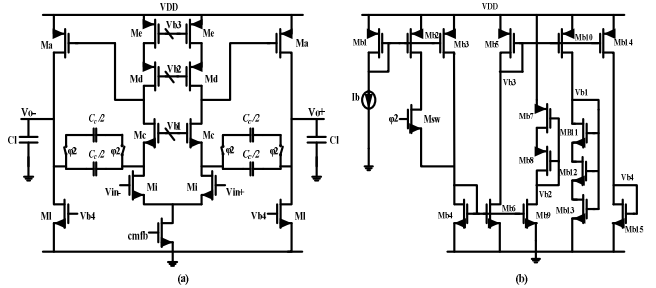


Fig. 5 (a) Schematic of the two stage fully-differential amplifier with (b) adaptive biasing

#### C. Design Issues

In the proposed SC implementation, each CA implies four switches. Charge injection from this switches cause an error, to eliminate this error, these switches are implemented with transmission gate switches with careful switching sequence and also bottom plate sampling technique is applied.

However, in each cycle of the cyclic A/D conversion, the usual errors especially caused by capacitor mismatch and finite open-loop opamp gain, occur and limit the performance of the ADCs with resolution of more than 11 bits. In the proposed cyclic ADC, we can apply on chip error correction circuit just like in conventional structure used in [2], and improve the linearity of the circuit.

#### V. SIMULATION RESULTS

Based on the proposed structure, a 1.8V 12-bit 104kS/s cyclic ADC with a full-scale voltage,  $V_{FS}$ , of 1.2V in a 0.18 $\mu$ m CMOS technology has been designed and simulated using HSpice. Fig. 6 shows the simulated FFT output

spectrum of the ADC for a Nyquist-frequency input. Simulated values of the spurious-free dynamic range (SFDR) and total harmonic distortion (THD) for the proposed structure are 69dB and -65.1dB, respectively, while, these values for simulated conventional ADC are 72.5dB and -65.9dB. Table. II compares the power dissipation for the conventional cyclic ADC and the proposed architecture. The total power dissipation in the proposed cyclic ADC is 240 $\mu$ W compared to 510 $\mu$ W for the traditional cyclic ADC. Therefore, the proposed technique results in 53% reduction in power consumption of the ADC.

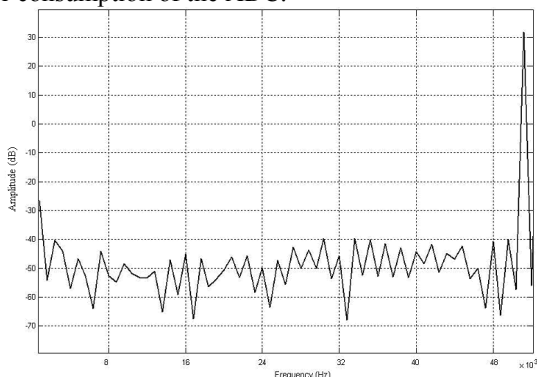


Fig. 6 simulated FFT output spectrum

TABLE II. COMPARISON OF THE POWER DISSIPATION

<i>ADC Architecture</i>	<i>Power consumption</i>	<i>Power saving</i>
<b>Conventional</b>	510 $\mu$ W	0%
<b>Proposed</b>	240 $\mu$ W	53%

## VI. CONCLUSIONS

In cyclic ADCs, noise and accuracy requirements decrease from the most-significant bit (MSB) to the least-significant bit (LSB) cycle, but the invested energy per cycle has been conventionally constant. In this paper, a low-power design technique was proposed where the values of the capacitors for different cycles in digitizing an analog input sample are scaled down. The current consumption of the operational amplifier is adaptively reduced as well. Simulation results of a 1.8V 12-bit 104kS/s ADC in a 0.18 $\mu$ m CMOS technology confirm that applying the technique has reduced the power consumption of the ADC with a factor of more than 2.1. Simulated values of the SFDR and THD were 69dB and -65.1dB, respectively. Although the technique has been applied to specific 4-capacitor architecture, it can be readily applied to various architectures of cyclic ADCs.

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