Design and Optimization of LNA Topologies with Image Rejection Filters

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ABSTRACT: An important problem in designing RFIC in CMOS technology is the parasitic elements of passive and active devices that complicate design calculations. This article presents three LNA topologies including cascode, folded cascade, and differential cascode and then introduces image rejection filters for low-side and high-side injection. Then, a new method for design and optimization of the circuits based on a Pareto-based multiobjective genetic algorithm is proposed. A set of optimum device values and dimensions that best match design specifications are obtained. The optimization method is layout aware, parasitic aware, and simulation based. Circuit simulations are carried out based on TSMC 0.18 μm CMOS technology by using Hspice. © 2010 Wiley Periodicals, Inc. Int J RF and Microwave CAE 20: 286–297, 2010.

Keywords: image rejection filter; LNA; multiobjective genetic algorithm; optimization

I. INTRODUCTION

The advancement of RF systems has increased demand for smaller, lighter, and cheaper devices. The opportunity of mixed analog and digital integration, high-level integration, and low-cost fabrication, has made CMOS a competitive technology for realization of RF circuits [1].

The parasitic elements of transistors and passive devices, particularly integrated inductors, need to be considered in RF integrated design in CMOS technology. These parasitic elements significantly decrease the efficiency of RF circuits. Hence, it is essential to use proper computer aided design tools with design and optimization capabilities that can take into account all parasitic elements of active and passive devices [2–6].

This article presents a new method for designing RF circuits. The method performs a limited but effective search within design boundaries. The efficiency of this method is evaluated by using benchmark problems. The results are compared against those of other multiobjective genetic algorithms.

The method simulates circuits and evaluates the results iteratively until a desired solution is found. The features of the presented method include its layout and parasitic awareness that take into account both component layouts and parasitic elements in the design process.

Three LNA structures including cascode, folded cascade, and differential cascode with and without image rejection (IR) filters are designed and optimized by our optimization method.

The article is organized as follows: Section II describes design methods and noise calculation for LNAs. Section III presents the structure and function of the proposed LNA circuits with IR filters. Modeling of integrated devices considering parasitic elements are explained in Section IV. Section V describes the proposed optimization algorithm. Section VI gives some benchmark test problems that are used to demonstrate the efficiency and effectiveness of the optimization algorithm. Section VII presents the results associated with the design and optimization of the LNA circuits. Finally, concluding remarks are given in Section VIII.

II. DESIGN METHOD AND NOISE CALCULATION FOR LNA

An LNA is the first stage of a receiver and according to (1) its noise figure (NF) directly influences the overall NF of the receiver. The total NF of the receiver can be calculated as follows:

$$\mathrm{NF} = \mathrm{NF}_1 + \frac{\mathrm{NF}_2 - 1}{G_1} + \frac{\mathrm{NF}_3 - 1}{G_1.G_2} + \ldots + \frac{\mathrm{NF}_n - 1}{G_1.G_2 \ldots G_n} \quad (1)$$

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where NF_i and G_i are NF and gain of ith stage of the receiver, respectively. It is therefore essential to reduce the NF of LNA. The required gain can be found from the noise value and the receiver IP3. Higher LNA gains can reduce the effect of the noise associated with other stages of circuit on input, but also decrease IP3.

The input impedance of LNA is usually 50 Ω to achieve power matching. The output impedance of LNA for the receiver with off-chip IR filter is also 50 Ω. However, for the on-chip IR filter or homodyne receivers, the output impedance should be matched with the input impedance of the next stage, and therefore need not be always 50 Ω.

The design objectives of LNA are the impedance matching for maximum gain and minimum NF. To achieve these desirable conditions, two inductors are placed in series with the gate and source of the transistor as shown in Figure 1a. Ignoring the resistance of the inductors and C_{g_d} capacitor, NF can be calculated as follows [7]:

$$\mathrm{NF} = 1 + \frac{1}{g_{\mathrm{m}}^2 R_{\mathrm{s}}} \cdot \times \left\{ \gamma . g_{\mathrm{d0}} . \left\{ \begin{array}{l} \left[1 + S^2 C_{\mathrm{gs}} (L_{\mathrm{g}} + L_{\mathrm{s}}) (1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}}) \right]^2 \\ - (\mathrm{SC}_{\mathrm{gs}} R_{\mathrm{s}})^2 (1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}})^2 \end{array} \right\} - \frac{\alpha\delta}{5} (1 - |c|^2) g_{\mathrm{m}} (\mathrm{SC}_{\mathrm{gs}})^2 (R_{\mathrm{s}}^2 - \mathrm{SL}_g^2) \right\} \tag{2}$$

where γ, thermal noise constant, is 2/3 for the long channel transistor and increases to 2 for the short channel transistor. g_{d0} is the drain-source conductance at zero drain-source voltage. For the long channel transistor, g_{d0} is equal to g_{m} and generally $\alpha = g_{\mathrm{m}}/g_{\mathrm{d0}}$. δ, gate noise constant, is 4/3 for the long channel and increases to 4 for the short channel transistors.

The channel noise current (i_{nd}) and gate-induced noise current (i_{ng}) are correlated and defined by:

$$c = \frac{\overline{i_{\mathrm{ng}} . i_{\mathrm{nd}}^*}}{\sqrt{\overline{i_{\mathrm{ng}}^2}} \sqrt{\overline{i_{\mathrm{nd}}^2}}} \tag{3}$$

Correlation coefficient for the long channel transistor is 0.395j and is purely imaginary because the noise sources affect each other through the capacitive coupling of gate and channel.

If we used (4) for NF, the noise parameters are defined by:

$$\mathrm{NF} = \mathrm{NF}_{\mathrm{min}} + \frac{R_{\mathrm{n}} |Y_{\mathrm{s}} - Y_{\mathrm{opt}}|}{G_{\mathrm{s}}} \tag{4}$$

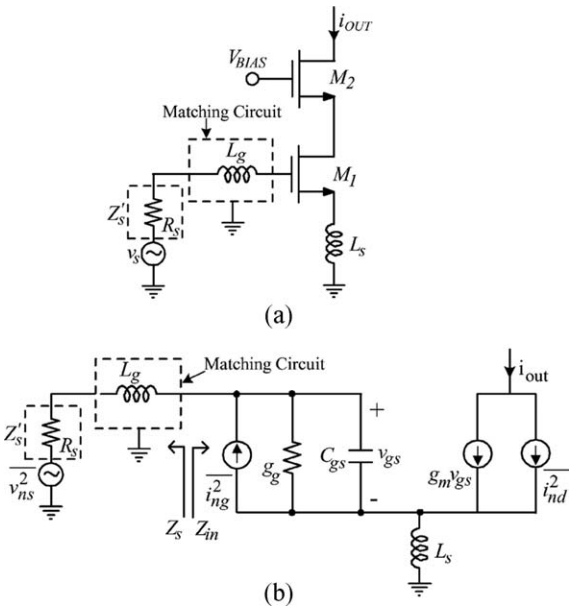

Figure 1 (a) Cascode LNA and (b) small-signal equivalent circuit for the cascode LNA.

$$R_{\mathrm{n}} = R_{\mathrm{n}}^0 = \frac{\gamma}{\alpha} . \frac{1}{g_{\mathrm{m}}} \tag{5}$$

$$Z_{\mathrm{opt}} = Z_{\mathrm{opt}}^0 - \mathrm{SL}_{\mathrm{s}} \tag{6}$$

$$\mathrm{NF}_{\mathrm{min}} = \mathrm{NF}_{\mathrm{min}}^0 = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{7}$$

where R_{n} is the noise resistance, Y_{opt} and Z_{opt} are the optimum noise admittance and impedance, and $\mathrm{NF}_{\mathrm{min}}$ is the minimum noise factor. In these equations, the upper case zero indicates the noise parameters for the circuit without using an inductor in the source. The value of Z_{opt}^0 in (6) is determined as follows:

$$Z_{\mathrm{opt}}^0 = \frac{1}{Y_{\mathrm{opt}}^0} = \frac{\alpha \sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j(1 + \alpha|c| \sqrt{\frac{\delta}{5\gamma}})}{\omega C_{\mathrm{gs}} \left\{ \frac{\alpha^2 \delta}{5\gamma(1-|c|^2)} + (1 + \alpha|c| \sqrt{\frac{\delta}{5\gamma}})^2 \right\}} \tag{8}$$

According to (6), it can be seen that Z_{opt} can be affected by L_{s} without changing NF and noise resistance. Referring to Figure 1b, the input impedance is as follows:

$$Z_{\mathrm{in}} = \mathrm{SL}_{\mathrm{s}} + \frac{1}{\mathrm{SC}_{\mathrm{gs}}} + \frac{g_{\mathrm{m}} L_{\mathrm{s}}}{C_{\mathrm{gs}}} = \mathrm{SL}_s + \frac{1}{\mathrm{SC}_{\mathrm{gs}}} + \omega_{\mathrm{T}} L_{\mathrm{s}} \tag{9}$$

In this equation, the input impedance has a real component which depends on L_{s} and can cause Z_{opt} to approach the conjugate value of Z_{s} without changing NF and R_{n}. In other word, optimized matching for higher gain and minimum NF can be achieved simultaneously. Hence, we have the following equations:

$$\mathrm{Re}[Z_{\mathrm{opt}}] = \mathrm{Re}[Z_{\mathrm{s}}] \tag{10}$$

$$\mathrm{Im}[Z_{opt}] = -\mathrm{Im}[Z_{in}] \quad (11)$$

$$\mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s] \quad (12)$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s] \quad (13)$$

In these equations, Z_s is the source impedance and can be expressed as follows:

$$Z_s = R_s + \mathrm{SL}_g \quad (14)$$

In common source or cascode amplifier design, first we select C_{gs} (related to the width of the transistor) to establish (10). Then, L_s is selected based on the value of C_{gs} according to (11). With the selected value of C_{gs} and L_s, V_{gs} can be determined using (12). Finally, L_g is calculated using (13).

From (9) and (12), we can find:

$$R_s = \frac{g_m}{C_{gs}}.L_s = \mathrm{Re}[Z_{opt}] \quad (15)$$

According to (8) and (15), in a 50 Ω input match, for a low power or a small dimension transistor (low value of g_m), or also for low-frequency operation (high value of C_{gs}), the value of L_s becomes very large. In this situation, (9) becomes inadequate because the value of C_{gd} becomes significant and NF is also increased. Nguyen et al. [7] overcome this issue by using an extra capacitor C_{ex} between the gate and the source of the transistor. In this case, all design equations are re-established by substitution ($C_{gs} + C_{ex}$) for C_{gs}. Hence, with a proper value of C_{ex}, to determine the bias current, suitable value of L_s can be found. In this way, the maximum power dissipation of LNA can be also considered in the circuit design.

III. THREE LNA ARCHITECTURES WITH IR FILTER

The conventional architecture of RF receivers is the heterodyne structure, which gives high stability and needed efficiency. In heterodyne receivers, one dilemma is unwanted image frequency that must be attenuated. Usually, the unwanted image frequency is suppressed by off-chip SAW filters. However, these filters are large and costly, and incompatible with integration. To address these issues, research is being carried out to develop on-chip integrated filters. Attenuating the unwanted image frequency can be done by means of IR filter or IR architectures [8–12].

In this article, three LNA structures including cascode, folded cascade, and differential cascode are presented, and then IR filters are added to them. These circuits can be used for two conditions where the image frequency is smaller or greater than the desired RF frequency (low-side and high-side injection) [13].

A. Cascode

The cascode topology is one of the most popular LNA architectures, which has wide bandwidth and higher reverse isolation. Hence, it provides more stability than a common source amplifier. High isolation causes less local oscillator leakage to input and hence to antenna.

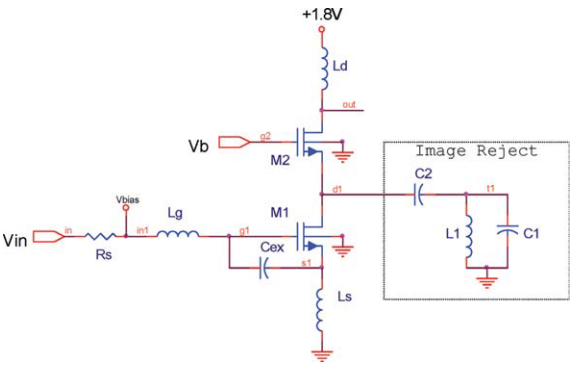

Figure 2 Cascode LNA with an image rejection filter. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

Figure 2 displays the LNA with a cascode topology and an added third-order passive notch IR filter. The input elements of this circuit are designed as explained in Section II. In this topology, inductor L_d resonates with the output capacitors for maximum gain at desired frequency.

The output impedance of M1 is very high (infinite) for the desired frequency and very low (zero) for the image frequency. Therefore, its elements can be calculated as follows:

$$f_{im} = \frac{1}{2\pi\sqrt{L_1(C_1 + C_2)}} \quad (16)$$

$$f_{wanted} = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (17)$$

It should be noted that the image frequency in this design is less than the frequency of RF desired channel. Therefore, the frequency of the local oscillator is less than the received RF frequency (low-side injection) [8]. Considering IEEE 802.11a, the minimum IR ratio is 30 dB. This isolation can be realized by one or two filters.

B. Differential Cascode

Figure 3a shows the differential cascode LNA circuit. The circuit has several advantages because of the high IP2 of the differential amplifier that is suitable for inclusion in homodyne receivers, as well as lowering the common noise of the circuit [14].

A double-ended output can be connected directly to a double balance mixer. It should be noted that ground and biasing connections cause un-negligible parasitic inductors due to bond wires. These inductors need to be considered in the circuit design or to be suppressed by using several parallel connections. In differential topology, the center of the circuit is grounded and all parasitic effects are neglected. L_s and C_s resonate in operating frequency rejecting more common mode noise.

Figure 3a presents the differential cascode LNA with an added IR filter. The differential half-circuit of filter is

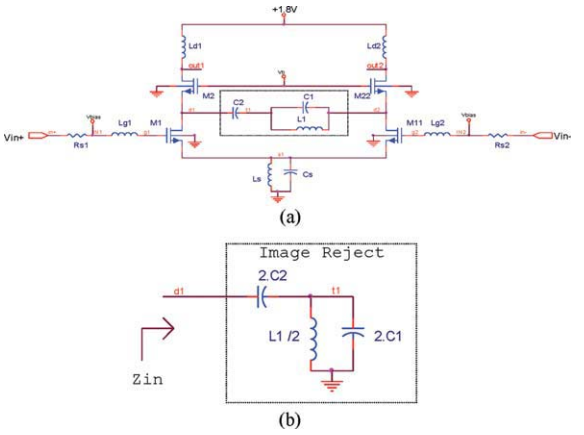

Figure 3 (a) Differential cascode LNA with an image rejection filter and (b) the differential half-circuit of the image rejection filter. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

shown by Figure 3b. The input impedance of filter must be infinite in the desired frequency and zero in the image frequency. Similarly, the value of circuit elements can be calculated using (16) and (17).

C. Folded Cascode

The folded cascade LNA circuit is more convenient for low-voltage operation because the number of stacked transistors between supply voltage and ground is limited. In the folded cascade LNA circuit, shown in Figure 4a, the input elements are designed for minimum noise and impedance matching of a specific power. Inductor L_d resonates with the parasitic capacitors at the drain of M1 in the desired frequency, and helps to suppress the noise of the common gate at output and avoids the signal loss into the silicon substrate [8]. L_o resonates with the output capacitors to increase the voltage gain.

The novelty of this work includes adding an IR filter to the folded cascode LNA circuit as presented in Figure 4b. The inductors L_1, L_2, and C_1 are designed to reject image frequency. The values of these elements are calculated such that the filter becomes short at the image frequency and open at the desired frequency as follows:

$$f_{\text{image}} = \frac{1}{2\pi.\sqrt{L_1.C_1}} \tag{18}$$

$$f_{\text{wanted}} = \frac{1}{2\pi.\sqrt{(L_1+L_2).C_1}} \tag{19}$$

As can be seen, the image frequency is larger than the operational frequency for the receivers whose local oscillator frequency is larger than the desired RF input frequency (high-side injection).

IV. RF MODELING

For analysis of RF circuits in very high frequencies, mathematical models that take into account all parasitic elements need to be used. These models are usually determined by physics of devices, measurement, or electromagnetic analysis. In this section, RF modeling in 0.18 μm CMOS TSMC technology is reviewed. The described models are matched for up to 20 GHz [15].

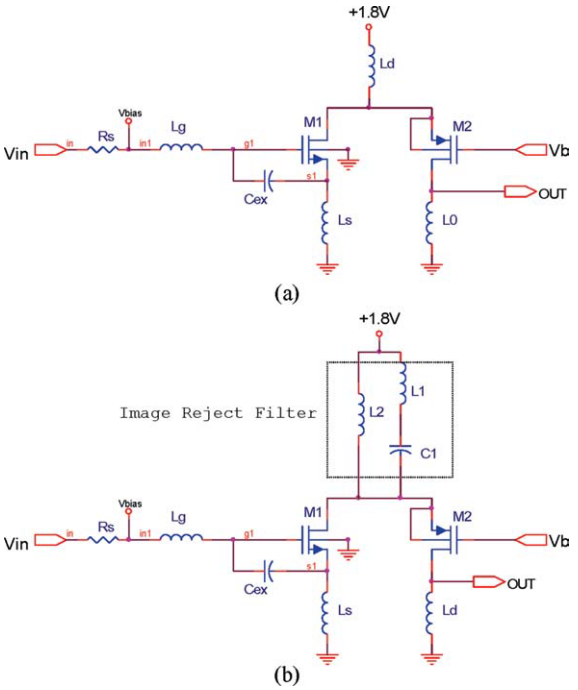

Figure 4 (a) Folded cascode LNA and (b) folded cascode LNA with an image rejection filter. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

High-frequency modeling of MOS transistors is achieved by adding the parasitic elements to the typical transistor model (BSIM3V3) as shown in Figure 5.

As can be seen from the figure, the parasitic elements are added to an ideal transistor, and the entire circuit is used to represent a real transistor.

The spiral integrated inductors are realized in higher metal layer (sixth layer) as shown in Figure 6a. Figure 6b

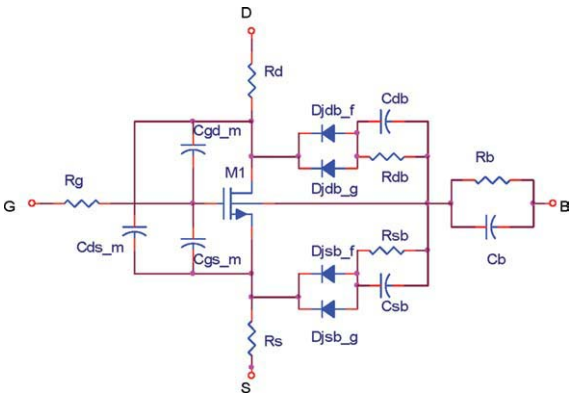

Figure 5 Equivalent RF-circuit of an nMOS transistor. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

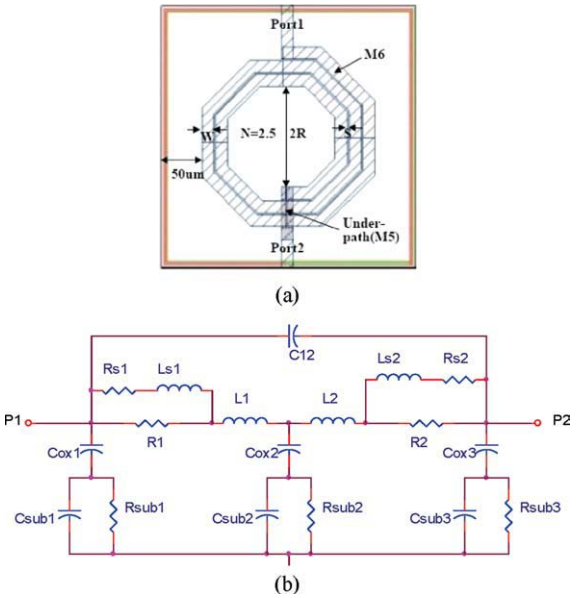

Figure 6 (a) Spiral inductor and (b) equivalent circuit of the spiral inductor. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

represents the parasitic elements of a nonideal inductor. The inductor losses are mainly due to inductors metal type, skin effect, leakage effect, the parasitic capacitances between spirals, the parasitic capacitances between inductor and substrate, and losses due to eddy current.

In the presented model, L_i is the value of inductor, R_i is the resistance of the inductor, R_{si} and L_{si} are the resistance and inductance of skin effect, C_{oxi} is the capacitor between the inductor and the substrate, R_{subi} and C_{subi} are the resistance and the capacitance due to the losses of the substrate, and C_{12} is the coupling capacitance between the ports.

In manufacturing processes, a metal layer is used for realizing the capacitors. The capacitors are formed between this metal layer and another metal layer above this layer. The capacitors can be made using two methods: with and without a shield layer. The shield layer is another metal layer that is connected to ground.

The capacitor without the shield layer is modeled by the circuit shown in Figure 7a. In this model, C_{mim} is the essential capacitor and the other elements are parasitic elements. R_{top} and R_{bot} are the resistances and L_{top} and L_{bot} are the inductances due to upper and lower electrodes. C_{ox} is the parasitic capacitor that exists between the lower electrode and the shield layer or the substrate. For the case with the shield layer, the elements R_{sub} and C_{sub} that are due to the substrate loss are neglected (Fig. 7b).

V. OPTIMIZATION WITH MULTIOBJECTIVE DISTRIBUTED PARETO-BASED GENETIC ALGORITHM

We employ a new multiobjective optimization algorithm named distributed Pareto-based genetic algorithm (DPGA) developed for RF circuit design. The initial version of this algorithm [16] was used for optimization of analog circuit design. The authors then developed a new version of the algorithm [17] that employs clustering to limit the number of members and maintain population diversity and distribution of Pareto solutions. Figure 8 illustrates the flowchart diagram description of the implemented genetic algorithm. As can be seen from the figure, the initial population is randomly selected. Next, in each iteration, the cost function is calculated and the best members are stored in an external set including Pareto solutions. Then, dominated members in Pareto front are replaced by dominant member.

To produce the next generation, a member of the current population is combined with a member of the Pareto set. The algorithm is implemented with 30 members each including information that is related to the input parameters of the circuit. There exist six output parameters, and the algorithm is executed for 150 generations. In the following, different parts of the algorithm are explained.

A. Calculating Cost Functions

The input parameters of the circuit consist of the number of turns and the diameter of the circuit inductors, the number of fingers of transistors with fixed $\frac{W}{L} = \frac{8\mu m}{0.18\mu m}$ dimension, dimension of capacitors, and bias voltages. These parameters are specified and stored into the input file (.sp). Next, Hspice is run and from the generated output file (.lis) S21, S11, S22, NF, and power consumption are extracted. The chip area is separately calculated using the dimension of components. Figure 9 displays the block diagram description of the cost function calculation procedure.

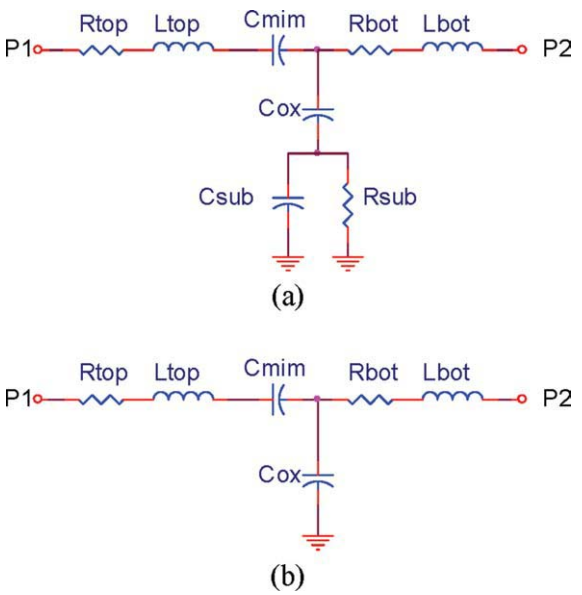

Figure 7 Equivalent circuit of a MIM capacitor (a) without shield and (b) with grounded shield. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

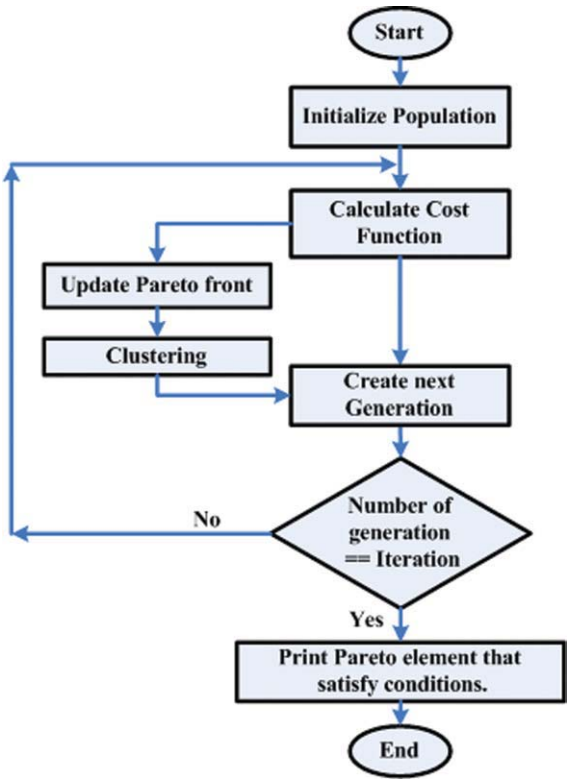

Figure 8 Description of the implemented genetic algorithm. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

In this stage, if a transistor is not in the active region, a large negative score (penalty) is assigned to it, so that the transistor is eliminated in the future generations.

B. Updating Pareto Front

After the calculation of the cost function in the next generation, the new members are compared against the members of the Pareto front. The new members that are found to be dominant to the members of the Pareto front replace those Pareto front members.

C. Producing Next Generation

As shown in Figure 10, to implement elitism, the best member produced by each cost function is directly allowed into the next generation to ensure that the quality of solutions is not diminished (six members).

To produce the rest of members, one member from the current population and one member from the Pareto front are selected. After crossover and mutation, these two members create a new member of next generation. The selection from the members of the current population occurs using the roulette wheel method based on cost function switching for four times (totally 24 members).

The selection from the Pareto front occurs using the roulette wheel method based on crowded functions. For each member of the Pareto front, a crowded function is defined as follows.

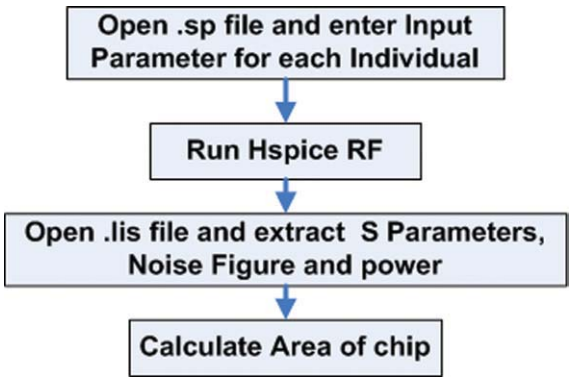

Figure 9 Cost function calculation procedure. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

d_{ij} is defined as the distance between the members i and j, which is the normalized Euclidian distance [18]:

$$d_{ij} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(\frac{p_{ik}-p_{jk}}{p_k^u - p_k^l}\right)^2} \tag{20}$$

d_{ij} is obtained from the summation of the squared normalized distances of input and output parameters of each member. N is the total number of input and output parameters, and p_k^u and p_k^l are the maximum and minimum values of the kth parameter.

S_{ij} is defined as the sharing function of member i and member j:

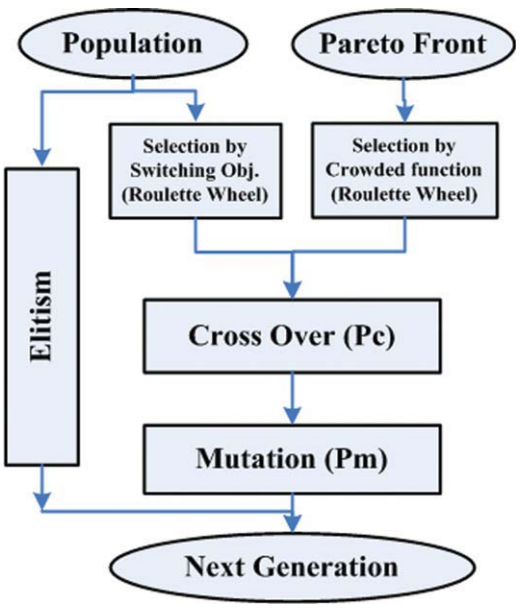

Figure 10 Description of the method that produces the next generation. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

TABLE I Test Function for Comparison Study

Function	N	Domain	Objective Functions
ZDT6	100	[0, 1]	$f_1(X) = 1 - e^{-4x_1}\sin^6(6\pi x_1)$ $g(X) = 1 + (n-1)\left[\frac{\sum_{i=2}^{n} x_i}{n-1}\right]^{0.25}$ $f_2(X) = g(X).\left[1 - \left(\frac{f_1(X)}{g(X)}\right)^2\right]$
KUR	100	[−1000, 1000]	$f_1(X) = \sum_{i=1}^{n-1}(-10e^{-0.2\sqrt{x_i^2 + x_{i+1}^2}})$ $f_2(X) = \sum_{i=1}^{n}\left[\lvert x_i\rvert^{0.8} + \sin^3(x_i)\right]$
SPH-2	100	[−1000, 1000]	$f_1(X) = (x_1 - 1)^2 + \sum_{i=2}^{n} x_i^2$ $f_2(X) = x_1^2 + (x_2 - 1)^2 + \sum_{i=3}^{n} x_i^2$

N is the number of parameters.

$$S_{ij} = \begin{cases} 1 - \left(\frac{d_{ij}}{\delta_{\text{share}}}\right)^2 & \text{if} \quad d_{ij} < \delta_{\text{share}} \\ 0 & \text{otherwise} \end{cases} \tag{21}$$

in which $\delta_{\text{share}} = 0.1$. This value for sharing radius (δ_{share}) has been determined as described in the following. If D is the diameter of the space representing the input parameters, the radius of neighborhood is selected in such a way to have N_{ind} spheres in the whole space (N_{ind} is the number of population members). This means that if the population members are distributed uniformly in the entire space, their sharing function would be zero.

For N_{Par} input variables, the space would be N_{Par} dimensional and the volume of a sphere would be proportional to ${\delta_{\text{share}}}^{N_{\text{Par}}}$. We will thus have:

$$k.\left(\frac{D}{2}\right)^{N_{\text{Par}}} = N_{\text{ind}}.k.{\delta_{\text{share}}}^{N_{\text{Par}}} \tag{22}$$

in which k is a constant for calculating of the value of sphere. Then we have:

$$\delta_{\text{share}} = \frac{D}{2.\sqrt[N_{\text{Par}}]{N_{\text{ind}}}} \tag{23}$$

in which maximum value of D is equal to one because all values are normalized. However, if the diameter of the population members is taken into consideration, D will become equal to the maximum distance between two existing members and thus will usually be less than one. In this case, D can be selected within the interval 1/4 to 1/2. For instance, when the population contains 30 members, and the number of input parameters is 10, δ_{share} becomes $0.36D$, which is therefore assigned as 0.1.

The crowded function of member i is calculated as follows:

$$C_i = \sum_{j=1}^{N_p} S_{ij} \tag{24}$$

where N_p is the number of members of the Pareto front. The selection of members in the Pareto front is performed is such a way to minimize C_i.

D. Clustering

After updating Pareto-front, clustering is performed and from the members of the Pareto front that are within the radius of δ_{Clust}, the oldest member is kept and the rest are discarded. By trial and error, it is shown that 0.1 δ_{share} is opportune for δ_{Clust}.

VI. BENCHMARK PROBLEMS

To test the performance of the developed algorithm, a comparative study with three other algorithms, SPEA2

TABLE II Comparison Between the Algorithms After 100,000 Fitness Evaluations

100,000 Evaluations	SPH-2	KUR	ZDT6
PESA	[1, 0]	[0, 0]	[0.0008, 1]
NSGA2	[1, 0]	[0.64, 0]	[0.0003, 1]
SPEA2	[1, 0]	[0.67, 0]	[0.0007, 1]

TABLE III Comparison Between the Algorithms After 1,000,000 Fitness Evaluations

1000,000 Evaluations	SPH-2	KUR	ZDT6
PESA	[1, 0]	[1, 0]	[0.13, 0.003]
NSGA2	[1, 0]	[1, 0]	[0.1, 0.09]
SPEA2	[0.99, 0]	[1, 0]	[0.18, 0.09]

[19], NSGA-II [20], and PESA [21] is carried out. The three problems presented in Table I are used [19]. For each problem, three runs are carried out to facilitate an appropriate statistical comparison with the stated algorithms.

In the continuous test functions, different difficulties aroused. We enhanced the difficulty of each problem by taking 100 decision variables in each case. For the Sphere Model (SPH-m) and Kursawe's function (KUR), we chose large domains to test the algorithm's ability to locate the Pareto-optimal set in a large objective space.

The function SPH-m is a multiobjective Sphere Model, a symmetric unimodal function, where the isosurfaces are given by hyperspheres. ''m'' is the number of function.

The sphere model has been subject to intensive theoretical and empirical investigations with evolution strategies, especially in the context of self-adaptation. Here, a SPH-2 (two objectives instance) is considered.

Zitzler, Deb, and Thiele's T6, here referred to as ZDT6, is also unimodal and has a nonuniformly distributed objective space, both orthogonal and lateral to the Pareto-optimal front. It is proposed to test the algorithm's ability to find a good distribution of points even in this case.

Kursawe's function has a multimodal function in one component and pair-wise interactions among the variables in the other components. The Pareto-optimal front is not connected and has an isolated point as well as concave and convex regions [19].

For comparison purposes, the results obtained by Zitzler [22] from 30 runs are used. In these runs, Zitzler implemented the PESA, NSGA-II, and SPEA2 algorithms. The comparison was made by using a statistical analysis suggested by Zitzler and Thiele [19]. In this metric, when the algorithms are compared, two numbers are obtained for each algorithm. The first number represents the percentage of the Pareto frontier, in which the algorithm is not beaten by the others; the second number represents the percentage of the Pareto frontier on which the algorithm beats all the others. Tables II and III show the average results obtained when the DPGA algorithm is compared with the other three algorithms using this metric for 90 comparisons (each of our three results compared with 30 results of Zitzler). Size of population is 100 and Table II gives the outcome of 1000 generations (100,000 fitness evaluations) whilst Table III shows the result of 10,000 generations.

According to Table II, the proposed method converges faster than the other algorithms for SPH-2 and KUR problems. In SPH-2, the Pareto members that are earned by our algorithm dominate some answers from other algorithms, but there is no member in other algorithms that can dominate any member of our algorithm answers.

In KUR problem, 64–67% of Pareto members which are earned by our algorithm dominate some answers from other algorithms and there is no member in other algorithms that can dominate any member of the answers of our algorithm.

In these problems, when one input is variable and others are constant, the KUR and SPH-2 functions have only one minimum (Fig. 11a) but ZDT6 contains many local minimums (Fig. 11b). Therefore, the convergence property of our algorithm will become poor. However, according to Table III, responses attained from the presented algorithm meet final answers if the number of generation increases and the algorithm demonstrates more

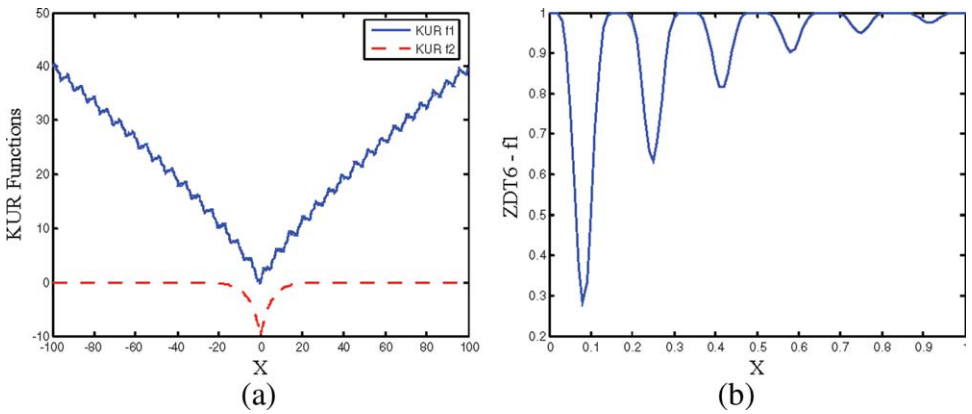

Figure 11 (a) $f_1(x)$ of ZDT6 function (b) KUR functions. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

TABLE IV Design Parameters and Ranges

Parameter	Min.	Max.	Bits
2R-inductor	40 μm	120 μm	8
N-inductor	1	5	4
L = W-capacitor	5 μm	100 μm	8
NoF-transistor	1	64	6

NoF is the number of finger.

effective performance compared to the conventional methods.

Clearly, there is a smooth relationship between design parameters and performance parameters in the design of analog integrated circuits. This means that if an input parameter (e.g., the size of a transistor or the value of a passive element) varies smoothly, the related output parameter has only one optimum point. Consequently, our proposed algorithm has a significant increase in the convergence rate, compared to the conventional algorithms. Our method contains some complexity in producing the new generations. Although the production time of each generation adds to the required time for simulating individuals in the next generation, the algorithm reveals considerable improvement in the convergence rate. This is appropriate for the problems whose simulations require long execution times.

In analog circuit design, the relation between input parameters and output parameters such as gain, bandwidth, power, and area are typically smooth and if one parameter is varied, typically output parameters would not oscillate. Consequently, our algorithm proves to be appropriate for design of analog circuits.

VII. OPTIMIZATION OF LNA TOPOLOGIES

In this section, the circuits are designed and optimized by the method explained in Section V. All parasitic elements according to section IV are considered in the optimization of the circuits.

TABLE V Optimization Results of the Cascode LNA at 5.7 GHz Frequency

	Ans. 1	Ans. 2	Ans. 3	Ans. 4
N-Ld	3.5	3.75	3.5	3.75
R-Ld (μm)	73	74	72	75
N-Lg	3.0	2.75	2.5	3.0
R-Lg (μm)	85	74	65	77
N-Ls	1.25	1.0	1.0	1.0
R-Ls (μm)	43	47	62	41
Vin(DC) (V)	0.68	0.67	0.63	0.7
Vb (V)	1.19	1.14	1.23	1.09
NF-M1	16	23	34	18
NF-M2	29	20	25	17
S21 (dB)	13.8	14.3	12.7	14.4
S11 (dB)	−18.7	−15.3	−13.9	−14.1
S22 (dB)	−17.4	−17.4	−12.8	−15.2
NF (dB)	2.88	2.30	2.13	2.66
Power (mW)	9.0	11.4	11.7	11.1
Area (mm^2)	0.39	0.37	0.36	0.38

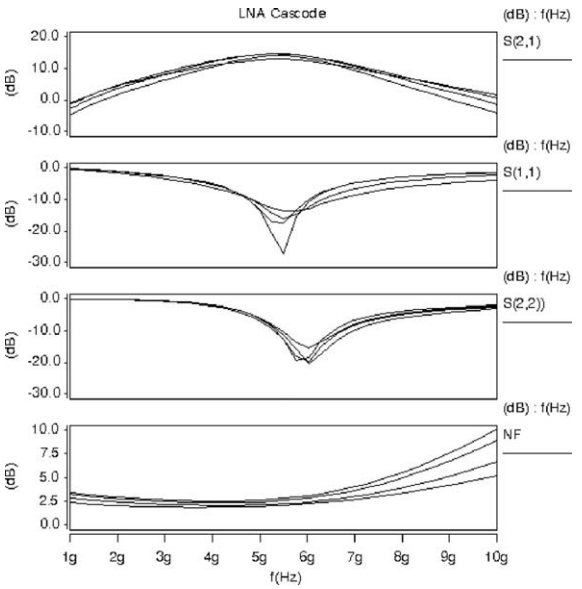

Figure 12 S parameters and NF of the best results of the LNA cascade.

In our circuit optimization, the design parameters are number of turns and diameter of inductors, number of transistor fingers, dimension of capacitors, and bias voltages. The dynamic range of these parameters and the bit number for their coding are represented in Table IV. The optimization algorithm searches within the given dynamic ranges.

The circuits described in Section III are designed and optimized by the optimization algorithm (DPGA). Some

TABLE VI Optimization Results of the Cascode LNA with IR Filter at 5.7 GHz Frequency and 1.9 GHz Image Frequency

	Ans. 1	Ans. 2	Ans. 3	Ans. 4
N-Ld	3.25	4	3.25	3.25
R-Ld (μm)	77	64	79	74
N-Lg	1.75	3.5	2.25	1.75
R-Lg (μm)	120	53	100	110
N-Ls	1.0	1.25	1.75	1.0
R-Ls (μm)	51	58	54	52
Vin(DC) (V)	0.68	0.84	0.81	0.67
Vb (V)	1.58	1.44	1.59	1.59
NF-M1	23	13	24	26
NF-M2	42	24	30	44
N-L1	3.0	3.75	3.25	3.0
R-L1 (μm)	79	90	80	82
LC1 (μm)	16	12	14	15
LC2 (μm)	44	34	41	43
S21 (dB)@Freq	14.1	13.5	11.6	14.2
S21(dB)@image	−3.44	−1.5	−2.63	−2.23
S11 (dB)	−16.4	−11.7	−16.4	−15.9
S22 (dB)	−11.7	−25.5	−16.9	−11.9
NF (dB)	2.19	2.84	2.6	2.08
Power (mW)	13.8	18.5	28.3	17.7
Area (mm^2)	0.42	0.36	0.41	0.40

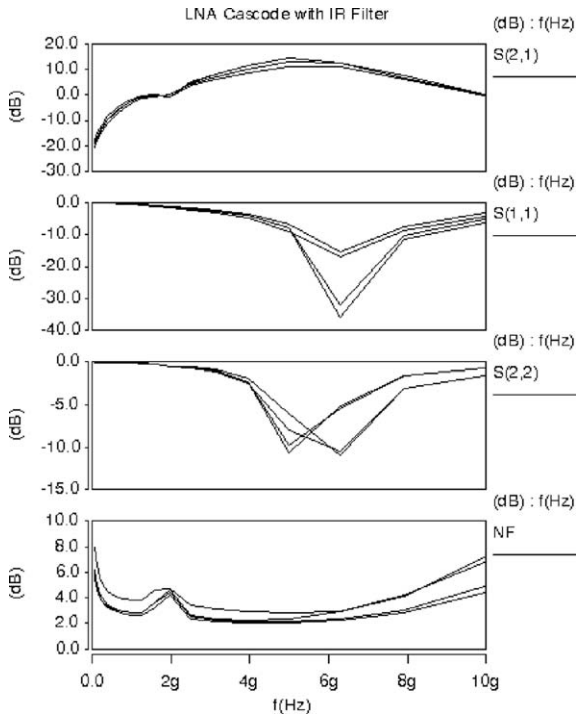

Figure 13 *S* parameters and NF of the best results of the LNA cascode with IR filter.

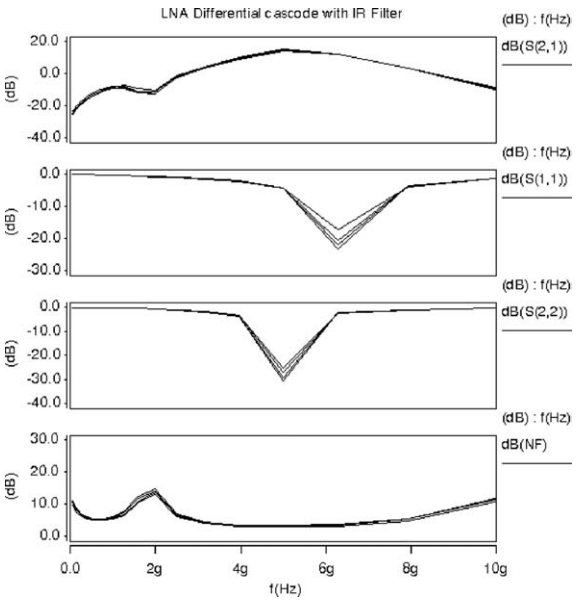

Figure 14 *S* parameters and NF of the best result of the differential cascode LNA with IR filter.

of the best answers of Pareto front are presented. The cascode LNA is optimized for 5.7 GHz. The results that consist of four best answers from the Pareto front are presented in Table V. The *S* parameters of the results are plotted in Figure 12.

The cascode LNA with image reject filter (Fig. 2) is designed and optimized, similarly. In this case, the frequency of LNA is 5.7 GHz and the image frequency is 1.9 GHz. For designing the IR filter, the optimization algorithm proposes the inner radios and the number of turns for L_1. Next, the value of C_1 and C_2 are calculated using (16) and (17). These capacitors are implemented by the MIM square capacitor.

TABLE VII Optimization Results of the Differential Cascode LNA with IR Filter at 5.7 GHz Frequency and 1.9 GHz Image Frequency

	Ans. 1	Ans. 2	Ans. 3	Ans. 4
N-Ld	4.5	4.25	4.25	4.5
R-Ld (μm)	50	56	57	50
N-Lg	3.25	3.25	3.25	3.5
R-Lg (μm)	71	79	79	65
N-Ls	2.75	2.0	2.25	2.75
R-Ls (μm)	79	77	48	80
Vin(DC) (V)	0.72	0.72	0.75	0.71
Vb (V)	1.03	0.99	1.0	1.0
NF-M1	11	9	9	10
NF-M2	37	39	39	36
N-L1	2.5	3.0	3.0	2.5
R-L1	72	78	78	81
LC1	19	15	15	18
LC2=LC3	70	57	56	70
S21 (dB)@Freq	13.8	13.0	13.4	13.3
S21(dB)@image	−11.2	−11.8	−10.2	−12.5
S11 (dB)	−11.2	−14.4	−13.9	−13.1
S22 (dB)	−15.3	−13.8	−14.7	−13.0
NF (dB)	3.07	3.48	3.45	3.32
Power (mW)	14.0	12.2	14.7	12.1
Area (mm^2)	0.44	0.44	0.40	0.44

TABLE VIII Optimization Results of the Folded Cascode LNA with IR Filter at 2.4 GHz Frequency and 4.0 GHz Image Frequency

	Ans. 1	Ans. 2	Ans. 3	Ans. 4
N-Ld	5	4.75	5	4.5
R-Ld (μm)	115	117	114	119
N-Lg	4.25	4.5	4.25	4.0
R-Lg (μm)	90	89	89	107
N-Ls	1.25	1.25	1.25	1.5
R-Ls (μm)	54	50	54	47
Vin(DC) (V)	0.64	0.61	0.65	0.67
Vb (V)	0.80	0.77	0.81	0.79
NF-M1	41	38	45	46
NF-M2	40	46	41	54
N-L1	1.5	1.25	1.5	1.25
R-L1 (μm)	106	108	108	106
N-L2	3.5	1.75	3.0	2.5
R-L2 (μm)	40	113	58	60
LC1 (μm)	34	39	34	39
S21(dB)@Freq	21.4	12.9	12.9	16.2
S21(dB)@Image	−5.4	−18.2	−18.2	−8.4
S11 (dB)	−15.5	−13.7	−14.5	−14.2
S22 (dB)	−21.2	−12.2	−12.6	−14.3
NF (dB)	2.16	3.39	3.38	1.91
Power (mW)	52.0	55.0	54.8	69.4

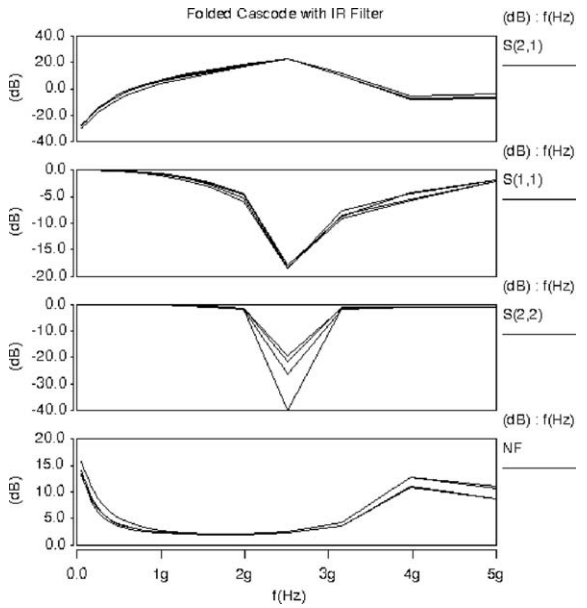

Figure 15 *S* parameters and NF of the best result of the folded cascode LNA with IR filter.

The size of the capacitors is calculated approximately with 1 $fF/(\mu m)^2$ density. The results that consist of four best answers from the Pareto front are presented in Table VI. The *S* parameters of the results are plotted in Figure 13. Table VII contains the optimization results of differential cascode LNA with IR filter with 5.7 GHz frequency and 1.9 GHz image frequency. The IR filter is designed as described previously. Figure 14 shows the NF and *S* parameters of the circuits.

Table VIII contains the optimization results for the folded cascode LNA with the IR filter for the frequency of 2.4 GHz and image frequency of 4.0 GHz. Figure 15 shows the NF and *S* parameters of the circuits. For designing the IR filter, the optimization algorithm proposes the inner radios and the number of turns of L_1.

After that, the value of C_1 and L_2 are calculated using (18) and (19). The size of C_1 is calculated directly and the inner radios and the number of turns of L_2 are found by sweeping the values to minimize error of the inductance value.

VIII. CONCLUSIONS

Design of high-frequency circuits cannot be accurately carried out through hand calculations due to the existence of parasitic elements associated with transistors and inductors. Employing approximate formulas would not produce the desired results giving rise to the use of trial and error in pursuit of the needed solution. This method is however computationally expensive and does not also guarantee the best possible solution.

This article presented a method for designing RF circuits that performs a limited but effective search within design boundaries. The method simulates the circuit and evaluates the results iteratively until the desired solution is found. An important feature of the presented method is its layout and parasitic awareness that take into account of both component layouts and parasitic elements in the design process. Moreover, the method utilizes accurate simulation tools in the design process that helps produce accurate solutions.

More importantly, the proposed method can be used as a generic computer-aided design tool to design various types of RF circuits.

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BIOGRAPHIES

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