ELectronics EXpress

IEICE Electronics Express, Vol.7, No.20, 1592–1596

Ultra-low power BPSK demodulator for bio-implantable chips

Ghazal Nabovati[a)] **and Mohammad Maymandi-Nejad**

Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran

a) *nabovati@stu-mail.um.ac.ir*

Abstract: A novel non-coherent binary phase shift keying (BPSK) demodulator featuring ultra-low power and high data rate is presented for inductively powered biomedical implants. The circuit is designed in the 0.18 μm standard CMOS technology. Simulation results show that at a data transmission rate of 16 Mbps, the power consumption of the circuit is as low as 6.3 μW and 1.96 μW at a supply voltage of 1.8 V and 1 V, respectively. The proposed demodulator tolerates a relatively large frequency shift for the input signal and operates properly in all process corners.

Keywords: bio-implantable, BPSK demodulator, noncoherent detection

Classification: Integrated circuits

References

[1] M. Ghovanloo and K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 2374–2383, 2004.

[2] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. De Juan, J. D. Weiland, and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1487–1497, 2000.

[3] Y. Hu and M. Sawan, "A fully-integrated low-power BPSK demodulator for implantable medical devices," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 52, no. 12, pp. 2552–2562, 2005.

[4] C.-S. A. Gong, M.-T. Shiue, K.-W. Yao, and T.-Y. Chen, "Low-power and area-efficient PSK demodulator for wirelessly powered implantable command receivers," *Electron. Lett.*, vol. 44, no. 14, 2008.

[5] F. Asgarian and A. Sodagar "A High-Data-Rate Low-Power BPSK Demodulator and Clock Recovery Circuit for Implantable Biomedical Devices," *Proc. International IEEE EMBS Conference on Neural Engineering*, May 2009.

[6] S. F. Al-Sarawi, "Low power Schmitt trigger circuit," *Electron. Lett.*, vol. 38, no. 18, Aug. 2002.

DOI: 10.1587/elex.7.1592
Received September 12, 2010
Accepted September 28, 2010
Published October 25, 2010

IEICE Electronics Express, Vol.7, No.20, 1592–1596

1 Introduction

The inductive coupling between two closely spaced coils is one of the most common methods for wireless power and data transfer from an external device to a bio-implanted chip. However, design of an efficient data transfer link in such applications is a nontrivial task. This is mostly due to very tight design parameters, e.g., limited carrier frequency, low power consumption, and high data transfer rate [1]. In order to satisfy design issues of implantable devices, various digital modulation techniques have been reported in the literature, namely: amplitude shift keying (ASK) [2], frequency shift keying (FSK) [1], and binary phase shift keying (BPSK) [3]. Among these techniques, the BPSK features high power transmission efficiency and high bandwidth efficiency [3]. Hence, in many bio-implantable applications the BPSK is used for data transfer.

To demodulate the BPSK signal, an accurate reference carrier clock at the receiver side is required, which results in complicated and power hungry circuits using PLLs. To overcome this problem, non-coherent detection methods have been presented [4, 5]. Despite of the higher bit error rate (BER) of the non-coherent BPSK compared to the coherent BPSK, it is widely used in RF circuits because of its simple circuitry.

In this article, we present a new non-coherent low power BPSK demodulator, which can be used in the downlink data communication of narrow-band inductive link systems. Low power consumption, high data rate, and reliability of the circuit have been the main design parameters in the proposed demodulator. The proposed circuit has a better performance compared to other state of the art BPSK demodulators.

2 The proposed demodulator

In the BPSK modulation, the phase of the carrier changes according to the data which is being modulated. Hence, in the BPSK demodulator the phase transitions should be detected in order to extract the transmitted data. Fig. 1.a illustrates the architecture of the proposed BPSK demodulator. It mainly consists of two blocks, namely: a phase transition detector block, and a data detection block. The BPSK signal that is coming from the LC tank of the inductive link (V_{in}) enters a 1-bit digitizer. This signal then goes into the phase transition detector, and then passes through the data detector block. The output of the data detector block is the demodulated data. The operation of each block is discussed in the following section.

Fig. 2 shows the simulated waveforms of the BPSK demodulator. We assume a piece of data, as shown in Fig. 2-a, phase modulates a carrier signal to generate the BPSK signal (V_{in} in Fig. 2-b). It is worth mentioning that in non-coherent BPSK modulation successful operation requires the carrier frequency f_c to be an integer multiple of the bit rate r_b. In other words if we assume that the carrier period is equal to T, then the phase transitions should only occur at times nT, where n is an integer number. The modulated signal, V_{in}, enters the quantizer of the demodulator. The quantizer compares the

DOI: 10.1587/elex.7.1592
Received September 12, 2010
Accepted September 28, 2010
Published October 25, 2010

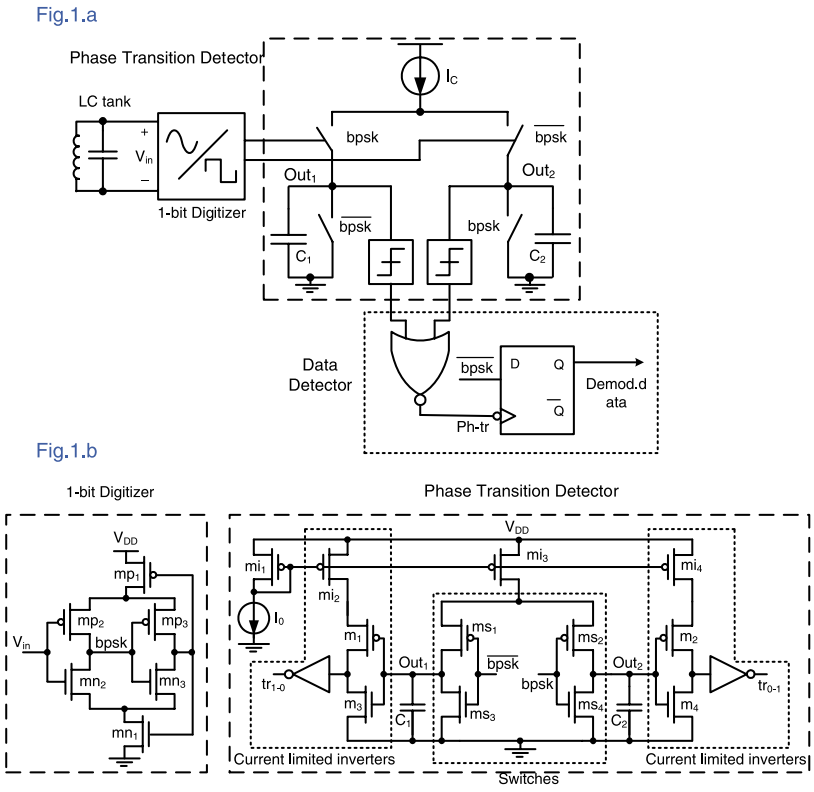

Fig. 1. a) The architecture of the proposed BPSK demodulator, b) The schematic of the proposed BPSK demodulator

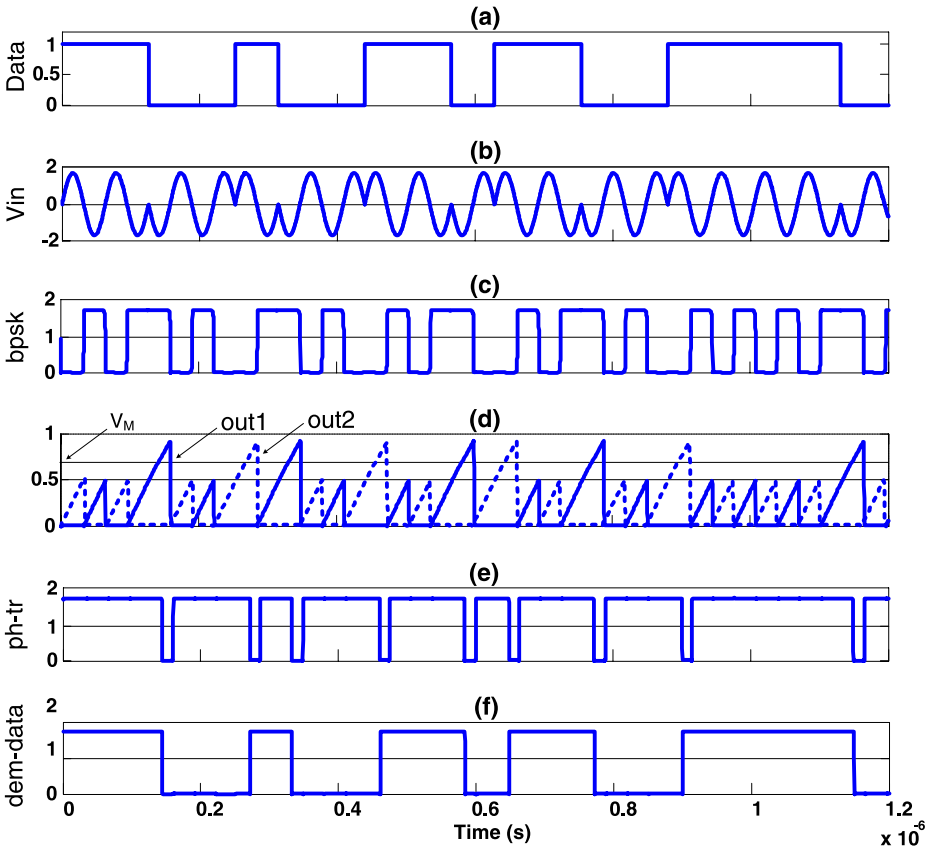

Fig. 2. Simulated waveforms of the BPSK demodulator at 1.8 V supply voltage

DOI: 10.1587/elex.7.1592
Received September 12, 2010
Accepted September 28, 2010
Published October 25, 2010

modulate signal, V_{in}, with 0 and generates the digital *bpsk* signal as shown in Fig. 2-c. As it can be seen in this figure, if a phase shift happens, the "0" or "1" duration of the *bpsk* signal becomes longer. In the phase transition detector block, depending on the *bpsk* and $\overline{bpsk}$ signals, the current of the current source I_c goes into the capacitor C1 or C2. This causes the voltages of the two capacitors (out_1 and out_2) to change linearly as a function of time, as is illustrated in Fig. 2-d. The peak values of the capacitors' voltages change according to the pulse duration of the *bpsk* and $\overline{bpsk}$ signals. Therefore, if we compare the $out1$ and $out2$ voltages with a predetermined threshold voltage (V_M), it is possible to distinguish the phase transition in the BPSK signal. In our proposed design, this is done by introducing two stages of current limited inverters. The capacitor voltages are fed to these inverters to generate a digital voltage. The outputs of the inverters go into a NOR gate to generate a voltage that indicates the phase transitions in the BPSK signal (*Ph-tr* signal in Fig. 2-e). The output of the NOR gate generates a falling edge on every phase transition. Finally, in the data detector block, the data is extracted by applying the $\overline{bpsk}$ and *Ph-tr* signals to a D flip flop (DFF). The output of the DFF is shown in Fig. 2-f and can be compared with Fig. 2-a to see how the data is properly retrieved.

The schematic of the proposed BPSK demodulator is depicted in Fig. 1.b. For the quantizer a very low power Schmitt trigger, presented in [6], is used. It is possible to use a simple inverter as a quantizer for the BPSK signal; however it is essential to use a Schmitt trigger if low power consumption is of interest. This is due to the fact that an inverter becomes very power hungry when it receives an analog signal (due to the direct current path between V_{dd} and *GND* when the signal is neither 0 nor 1). The switching points of the Schmitt trigger are designed to be at 0.4 V and 1.1 V when the supply voltage is 1.8 V. The BPSK signal is capacitively coupled to the input of the Schmitt trigger to match the common mode input range of the quantizer. The PMOS transistor M_{i3} operates as a current source. Transistors M_{s1} to M_{s4} make the switches shown in Fig. 1.a. Transistors M_1 to M_4 form two current limited inverters whose currents are limited by two PMOS transistors M_{i2} and M_{i4}. To make the edges sharper, these inverters are followed by another inverter before being applied to the NOR gate.

3 Simulation results

The proposed demodulator is designed and simulated in the 0.18-μm standard CMOS technology. A sample data stream is modulated with a carrier frequency of 16 MHz. The simulated waveforms for the typical device model at a supply voltage of 1.8 V are illustrated in Fig. 2. In order to inspect the robustness of the circuit against the process variation and carrier frequency shift, simulations are done at all process corners and the frequency of the carrier is shifted around the centre frequency of 16 MHz. The circuit is able to operate properly at all corners. The power consumption and tolerable frequency range of the circuit is measured in each case. In TT process corner,

DOI: 10.1587/elex.7.1592
Received September 12, 2010
Accepted September 28, 2010
Published October 25, 2010

the demodulator is functional for the considerably large frequency range of 11.3 MHz–21 MHz and 11.2 MHz–20.5 MHz, at 1.8 V and 1.0 V, respectively. The worst case happens in SS process corner, in which the operational frequency range reduces to 9.5 MHz–17.5 MHz and 10.5–17.5 MHz under supply voltages of 1.8 V and 1.0 V, respectively. These results demonstrate that in all process corners the demodulator can tolerate a relatively large frequency shift.

For the purpose of comparison, the specifications of the demodulator are compared with a few other BPSK demodulators in Table I. Clearly, the proposed circuit has a superior performance, especially in terms of the power consumption. In addition to the extremely low power consumption, simulation results show that the proposed circuit provides a data rate to carrier frequency of 100%, which is essential for high data rate transcutaneous telemetry systems.

Table I. Comparison of the proposed circuit with a few state of the art BPSK demodulators

Reference	Modulation/ Detection type	Carrier frequency (MHz)	Data rate (Mbps)	Power consumption (μW)
[3]	BPSK/coherent	10	1.12	610 @1.8
[4]	BPSK/non coherent	4	0.8	59 @1.8
[5]	BPSK/non coherent	8	8	148 @1.8
This work	BPSK/non coherent	16	16	6.3 @1.8

4 Conclusion

A new ultra-low power BPSK demodulator based on non coherent detection is presented. The proposed circuit operates with a data rate to carrier ratio of 100%, and at 16 Mbps data rate its power consumption is as low as 6.3 μW and 1.96 μW at 1.8 V and 1.0 V supply voltages, respectively. This feature is very important in inductively powered implantable chips in which the power budget is very limited. The proposed circuit is simulated in the 0.18 μm CMOS technology using HSPICE. Simulation results show that the proposed demodulator is very robust against process variations and carrier frequency shift.

DOI: 10.1587/elex.7.1592
Received September 12, 2010
Accepted September 28, 2010
Published October 25, 2010