

A new robust capacitively coupled second harmonic quadrature LC oscillator

Emad Ebrahimi · Sasan Naseh

Received: 1 June 2010/Revised: 6 July 2010/Accepted: 29 July 2010/Published online: 10 August 2010
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Abstract A study of some reported superharmonic LC quadrature voltage-controlled oscillator (LC-QVCO) is performed in which it is shown that robustness of the quadrature oscillation varies depending on the coupling configuration. Next, a new superharmonic LC-QVCO is proposed in which the common source node in either of two identical cross-connected LC-VCOs is coupled via a capacitor to the node common between the two varactors in the LC-tank of the other LC-VCO. As a result of connecting common mode nodes, the currents flowing through the two coupling capacitors are comprised of only the even harmonics. In the proposed coupling configuration there exists a closed loop through which the second harmonic signals circulate. A qualitative argument is presented to justify the robustness of the quadrature nature of the proposed QVCO by applying the Barkhausen phase criterion to the second harmonic signals in the loop. Since the coupling devices are only two capacitors, no extra noise sources and power consumption are added to the core VCOs. A Monte-Carlo simulation showed that the phase error of the proposed QVCO caused by device mismatches is no more than 1° . Also, generalizing this method to several numbers of VCOs in a loop, multiphase signals can be generated. The proposed circuits were designed using a $0.18\text{-}\mu\text{m}$ RF CMOS technology and simulation results are presented.

Keywords LC quadrature voltage-controlled oscillators · Low-phase noise · Low-power · Multiphase · Quadrature robustness · Superharmonic QVCO

1 Introduction

Many modern communication systems such as zero-IF receivers, image rejection architectures, clock and data recovery (CDR), and QPSK modulators require oscillating signals with 90° phase differences (I/Q signals) and therefore, quadrature voltage-controlled oscillators (QVCO) are an indispensable part of these systems. Performance of the QVCO can affect the overall performance of the system and therefore, many efforts have been put on the design of low-phase noise, low-power, highly integrated and robust QVCOs. Some circuits and methods used for quadrature signals generation are [1]: poly-phase RC-CR filters, master-slave flip-flops used as frequency divider, ring oscillators, and QVCOs with LC tanks (LC-QVCOs).

Due to their low phase noise and low power consumption, LC-QVCOs have received lots of attention in the recent years [2–15]. LC-QVCOs are usually made of coupling two identical cross-connected LC-VCOs in which oscillating signals are injected from one oscillator to the other and vice versa [2]. Depending on their mechanism of operation, LC-QVCOs can be categorized in two main groups. In the first group, two identical LC-VCOs are coupled in an “in-phase anti-phase” manner in such a way that the *first* harmonic oscillating signals are injected from each of the core oscillator to the other [2–4]. In the second group known as superharmonic QVCOs, the *second* harmonic oscillating signals, instead of the first harmonics, from a common mode node in each of the core oscillators are injected to the other. In most of the QVCOs in the

E. Ebrahimi (✉) · S. Naseh
Department of Electrical Engineering, Ferdowsi University
of Mashhad, Mashhad, Iran
e-mail: ebrahimi_em@yahoo.com

S. Naseh
e-mail: naseh@um.ac.ir

former group, presence of additional coupling devices can cause extra capacitive loading and hence degradation in the tuning range. Furthermore, the QVCO oscillation frequency deviates from the LC-tank resonance frequency, leading to phase noise degradation [16]. In superharmonic QVCOs, however, each QVCO operates at its tank resonance frequency and as such, a 3 dB phase noise improvement in comparison with that of the core VCO is observed [5].

In this work a new low-phase noise and robust superharmonic LC-QVCO is proposed. In Sect. 2, some different mechanisms of coupling of the two core oscillators in the previous superharmonic QVCOs are explained and discussed. In Sect. 3 the circuit configuration of the proposed LC-QVCO is described and a qualitative analysis of its operation is presented. Results of the simulation of the proposed circuit and its comparison with previous superharmonic QVCOs are presented in Sect. 4. In Sect. 5 a new *multiphase* superharmonic LC-VCO is introduced. A summary of the main results is presented in the last section.

2 Superharmonic coupling mechanisms and quadrature robustness

The superharmonic QVCOs presented in the recent years are all made of coupling two identical cross-connected LC-VCOs via pairs of *identical* common mode nodes. Schematics of three different superharmonics QVCOs are shown in Fig. 1 and the common mode node pairs in these circuits are denoted with (a, a') , (b, b') , and (c, c') . As can be easily verified, presence of a 180° phase difference between the voltage and/or current signals (e.g. V_a and $V_{a'}$, or I_a and $I_{a'}$) at the common mode nodes of each of the core oscillators, results in 90° phase difference in the first harmonic components of the output signals [5–14].

The 180° phase difference can be provided with a transformer. An inverting transformer, as shown in Fig. 1(a), enforces 180° phase difference between the potentials of the common source nodes ($V_a, V_{a'}$) [6]. While the transformer used in [6] is an inverting transformer, simulations showed that non-inverting transformers with coupling factor $K < 0.7$ can also be used, in which the 180° phase difference is enforced between the second harmonics of the currents I_a and $I_{a'}$ (V_a and $V_{a'}$ being in-phase). Since the DC voltage drop across each of the primary and secondary inductors of the transformer is zero, this QVCO can operate with a lower supply voltages compared to the QVCOs with tail transistors. However, the on-chip transformer occupies large chip area and its limited quality factor can cause degradation of the phase noise.

In the QVCO proposed in [7], the transformer is replaced with a cross-connected differential pair and in this way the chip area is reduced (Fig. 1(b)). It can be easily verified that presence of the positive feedback in the cross-connected tail transistors M_{tail1} and M_{tail2} causes that the variations of the voltages V_b and $V_{b'}$, and also the variations of the currents I_b and $I_{b'}$, to be in the opposite phases, which means that 180° phase difference is enforced between the second harmonics of V_b and $V_{b'}$ and between the second harmonics of I_b and $I_{b'}$.

Another way of implementing superharmonic QVCOs is to couple two identical LC-VCOs by connecting two identical common mode nodes in the core VCOs via passive elements such as capacitor [8], or even via a short circuit [9]. An example is shown in Fig. 1(c).

Although the coupling devices in [8] and [9] have the advantage of not introducing any extra noise to the circuit, further simulations using a wide variety of the circuit parameter values revealed that the outputs, while synchronized (i.e. the two oscillators oscillate at the same frequency), are not always in quadrature. Simulations showed

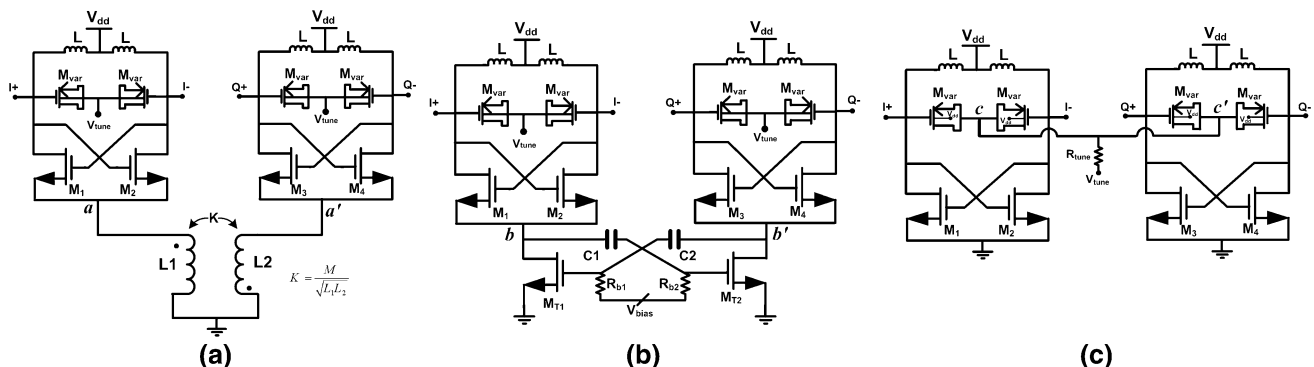


Fig. 1 a, b Schematics of the superharmonic QVCOs with anti-phase (i.e. 180° phase difference) coupling ([6], [7]), c QVCO with direct coupling [9]

that these circuits may oscillate in-phase and generate quadrature outputs only for a limited region of circuit elements values, a behavior in contrast to those of [6, 7] in which almost always generated quadrature outputs. In other words, the quadrature nature of the circuits in [8, 9] is not as robust as that of the circuits in [6, 7]. This difference can be explained as follows. In the circuits in [8, 9] it is the non-linear nature of the injection locking that puts the circuit in the quadrature mode, and the coupling devices play no role in enforcing the 90° phase difference, while in the circuits in Fig. 1(a) and (b), besides the injection locking phenomenon, the coupling devices also enforce the 180° phase difference between the second harmonics.

The circuits described above have advantages and disadvantages in terms of quadrature robustness and chip area efficiency. In the next section a new low-phase noise, area-efficient and robust superharmonic QVCO is proposed.

3 The proposed superharmonic QVCO

In the QVCOs reviewed in the last section, it was seen that a common mode node in one of the core VCOs is coupled to the *same* common mode node of the other core VCO, e.g. in Fig. 1 node *a* is coupled to node *a'*, or, node *c* is coupled to node *c'*. In the superharmonic QVCO presented in this work, *two* common mode nodes from one core oscillator are *cross-coupled* to the *same two* nodes in the other core VCO.

The proposed QVCO is shown in Fig. 2: two identical LC-VCOs are coupled together via the common source nodes (*a, a'*) of cross-connected transistors (M_{1-4}), and the middle nodes (*b, b'*) of varactors (M_{var}) in a cross-coupled manner, i.e. nodes *a* and *b'* are connected to each other and nodes *b* and *a'* are connected to each other, via two identical coupling capacitors C_{cpl1} and C_{cpl2} , respectively.

As illustrated in Fig. 2, the second harmonics are injected from node *a* to node *b'*, and from node *b* to node

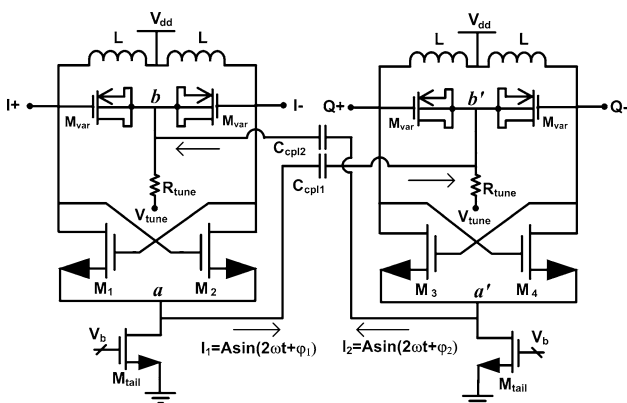


Fig. 2 Schematic of the proposed superharmonic QVCO

a'. This scheme of connection enforces 180° phase difference between the second harmonics of the two core VCOs and thus, a 90° phase difference will appear between the fundamental harmonics of the core VCOs at output nodes I^\pm and Q^\pm .

The circuit operation can be analyzed from a different point of view as well. The injected second harmonics flow in a closed loop, i.e. $a \rightarrow b' \rightarrow a' \rightarrow b \rightarrow a$. Depicted in Fig. 3, each LC-VCO has been modeled as a black box with two terminals *a* and *b* (*a'* and *b'*) oscillating at frequency $2f_0$. The two black boxes are placed in a loop and therefore, according to the Barkhausen phase criterion, 360° phase shift will exist around the loop. That is:

$$\Delta\varphi_1 + \Delta\varphi_3 + \Delta\varphi_2 + \Delta\varphi_4 = 360^\circ \tag{1}$$

where $\Delta\varphi_{1,2}$ are the phase shifts of the signal through each black box and $\Delta\varphi_{3,4}$ are the phase shifts due to the coupling capacitors. The two black boxes (LC-VCO) are identical and hence:

$$\Delta\varphi_1 = \Delta\varphi_2 \tag{2}$$

Also, due to the symmetry of the circuit the phase shifts introduced by the coupling capacitors are the same. Thus:

$$\Delta\varphi_3 = \Delta\varphi_4. \tag{3}$$

Equations 1–3 simply mean that $\Delta\varphi_1 + \Delta\varphi_3 = \Delta\varphi_2 + \Delta\varphi_4 = 180^\circ$, which, as explained before, leads to a 90° phase difference between the first (i.e. fundamental) harmonics, e.g. potentials of the nodes I^+ and Q^+ . It can be seen that, while the injection locking phenomenon results in the synchronization of the two core oscillators, presence of the *closed loop* in this coupling configuration enforces 180° phase difference between the second harmonics and subsequently results in quadrature output signals. Similar to the QVCOs in [6, 7] (in which the utilization of the particular coupling devices resulted in more robust quadrature oscillation compared to those in [8, 9]), in the proposed QVCO the robustness of the quadrature oscillation is guaranteed due to the presence of the loop;

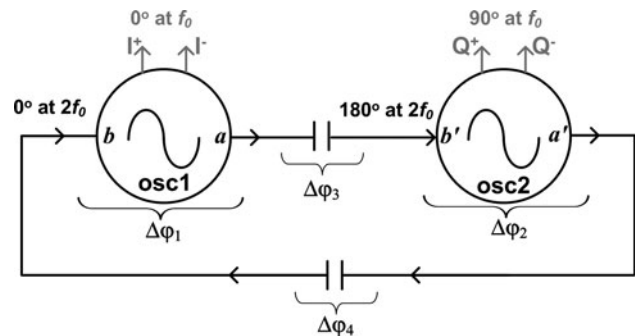


Fig. 3 An intuitive model of the proposed QVCO

no on-chip transformer or other noisy coupling devices are utilized.

The capacitors $C_{cp1,2}$ used as the coupling devices in the proposed QVCO introduce no extra noise and power dissipation, and at the same time occupy much less chip area compared to the on-chip transformers [6]. Also, capacitors as coupling devices do not transfer any low frequency noise (e.g. flicker noise at the drain of the tail transistors) from one core oscillator to the other.

The idea of taking advantage of a loop in the coupling configuration in order to increase the robustness of the quadrature oscillation in superharmonic LC-QVCOs, can be implemented in different forms. One such an example is shown in Fig. 4, in which the substrates of the tail transistors are utilized instead of the common source nodes of the cross-connected transistors (instead of the substrate nodes of the tail transistors, their gate terminals could be used too). In this circuit the second harmonics of the nodes a and a' are injected to the substrates of the tails via the drain-substrate junction capacitances of M_{tail} . The DC biasing of the substrates are provided via the R_b resistors. The analysis and features of this circuit are very similar to those of the proposed QVCO in Fig. 2 (though simulations gave slightly better numbers for the QVCO in Fig. 4).

To investigate the stability of the proposed QVCO, the stability criterion in [17] is checked. It can be said that the stability of the proposed QVCO depends on the stability of each of its core VCOs. The core VCO is a conventional negative resistance ($-Gm$) oscillator in which the cross-connected transistors produce a negative resistance. Therefore, the simplified model of each of the core LC-VCOs is comprised of a lossy LC-tank in parallel with a negative resistance (similar to a tunnel diode oscillator). As discussed in [18], since the tunnel diode oscillators always satisfy Ohira’s stability criterion, it can be deduced that the core LC-VCOs always satisfy the stability

criterion. Simulation results also confirm the stability of the proposed QVCO.

4 Simulation results

The simulation results of the proposed superharmonic QVCOs are presented and compared with simulation results of some previously reported superharmonic QVCOs. The circuit in Fig. 2 was simulated using the models of a commercial $0.18\text{-}\mu\text{m}$ RF CMOS technology with circuit parameter values shown in Table 1. The values of inductors and capacitors (i.e. the size of the MOS varactors) have been chosen in such a way that the LC-tank has resonance frequency at 5 GHz. Setting the power budget to 10 mW as a typical value, the size of the current source transistors (M_{Tail}) were chosen in a way that each draws 2.7 mA from a 1.8-V power supply. The other parameters were adjusted accordingly using simulation. Resistors r_L with values of 1Ω per each nH of inductance are inserted in series with the inductors to model the inductors’ ohmic loss. Figure 5 shows the output signals of nodes I^+ , I^- , Q^+ and Q^- , and the waveforms of the common source nodes a and a' . It can be seen that there exist 90° and 180° phase difference between the outputs of the proposed circuit and between the common source voltages, respectively. The total current drawn from 1.8-V power supply is 5.2 mA. By varying V_{tune} from 0 to 1.8 V, the oscillation frequency changed from 4.75 to 5.25 GHz (a 10% frequency tuning range). Figure 6 shows the phase noise of the proposed QVCO for several frequencies within the tuning range. As can be seen the phase noise has almost a flat profile in the whole tuning range.

For preparing Figs. 5 and 6, the *Transient* and *Harmonic Balance (HB)* analysis have been utilized, respectively.

To have an estimate of the phase error caused by the various mismatches (process variations, layout asymmetries and device mismatches) in the real implementation of

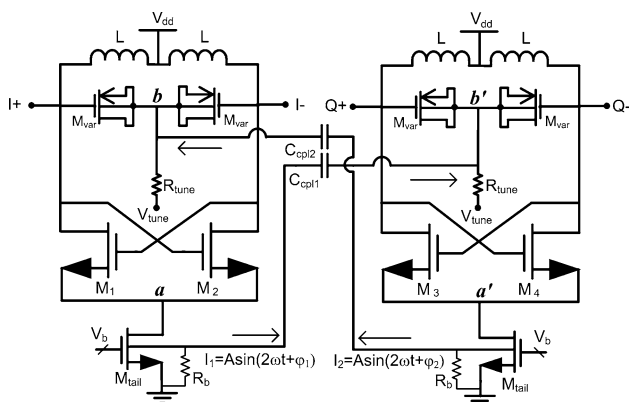


Fig. 4 Schematic of another version of the proposed QVCO: using bulk of current sources instead of the source of cross-connected transistors

Table 1 Circuit parameter values of the proposed QVCO used for simulations (r_L is the ohmic loss of the inductors)

Parameter	Value
$(W/L)_{M1-4}$	8 $\mu\text{m}/0.18 \mu\text{m}$
$(W/L)_{Mvar}$	280 $\mu\text{m}/0.18 \mu\text{m}$
$(W/L)_{Mtail}$	50 $\mu\text{m}/0.18 \mu\text{m}$
L	2 nH
r_L	2 Ω
R_{tune}	1 K Ω
C_{cp1-2}	0.5 pF
V_{dd}	1.8 V
V_{tune}	0.8 V
V_{bias}	0.85 V

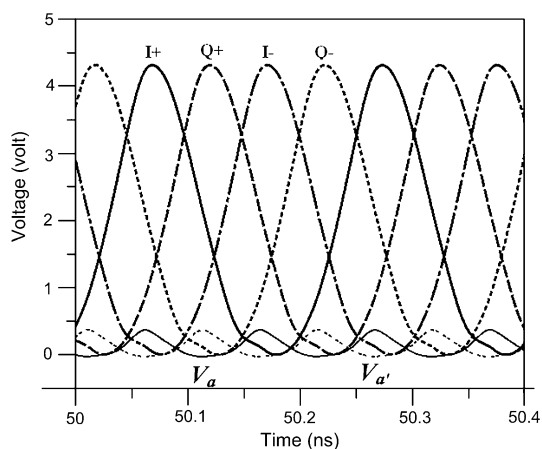


Fig. 5 Volages of the quadrature outputs and the common source nodes of the proposed QVCO in Fig. 2

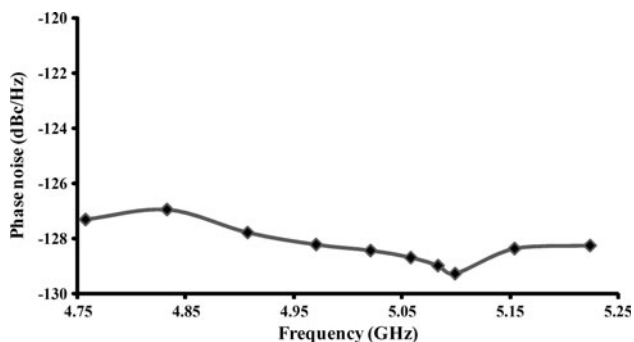


Fig. 6 Phase noise of the proposed QVCO for tuning range’s frequencies (phase noise was simulated at 3 MHz frequency offset)

the circuit, a Monte-Carlo simulation was performed with 3% mismatches in the circuit parameters. The results of 30 trials of the Monte-Carlo simulation are shown in Fig. 7. A maximum of less than 1° phase error was observed.

A comparison of the simulated phase noise of the proposed QVCO (Fig. 2) and that of the CMOS version of Hancock’s QVCO [14] is presented in Fig. 8. While for preparation of Fig. 8 no formal optimization was performed on the two QVCOs, the parameters of both circuits

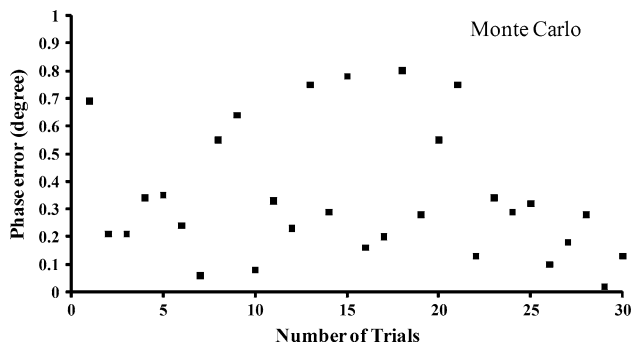


Fig. 7 Monte Carlo simulation results

were adjusted using try and error in such a way that they have the same frequency and power consumption. The proposed QVCO shows a reduction of at least 7 dB in the phase noise compared to the QVCO in [14]. This improvement can probably be explained by observing that in the QVCOs in [7, 14] each M_{tail} acts as a common source amplifier. Therefore, the noise at the drain of each M_{tail} reaches the gate of the other M_{tail} and gets amplified, which consequently can significantly degrade the phase noise of each of the core oscillators. In the proposed QVCO, however, there is no such noise amplification.

In Table 2 the performance specifications of the proposed QVCOs and several previously reported superharmonic QVCOs are presented. To compare the performance of the different QVCOs, the figure of merit (FOM) suggested in [11] is adopted:

$$FOM = 10 \log \left(S_{SSB} \left(\frac{\Delta f}{f_{osc}} \right)^2 P_{QVCO} \right). \quad (4)$$

in which S_{SSB} is the phase noise at the offset frequency Δf in dBc/Hz, f_{osc} is the oscillation frequency and P_{QVCO} is the total power consumption in milliwatts. (To have a fair comparison, *simulation* results were used to calculate the FOM for all the circuits, but interestingly, for [6] and [7] the experimental results were better than simulations, so only for these two circuits the data presented in the figure are based on the reported measurement in those papers.)

Simulations of the proposed QVCOs with a wide variety of the circuit parameter values (i.e. transistors’ dimensions, capacitors’ and inductors’ values, etc.) have resulted in quadrature outputs, confirming the robust quadrature nature of the proposed circuits.

The QVCO in Fig. 4 was also simulated with the same circuit parameter values as in Table 1 (with $R_b = 1 \text{ K}\Omega$) and a similar performance as that of the QVCO in Fig. 1 was observed. The simulation results and the FOM for this QVCO are presented in Table 2 as well. Simulations also

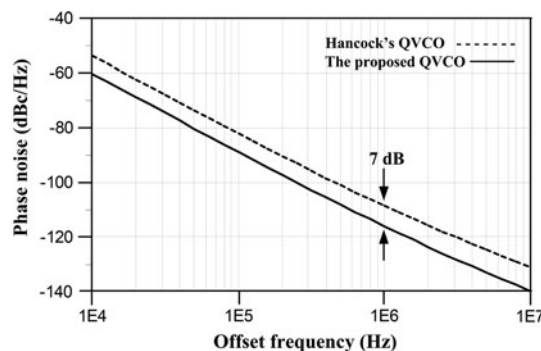


Fig. 8 Phase noise simulation results of the CMOS version of Hancock’s QVCO [14] and the proposed QVCO (Fig. 2) at 5 GHz oscillation frequency. Agilent ADS simulator was used for the simulations

Table 2 Performance specifications of some previously reported and the proposed QVCOs

QVCO	Technology (μm)	f_{osc} (GHz)	P_{QVCO} (mW)	S_{SSB} (phase noise) (dBc/Hz)	FOM (dBc)
[7]	n/a	6	n/a	-105 (at 1 MHz)	-170
[6]	0.25	5	22	-124 (at 1 MHz)	-185
[9]	0.18	5	18	-127 (at 3 MHz)	-179
[14]	0.18	3	7.5	-116 (at 1 MHz)	-177
This work (Fig. 2)	0.18	5	9.36	-128.3 (at 3 MHz)	-183
This work (Fig. 4)	0.18	5	11.5	-130 (at 3 MHz)	-184

showed that both the proposed QVCOs are able to operate with supply voltages as low as 0.7 V.

5 Multiphase signals generation

The proposed coupling method can be generalized by inserting more than two core oscillators in a loop, as depicted in Fig. 9. Simulations showed that for N = the number of LC-VCOs in the loop, $2N$ outputs with phases $n\pi/N$ ($n = 0, 1, 2 \dots 2N - 1$) are generated.

The qualitative analysis of the multiphase VCO made in this way is similar to that of the proposed QVCO (see Sect. 3). Simulations confirmed that it does show the same degree of robustness and phase noise performance.

To the authors' knowledge, this is the first reported *superharmonic* multiphase LC-VCO which thereby has the good attributes of the superharmonic coupling [5, 15], and at the same time it is robust.

As a typical case, a 3-stage multiphase LC-VCO was implemented with a commercial $0.18\text{-}\mu\text{m}$ RF CMOS process using the proposed coupling method, and simulated with the parameter values in Table 1. The circuit has a -130 dBc/Hz phase noise at 3 MHz frequency offset from the center frequency of 5 GHz, and the total power consumption is less than 15 mW. The FOM is also -182.5 dB.

6 Conclusion

Quadrature oscillators made by superharmonic coupling of two identical cross-connected LC-VCOs have wide tuning range and good phase noise [5, 15]. A careful examination of previously reported superharmonic QVCOs showed that the superharmonic QVCOs, based on their mechanism of coupling, can be categorized into two groups: in one group the coupling device does not play any role in enforcing the 90° phase difference between the output signals and the quadrature oscillation is caused solely by the nonlinear nature of injection locking phenomenon, while in the other group, in addition to the injection locking, the coupling device (e.g. transformer) enforces the 90° phase difference between the output signals as well. Simulation shows that in the former group, while the outputs do get synchronized, they are in quadrature only for a narrow region of circuit parameter values, but in the latter group the outputs are in quadrature for a wide range of circuit parameter values, meaning that quadrature oscillation is more *robust* in this group compared to the former.

To generate a robust quadrature oscillation a new superharmonic QVCO was proposed in which the two core VCOs are coupled to each other by connecting the common source node of one VCO through a capacitor to the middle node of the two varactors in the other VCO, and vice versa.

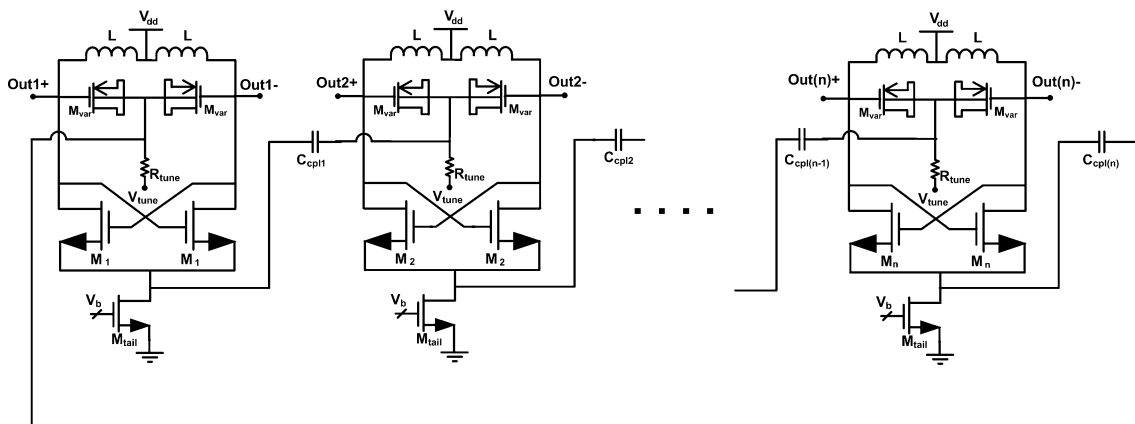


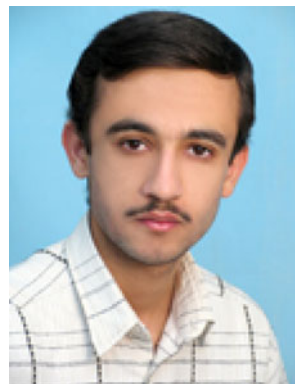
Fig. 9 The proposed multiphase LC-VCO (N is an odd integer)

This configuration effectively creates a loop through which the second harmonic signals circulate. It was shown that the 360° total phase shift existing in the loop according to the Barkhausen phase criterion, necessitates a 90° phase difference between the output signals, guarantying a robust quadrature signal generation. The coupling capacitors introduce no extra noise and power consumption to the core VCOs. Simulation results showed the proposed circuit can generate low-phase noise quadrature signals with low-power consumption while has a good robustness and phase accuracy. According to the Monte-Carlo simulation, a 3% standard deviation for device mismatches resulted in a phase error of no more than 1° .

Generalizing the proposed coupling method to N core LC-VCOs (N being an integer number), 2N multiphase signals placed in π/N phase interval can be generated.

References

- Razavi, B. (1998). *RF microelectronics*. Upper Saddle River, NJ: Prentice Hall.
- Rofougaran, A., et al. (1998). A single-chip 900-MHz spread-spectrum wireless transceiver in 1- μ m CMOS-Part I: Architecture and transmitted design. *IEEE Journal of Solid-State Circuits*, 33, 515–534.
- Andreani, A., Bonfanti, A., Romano, L., & Samori, C. (2002). Analysis and design of 1.8 GHz CMOS LC quadrature oscillator. *IEEE Journal of Solid-State Circuits*, 37(12), 1737–1747.
- Ebrahimi, E., & Naseh, S. (2009). A CMOS low-noise low-power quadrature LC oscillator. In *IEEE International Symposium on Circuits and Systems*, pp. 1305–1308.
- Tortori, P., et al. (2009). Quadrature VCOs based on direct second harmonic locking: Theoretical analysis and experimental validation. *International Journal of Circuit Theory and Applications*. doi:10.1002/cta.612.
- Gierkink, S., Levantino, S., Frye, R., Samori, C., & Boccuzzi, V. (2003). A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling. *IEEE Journal of Solid-State Circuits*, 38(7), 1148–1154.
- Hancock, T. M., & Rebeiz, G. (2004). A novel superharmonic coupling topology for quadrature oscillator design at 6 GHz. In *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 285–288.
- Soltanian, B., & Kinget, P. (2006). A low phase noise quadrature LC VCO using capacitive common-source coupling. In *European Solid-State Circuits Conference*, pp. 436–439.
- Naseh, S., Zarre, M., & Jamal Deen, M. (2008). A low-voltage low-noise superharmonic quadrature oscillator. In *IEEE International Conference on Electronics, Circuits and Systems*, pp. 400–403.
- Tortori, P., Guermandi, D., Franchi, E., & Gnudi, A. (2004). Quadrature VCO based on direct second harmonic locking. In *IEEE International Symposium on Circuits and Systems*, pp. I-169–I-172.
- Tiebout, M. (2001). Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. *IEEE Journal of Solid-State Circuits*, 36, 1018–1024.
- Alan, W. L., & Luong, H. C. (2006). A 1 V 17 GHz 5mW quadrature CMOS VCO based on transformer coupling. In *IEEE International Solid-State Circuits Conference*, pp. 711–720.
- Cabanillas, J., Dussopt, L., Lopez-Villegas, J. M., & Rebeiz, G. M. (2002). A 900 MHz low phase noise CMOS quadrature oscillator. In *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 63–66.
- Jackson, B. R., & Saavedra, C. E. (2007). A 3 GHz CMOS quadrature oscillator using active superharmonic coupling. In *Proceedings of the 37th European Microwave Conference*, pp. 1109–1112.
- Casha, O., Grech, I., & Micallef, J. (2007). Comparative study of gigahertz CMOS LC quadrature voltage-controlled oscillators with relevance to phase noise. *Analog Integrated Circuits and Signal Processing*, 52, 1–14.
- Romano, L., et al. (2004). Phase noise and accuracy in quadrature oscillators. In *IEEE International Symposium on Circuits and Systems*, pp. I-161–I-164.
- Ohira, T., & Araki, K. (2007). Active Q-factor and equilibrium stability formulation for sinusoidal oscillators. *IEEE Transactions on Circuits and Systems Part II*, 54(9), 810–814.
- Palumbo, G., Pennisi, M., & Pennisi, S. (2009). Approach to analyse and design nearly sinusoidal oscillators. *IET Circuits Devices and Systems*, 3(4), 204–221.



Emad Ebrahimi received B.Sc. and M.Sc. degrees in electrical and electronics engineering from Ferdowsi University of Mashhad, Mashhad, Iran, in 2006 and 2008 respectively. Since September 2008 he has been pursuing the Ph.D. at Ferdowsi University of Mashhad. His current fields of research are analog and RF integrated circuits design.



Sasan Naseh received the B.Sc. (1990) from Sharif University Technology, Tehran, Iran, M.A.Sc. (1995) from Concordia University, Montreal, Canada, and Ph.D. from McMaster University in Hamilton, Ontario, Canada on 2005, all in electrical engineering. Since September 2005 he has been an Assistant Professor in the Electrical Engineering Group of the Engineering Department at Ferdowsi university of Mashhad, Iran. His research and professional interest includes microelectronic device physics and analog and RF circuit design.