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A low-power Successive Approximation ADC for biomedical applications

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Abstract: A new switching algorithm is proposed in Successive Approximation Analog-to-Digital Converters (SA-ADCs) to reduce the power consumption in both DAC and comparator. This technique is more efficient in applications where the input signal has low-varying characteristics. For slow-varying samples, only the least significant bits of the new analog sample are extracted leading to power saving in both the capacitor-based DAC and the comparator. For an Electrocardiogram (ECG) signal and with the proposed structure, the simulated power consumption of the DAC, the comparator and the entire ADC for an 8-bit 10-kS/s converter are 74%, 38% and 52% less than those of a conventional architecture, respectively.

Keywords: Successive Approximation ADC, power consumption, biomedical applications

Classification: Integrated circuits

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1 Introduction

Successive approximation analog-to-digital converter (SA-ADC) has become a common choice for low-power applications because of their minimal active analog circuits [1, 2, 3, 4]. A conventional SA-ADC, one implementation example of which is shown in Fig. 1 (a), consists of a sample-and-hold (S/H) circuit, a (usually capacitive) digital-to-analog converter (DAC), a comparator and a successive approximation register (SAR). The value of each capacitor is obtained from $C_i = 2^{N-i}\, C_u$ where C_u is the size of the unit capacitor.

The operation of this structure is based on the binary search algorithm as follows. In the sampling phase, the input signal is sampled by the S/H circuit and does not change during the conversion phase. In addition, all the capacitors are discharged to ground. In the conversion phase, during the first clock cycle, C_1 (the largest capacitor in DAC) is connected to the reference voltage (V_{ref}) and all other capacitors are connected to ground. Thus the input signal is compared with the output of the DAC ($V_{DAC} = 0.5\, V_{ref}$). According to the comparison result, the most significant bit (MSB) D_1 is determined and stored in the SAR. In the second clock cycle, C_2 is connected to the V_{ref}, C_1 is discharged to ground (if $D_1 = 0$) or remains connected to V_{ref} (if $D_1 = 1$) and other capacitors remains connected to ground. Therefore, the input signal is compared with $V_{DAC} = 0.25\, V_{ref}$ (if $D_1 = 0$) or $V_{DAC} = 0.75\, V_{ref}$ (if $D_1 = 1$) and the second significant bit (i.e. D_2) will be determined. This binary search algorithm is continued until all digital bits are found after N clock cycles.

The two most important blocks that consume most of the overall power consumption of the ADC are the capacitive DAC and the comparator [3]. Although, several attempts have been reported to reduce the power consumption of SA-ADCs [1, 2, 3], few works have employed the characteristics of the input signal [4, 5]. In the conventional switching sequence of the SA-ADC, all capacitors of the capacitive array (i.e. C_1 to C_N) are switched between V_{ref} and ground according to the binary search algorithm (complete binary search) for every input sample independent of the previous one. This architecture is suitable for signals with high-varying characteristics. On the other hand, there are many applications (e.g. biomedical devices) where the input signal has large and fast variations only for short time intervals and for the rest of the time, the variations is small and slow. For such signals and for the majority of the samples, the difference between two consecutive samples of the input signal is very small compared to the entire full-scale range of the ADC. For these cases, instead of digitizing each new sample independently, only the low significant bits must be determined for every input sample. Hence, in this work, a new switching algorithm will be presented which not only reduces the power consumed in the DAC by switching only small LSB capacitors but also decreases the number of clock cycles in which the comparator is employed leading to further reduction in power consumption.

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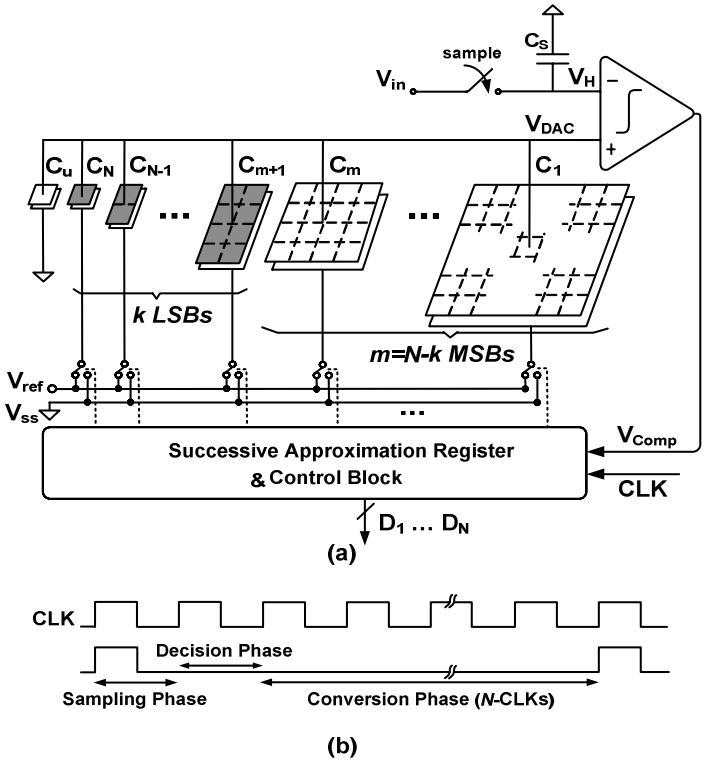

Fig. 1. (a) SA-ADC structure employing binary-weighted capacitive DAC. (b) Timing diagram for the proposed structure.

2 Proposed architecture

The operation of the proposed architecture is as follows. As shown in Fig. 1 (b), one clock cycle is added to the comparison phase (called as decision phase) compared to the conventional structure. After sampling the input signal in the sampling phase, the new analog sample (i.e. $V_H[i]$) is compared with the analog equivalent of the digital word corresponding to the previous input sample (i.e. $V_H[i\text{-}1]$) existing now in the output of the DAC. According to this comparison result, if the new sample is higher than the previous one, in the decision phase, m MSB capacitors (i.e. C_1 to C_m) are kept unchanged and the capacitors related to the k LSBs (i.e. C_{m+1} to C_N) are connected to the V_{ref}. Therefore the input sample instead of being compared with $0.5\,V_{ref}$, in the conventional structure is compared with $V_{DAC,H}$ in the proposed structure. On the other side, if the new sample is lower than the previous one, these LSB capacitors are connected to the ground and the input signal is compared with $V_{DAC,L}$. Note that m and k can be chosen according to the input signal characteristics ($m + k = N$). In addition, $V_{DAC,H}$ and $V_{DAC,L}$ are the highest and lowest levels of the DAC rounded by m bits, respectively. In the other words,

$$V_{DAC,H} = \left(\sum_{i=1}^{m}\frac{D_i}{2^i} + \sum_{i=m+1}^{N}\frac{1}{2^i}\right)V_{ref}, \quad V_{DAC,L} = \left(\sum_{i=1}^{m}\frac{D_i}{2^i}\right)V_{ref} \tag{1}$$

$$V_{DAC,H} - V_{DAC,L} = 2^{-m}V_{ref} \tag{2}$$

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According to these two comparison results, if the new input signal is between $V_{DAC,L}$ and $V_{DAC,H}$, the connections of the capacitors related to m MSBs are left unchanged and only a binary search will be done on the capacitors related to the k LSBs (i.e. C_{m+1} to C_N) during the k clock cycles. This will lead to roughly 2^m times smaller switching power consumption due to the fact that larger MSB capacitors are not switched [6]. Furthermore, during the next m clock cycles the comparator can be turned off in order to save more power consumption (the power saving ratio of which is $m/(N+2)$). On the other side, if the new sample is larger than $V_{DAC,H}$ or smaller than $V_{DAC,L}$then a complete binary search will be done during the N clock cycles similar to conventional structure.

It should be noted that in the conventional structure all the capacitors of the capacitive array including the MSB capacitor are reset to ground in

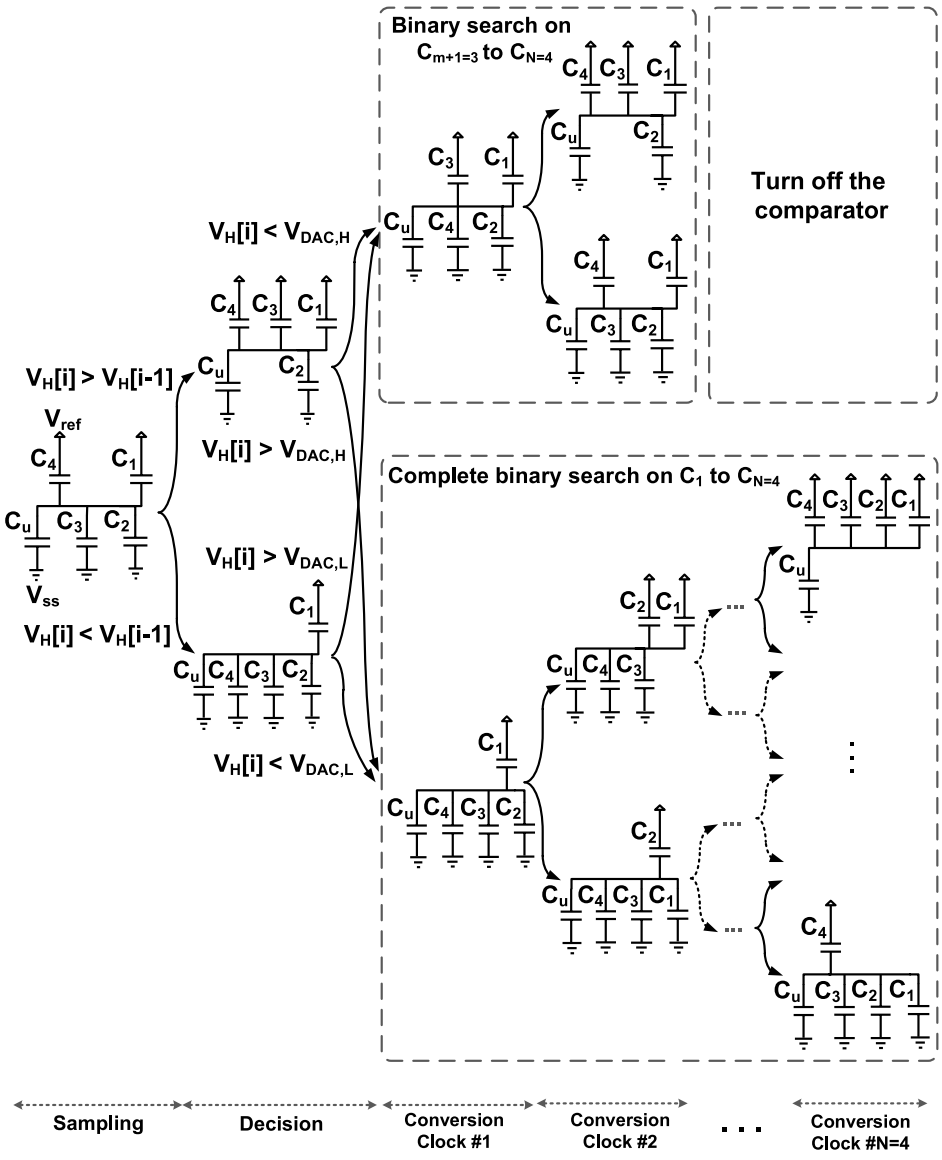

Fig. 2. Switching sequence of a 4-bit proposed structure with k = 2. The digital code corresponding to the previous input sample is assumed to be "1001".

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the sampling phase for each new input sample but in the proposed switching algorithm here, another modification is applied where the MSB capacitor (C_1) is not reset to ground for every new sample whenever a complete binary search is needed [3]. Fig. 2 illustrates the switching sequence of a 4-bit proposed structure with k = 2 (the digital code corresponding to the previous input sample is assumed to be "1001").

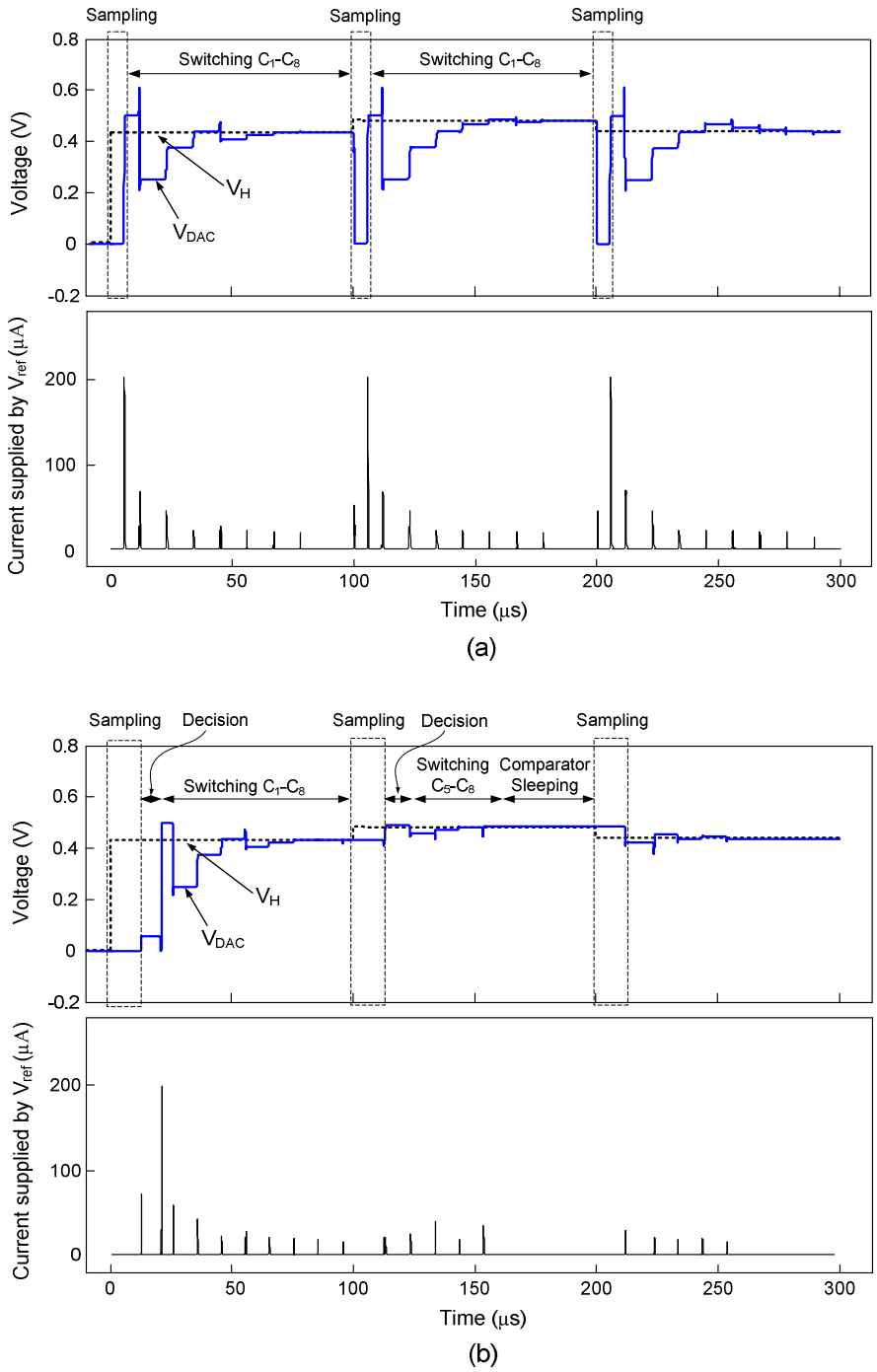

Fig. 3. Output voltage of the DAC and current supplied by V_{ref} in an 8-bit SA-ADC using (a) the conventional architecture and (b) the proposed architecture.

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Table I. Simulated values of the power consumption in the conventional and the proposed 1-V 8-bit 10 kS/s SA-ADC structures for an ECG signal as input.

	DAC	Comparator	Logic	Total
Conventional	360 nW	431 nW	24 nW	815 nW
Proposed	94 nW	267 nW	31 nW	392 nW
Power Saving	+%74	+%38	-%30	+%52

3 Simulation results

In order to verify the power saving realized by the proposed SA-ADC architecture, a 1-V 8-bit 10-kS/s SA-ADC has been designed and simulated in a 0.18-μm CMOS technology once with the conventional algorithm and then with the proposed algorithm. Based on the characteristics of the input Electrocardiogram (ECG) signal, the value of k has been chosen equal to 4 in the proposed architecture (i.e. $V_{DAC,H} - V_{DAC,L} = V_{ref}/16$). Fig. 3 shows the simulation results of the output voltage of the DAC in the conventional and the proposed structures for an identical input signal. As shown in Fig. 3 (a), the conventional structure converts the input samples independent of the previous sample. In other words, for every input sample all capacitors (i.e. C_1 to C_8) are charged according to the conventional binary search algorithm, as can be seen in the corresponding current waveform. But as shown in Fig. 3 (b), in the proposed structure, when the difference of the new sample and the previous one is less than the $2^{-4}V_{ref}$, the MSB capacitors (i.e. C_1 to C_4) are left unchanged and only the binary search will be done on the capacitors related to the k LSBs (i.e. C_5 to C_8) during only 4 clock cycles. This will lead to roughly 2^4 times smaller capacitor switching power consumption due to the fact that larger MSB capacitors are not switched. In addition, since the comparator is turned off during the next m = 4 clock cycles, the power saving of the idea is even more.

Simulation results for a real ECG input signal show that in the proposed structure the power consumption of the capacitive-array DAC and the comparator are 74% and 38% smaller than those of the conventional structure, respectively as shown in Table I. However, the modified digital circuitry imposes around 30% overhead to the power consumption of the conventional logic circuit. Therefore, the entire power consumption of the ADC using the proposed algorithm is 52% smaller than the conventional one. Finally, the linearity behavior (e.g. the integral non-linearity (INL) and differential non-linearity (DNL) characteristics) of this structure is the same as the conventional structure.

4 Conclusion

The switching algorithm of SA-ADCs have been modified in order to save the power consumption in applications where the input signal activity is low most of the time such as biomedical sensor interface circuits and wireless

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network sensors. In the proposed algorithm, if the new sample occurs in the small vicinity of the previous sample, only the LSBs are digitized leading to smaller power consumption in the DAC and the comparator.

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