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Investigation of the novel attributes in double recessed gate SiC MESFETs at drain side

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Abstract

In this paper, the potential impact of drain side-double recessed gate (DS-DRG) on silicon carbide (SiC)-based metal semiconductor field effect transistors (MESFETs) is studied. We investigate the device performance focusing on breakdown voltage, threshold voltage, drain current and dc output conductance with two-dimensional and two-carrier device simulation. Our simulation results demonstrate that the channel thickness under the gate in the drain side is an important factor in the breakdown voltage. Also, the positive shift in the threshold voltage for the DS-DRG structure is larger in comparison with that for the source side-double recessed gate (SS-DRG) SiC MESFET. The saturated drain current for the DS-DRG structure is larger compared to that for the SS-DRG structure. The maximum dc output conductance in the DS-DRG structure is smaller than that in the SS-DRG structure.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The SiC metal semiconductor field effect transistor (MESFET) technology is a candidate for high power microwave applications. Its wide bandgap and high thermal conductivity offer several advantages compared to Si- and GaAs-based technologies. SiC MESFETs are very well suited for high voltage, high power and high temperature applications due to their superior material properties, especially high critical electric field, high electron saturation velocity and high thermal conductivity. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of 300–500 cm^2 V^{-1} s^{-1}, at doping levels of interest for MESFETs in the range of 1×10^{17}–5×10^{17} cm^{-3}. This drawback results in a larger source resistance and lower transconductance compared to GaAs-based MESFETs [1–6].

A source side-double recessed gate (SS-DRG) SiC MESFET has two regions under the gate that have different channel thicknesses. The region with narrower channel thickness will lead to a larger aspect ratio of the gate length to the channel thickness (L_g/a) and reduces short-channel effects such as drain-induced barrier lowering. Also, the region with larger channel thickness will lead to a large product of the channel doping and the thickness ($N \times a$) and increases drain current. However, with increasing saturation drain current, the device performance is degraded with decreasing breakdown voltage due to larger channel thickness between gate and drain. Therefore, the conventional double recessed gate SiC MESFET increases the drain current and reduces the short-channel effects.

For the first time in this paper, the potential impact of drain side-double recessed gate (DS-DRG) on SiC MESFETs is studied using a two-dimensional (2D) simulation. The unique features of the SiC MESFET device with DS-DRG are explored and compared with those of a SiC MESFET with SS-DRG in terms of breakdown voltage, threshold voltage, drain current and dc output conductance. We demonstrate that the breakdown voltage improves in the DS-DRG structure if the double recessed gate length increases at a fixed double

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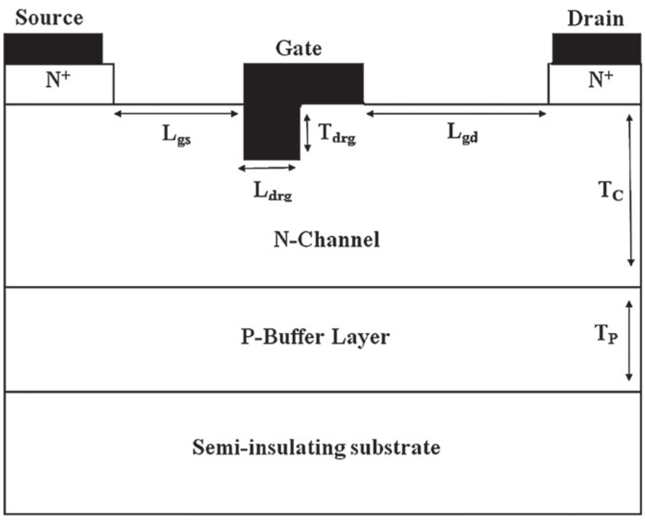
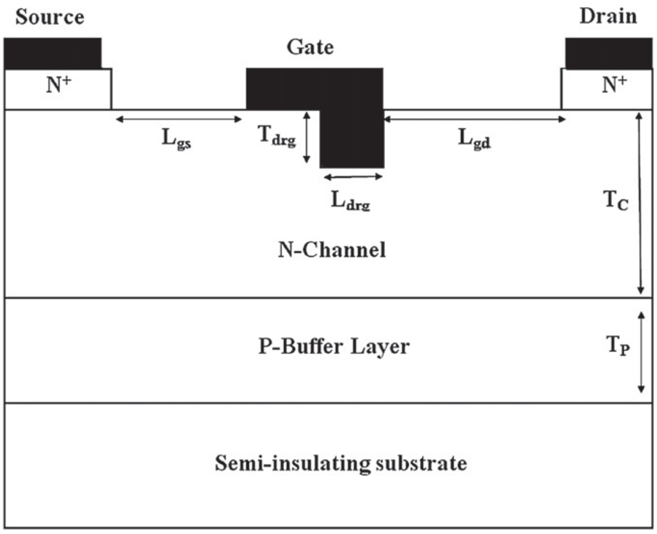


(*a*)



(*b*)

Figure 1. Cross section of the (*a*) SS-DRG and (*b*) DS-DRG structures. For the two structures: L_{drg} is double recessed gate length, T_{drg} is double recessed gate thickness, L_{gs} is gate–source spacing, L_{gd} is gate–drain spacing, T_{C} is channel thickness and T_{P} is P-buffer thickness.

recessed gate thickness. Also, the maximum dc output conductance in the DS-DRG structure is smaller than that in the SS-DRG structure at a fixed double recessed gate thickness.

2. Device structure

Figures 1(*a*) and (*b*) show the schematic cross-section of the SS-DRG [7, 8] and DS-DRG structures. The dimensions of the proposed structure are as follows: gate length $L_{\mathrm{g}} = 0.7\ \mu$m, recessed depth is 0.05 μm to the channel, gate–drain spacing $L_{\mathrm{gd}} = 1\ \mu$m, gate–source spacing $L_{\mathrm{gs}} = 0.5\ \mu$m, channel thickness $T_{\mathrm{C}} = 0.25\ \mu$m and channel doping $N_{\mathrm{D}} = 3 \times 10^{17}$ cm^{-3}. The doping and thickness of the P-buffer layer are $N_{\mathrm{A}} = 1.4 \times 10^{15}$ cm^{-3} and $T_{\mathrm{P}} = 0.5\ \mu$m, respectively. The substrate is semi-insulating. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV and aluminum is used for the source/drain contacts. All device parameters of the DS-DRG are equivalent to those of the SS-DRG unless otherwise stated. It is worth noting that the SS-DRG and DS-DRG structures can be fabricated using the same procedure as reported in [4, 9]. The devices are simulated using two-dimensional ATLAS software [10] with SiC material parameters [11–13]. In order to achieve more realistic results, several models are activated in simulation, including the 'SRH' model for Shockley–Read–Hall recombination, the 'Print' model for verifying models and material parameters, the 'Conmob' model for standard concentration-dependent mobility, the 'Fldmob' model for parallel electric field-dependent mobility, the 'Fermi Dirac' model for statistics and the 'Impact Selb' model for impact ionization [14].

3. Results and discussion

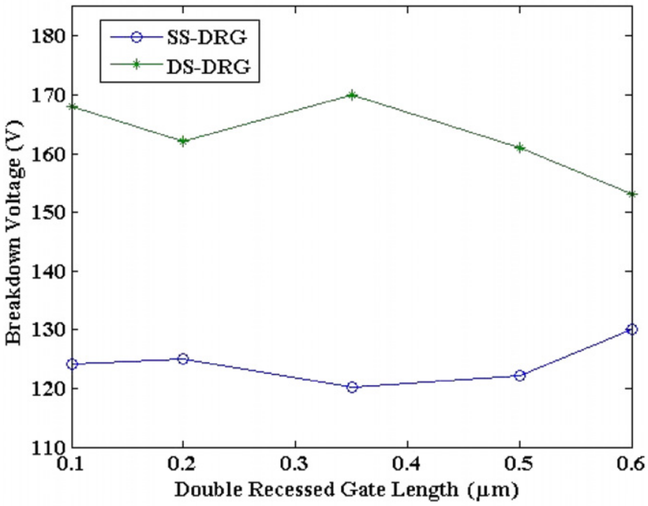
3.1. Breakdown voltage

Figure 2(*a*) shows the breakdown voltages with respect to the double recessed gate length (L_{drg}) in the DS-DRG and SS-DRG structures in a fixed double recessed gate thickness ($T_{\mathrm{drg}} = 0.05\ \mu$m) at $V_{\mathrm{GS}} = -1$ V conditions. As shown in the figure, the DS-DRG structure has larger breakdown voltage than the SS-DRG structure due to the narrower channel under the gate in the drain side. The maximum breakdown voltage for the DS-DRG and SS-DRG structures are 170 and 130 V, respectively. Simulation results shown in figure 2(*a*) show that the breakdown voltages vary slightly with increasing L_{drg} in the two structures. However, increasing L_{drg} in the drain side causes more variation at the breakdown voltage in comparison with increasing L_{drg} in the source side. Hence, the channel thickness under the gate in the drain side is an important factor in the breakdown voltage for the two structures [7].

A further investigation shows that the breakdown occurred at the gate corner near the drain due to the electric field crowding [7, 8]. Simulation results shown in figure 2(*b*) show the maximum lateral electric field at the gate corner near the drain at $V_{\mathrm{DS}} = 115$ V and $V_{\mathrm{GS}} = -1$ V for the two structures. Comparison of figures 2(*a*) and (*b*) reveals that the breakdown voltage improves with decreasing maximum lateral electric field at the gate corner in the drain side. As the figures show, for different L_{drg}, the maximum lateral electric field in the DS-DRG structure is smaller than that in the SS-DRG structure. Therefore, for different L_{drg}, the DS-DRG structure has larger breakdown voltage than the SS-DRG structure.

3.2. Drain current

Figure 3(*a*) shows the output characteristics of the DS-DRG and SS-DRG structures at different values of double recessed gate lengths at $T_{\mathrm{drg}} = 0.05\ \mu$m and $V_{\mathrm{GS}} = 0$ V conditions. As shown in the figure, increasing L_{drg} from 0.1 to 0.6 μm reduces the saturated drain current for the two structures, because, for high drain current, a large product of the channel doping and thickness ($N \times a$) is required. When the double recessed gate length varies from 0.1 to 0.6 μm, the region with narrow channel under the gate will increase and therefore the drain



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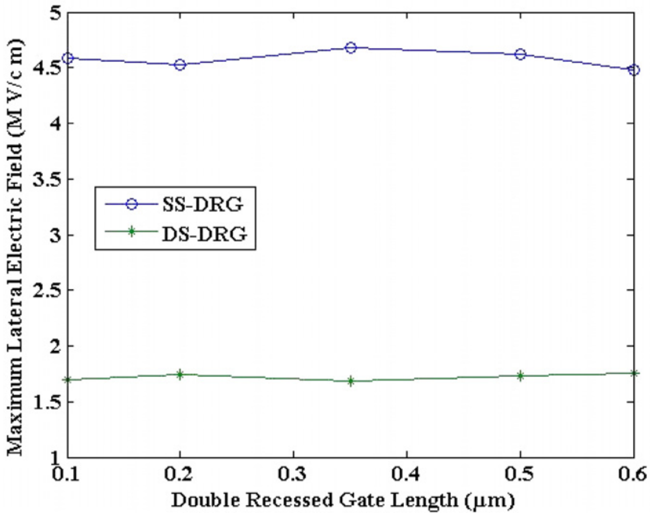
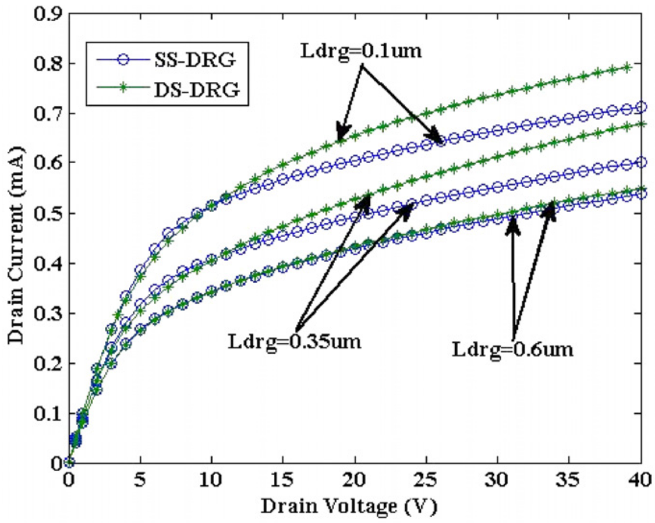


(*b*)

Figure 2. Breakdown voltage as a function of the (*a*) L_{drg} in the SS-DRG and DS-DRG structures at $V_{\mathrm{GS}} = -1$ V and maximum electric field as a function of the (*b*) L_{drg} in the SS-DRG and DS-DRG structures at $V_{\mathrm{GS}} = -1$ V and $V_{\mathrm{DS}} = 115$ V.



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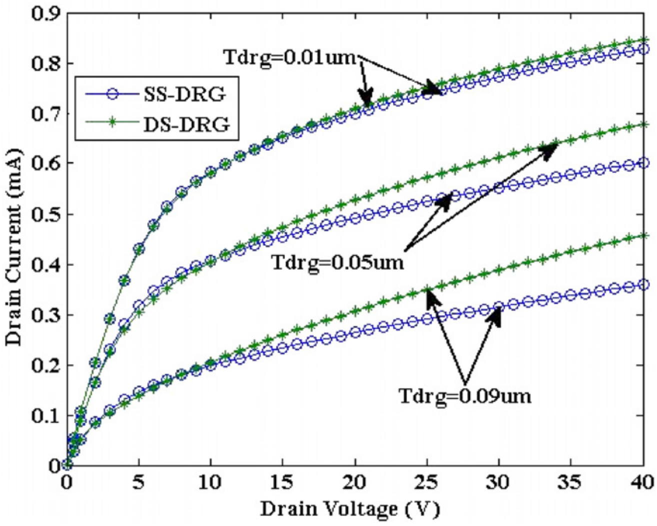


(*b*)

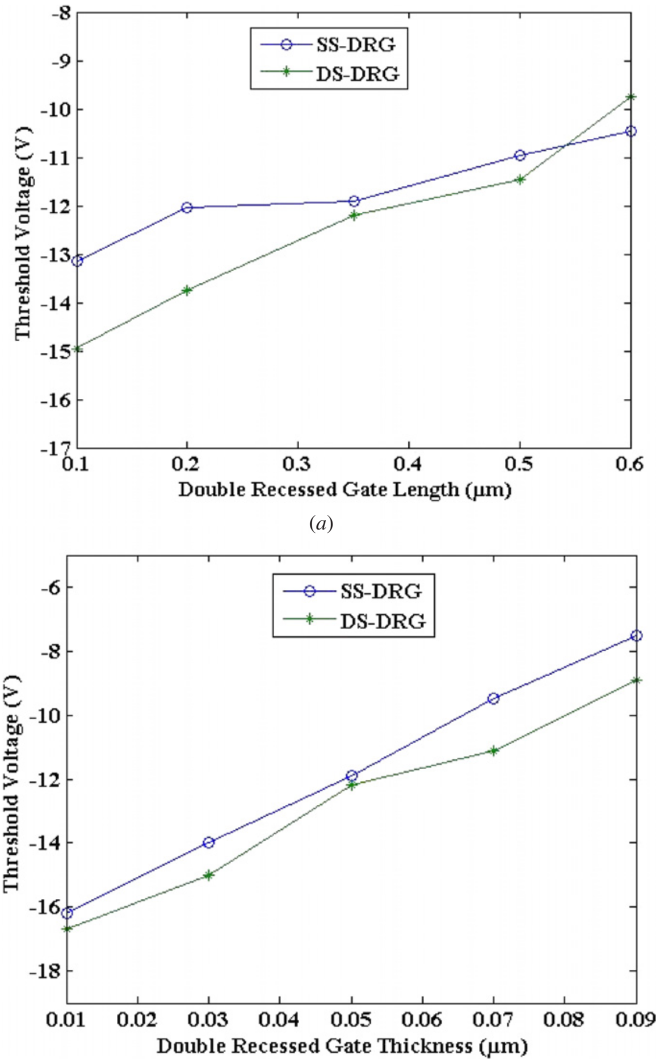
Figure 3. Drain currents as a function of drain voltages for different (*a*) L_{drg} and (*b*) T_{drg} in the SS-DRG and DS-DRG structures at $V_{\mathrm{GS}} = 0$ V.

current will decrease. It can be seen from figure 3(*a*) that drain currents for different L_{drg} in the DS-DRG structure are larger compared to those in the SS-DRG structure. This is because the region with narrow channel under the gate is in the drain side of the DS-DRG structure while in the SS-DRG structure it is in the source side. Therefore, the DS-DRG structure has better saturated drain current in comparison with the SS-DRG structure.

Figure 3(*b*) shows the drain currents as a function of different drain voltages for different T_{drg} in the SS-DRG and DS-DRG structures for $L_{\mathrm{drg}} = 0.35$ μm at $V_{\mathrm{GS}} = 0$ V. As shown in the figure, the saturated drain current decreases for the SS-DRG and DS-DRG structures when T_{drg} varies from $T_{\mathrm{drg}} = 0.01$ μm to $T_{\mathrm{drg}} = 0.09$ μm because the channel thickness under the gate is reduced. However, the DS-DRG structure has better saturated drain current compared to the SS-DRG structure for different T_{drg}, because the double recess in the DS-DRG structure is in the drain side. It is worth noting that the maximum saturated drain current for the SS-DRG and DS-DRG structures are obtained for $T_{\mathrm{drg}} = 0.01$ μm and $L_{\mathrm{drg}} = 0.35$ μm.

3.3. Threshold voltage

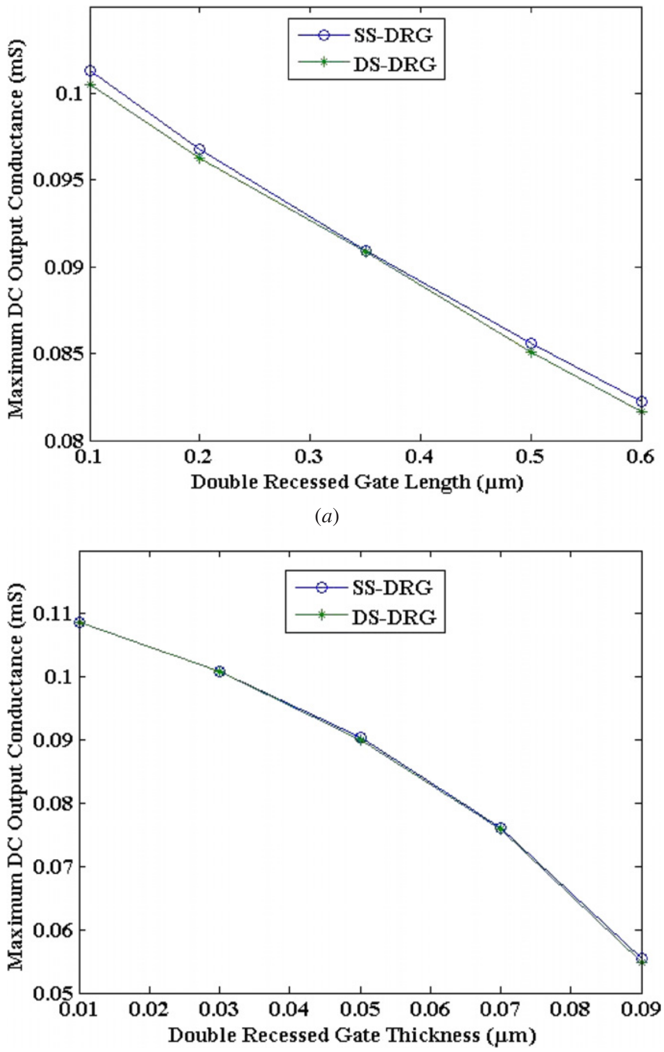
Figure 4(*a*) shows the threshold voltage as a function of L_{drg} in the SS-DRG and DS-DRG structures at $T_{\mathrm{drg}} = 0.05$ μm and $V_{\mathrm{DS}} = 10$ V conditions. As can be seen from the figure, a larger L_{drg} for the SS-DRG and DS-DRG structures increases the region under the gate with narrower channel which decreases the Schottky barrier thickness and then the threshold voltage increases. Also, the threshold voltages in the DS-DRG and SS-DRG structures have positive shift from -14.95 to -9.75 V and -13.15 to -10.45 V, respectively, with increasing L_{drg}. Therefore, the positive shift in the threshold voltage for the DS-DRG structure is larger compared with that in the SS-DRG structure.



(*a*)

(*b*)

Figure 4. Threshold voltage as a function of (*a*) L_{drg} and (*b*) T_{drg} in the SS-DRG and DS-DRG structures at $V_{\mathrm{DS}} = 10$ V.



(*a*)

(*b*)

Figure 5. Maximum dc output conductance as a function of (*a*) L_{drg} and (*b*) T_{drg} in the SS-DRG and DS-DRG structures at $V_{\mathrm{DS}} = 0$ V and $V_{\mathrm{GS}} = -1$ V.

Figure 4(*b*) shows the threshold voltages as a function of T_{drg} in the SS-DRG and DS-DRG structures at a fixed double recessed gate length ($L_{\mathrm{drg}} = 0.35\ \mu$m) and $V_{\mathrm{DS}} = 10$ V. As can be seen from the figure, the threshold voltage improves with increasing T_{drg} from 0.01 to 0.09 μm. This is due to the reduction in the channel thickness under the gate with increasing T_{drg} and therefore the vertical electric field in the channel increases under the gate. The threshold voltages in the SS-DRG and DS-DRG structures at $T_{\mathrm{drg}} = 0.09\ \mu$m are -7.5 and -8.9 V, respectively. As shown in the figure, the SS-DRG structure has better behavior compared to the DS-DRG structure because the SS-DRG structure has the narrow channel under the gate in the source side. Comparison of figures 4(*a*) and (*b*) demonstrates that the best behavior in the threshold voltage occurs in the SS-DRG structure at $T_{\mathrm{drg}} = 0.09\ \mu$m and $L_{\mathrm{drg}} = 0.35\ \mu$m conditions. It is worth noting that we determine the threshold voltage of a MESFET from a conventional definition which involves an abrupt transition between turn-on and turn-off operations [15].

3.4. DC output conductance

The output conductance (g_{o}) of the devices can be calculated by differentiating the drain–source current with respect to the drain–source voltage when the gate–source voltage is constant:

$$g_{\mathrm{o}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{DS}}} \bigg\| V_{\mathrm{GS}} = \text{const.} \tag{1}$$

It can be concluded from equation (1) that g_{o} shows the drain current dependence to the drain–source voltage for a fixed gate–source voltage.

Figure 5(*a*) shows the maximum dc output conductance as a function of L_{drg} in the DS-DRG and SS-DRG structures at $T_{\mathrm{drg}} = 0.05\ \mu$m and $V_{\mathrm{GS}} = -1$ V. As shown in the figure, the dc output conductance reduces with increasing L_{drg}. This is due to the reduction in the channel thickness under the gate which increases the vertical electric field by the gate–source voltage in the channel and then reduces the drain current dependence to the drain voltage. The maximum dc output conductance in the DS-DRG structure is smaller than that in the SS-DRG structure at a fixed T_{drg}. Therefore, the dc output conductance improves with increasing L_{drg} in the DS-DRG structure.

Figure 5(*b*) shows the maximum dc output conductance as a function of T_{drg} in the DS-DRG and SS-DRG structures at $L_{drg} = 0.35$ μm and $V_{GS} = -1$ V conditions. As can be seen from the figure, the maximum dc output conductance for the DS-DRG and SS-DRG structures is almost identical. The maximum dc output conductance decreases with increasing T_{drg} from 0.01 to 0.09 μm. Also, the maximum dc output conductance has a minimum value at $T_{drg} = 0.09$ μm. Comparison of figures 5(*a*) and (b) demonstrates that the least value in the maximum dc output conductance for the conditions we investigated occurred in the DS-DRG structure at $T_{drg} = 0.09$ μm and $L_{drg} = 0.35$ μm conditions.

4. Conclusion

Double recessed gate SiC MESFET structures with double recess in source/drain sides were simulated. The breakdown voltage, the threshold voltage, the drain current and the maximum dc output conductance for different values of double recessed gate length and thickness (L_{drg} and T_{drg}) for the SS-DRG and DS-DRG structures were simulated. Simulation results show that with increasing L_{drg} and T_{drg} in the DS-DRG structure, the threshold voltage and maximum dc output conductance improve while the saturation drain current reduces. The saturated drain current for different L_{drg} and T_{drg} in the DS-DRG structure is larger in comparison with that in the SS-DRG structure. The breakdown voltage for different L_{drg} in the DS-DRG structure is larger compared to that in the SS-DRG structure. The positive shift in the threshold voltage with increasing L_{drg} for the DS-DRG structure is higher than that for the SS-DRG structure. Also, the DS-DRG structure has smaller dc output conductance than the SS-DRG structure for different L_{drg}.

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