A 10-bit 50-MS/s redundant SAR ADC with split capacitive-array DAC

Amir Arian, Mehdi Saberi, Saied Hosseini-Khayat, Reza Lotfi & Yusuf Leblebici

Analog Integrated Circuits and Signal Processing
An International Journal

ISSN 0925-1030
Volume 71
Number 3

Analog Integr Circ Sig Process (2012)
71:583-589
DOI 10.1007/s10470-011-9812-5

Springer

Analog Integr Circ Sig Process (2012) 71:583–589
DOI 10.1007/s10470-011-9812-5

MIXED SIGNAL LETTER

A 10-bit 50-MS/s redundant SAR ADC with split capacitive-array DAC

Amir Arian · Mehdi Saberi · Saied Hosseini-Khayat · Reza Lotfi · Yusuf Leblebici

Received: 17 April 2011 / Revised: 16 November 2011 / Accepted: 30 November 2011 / Published online: 10 December 2011

Abstract A new architecture for successive-approximation register analog-to-digital converters (SAR ADC) using generalized non-binary search algorithm is proposed to reduce the complexity and power consumption of the digital circuitry. The proposed architecture is based on the split capacitive-array DAC with a simple switching logic as compared to the conventional non-binary SAR ADC architecture. A 10-bit 50-MS/s SAR ADC is designed based on the proposed architecture in a 0.18 μm CMOS technology. Simulation results show that at a supply voltage of 1.2 V, the SAR ADC achieves a peak signal-to-noise-and-distortion ratio of 59.5 dB, and a power consumption of 1.3 mW, resulting in a figure of merit of 33 fJ/conversion-step.

Keywords Digital-to-analog converter · Redundant successive approximation ADC · Redundant search algorithm · Split capacitive-array DAC · High speed SAR ADC

1 Introduction

In recent years, successive-approximation register (SAR) analog-to-digital converters (ADCs) have shown promising for implementing medium resolutions of 8–10 bits and high sampling rates of tens of MS/s with excellent power efficiency [1–5]. In SAR ADCs, when sampling rate increases, the settling time budget becomes insufficient for the capacitive DAC to stabilize. Instead of a conventional binary search, a non-binary search can be used to enable tolerating incomplete DAC settling errors. In non-binary search, there are overlaps between search ranges, compensating for wrong decisions made in earlier stages as long as they are within the error tolerance range. This approach eliminates the constraint of DAC settling accuracy to be less than 1 LSB, and thus helps to reduce the settling time. Although, non-binary search adds additional clock cycles to the conversion phase, the clock frequency can be increased to shorten the total conversion time [5]. A previous approach [6] to implement non-binary search in the SAR ADCs, was based on the geometrically non-binary scaled capacitor array DAC (see Fig. 2(a)). In that structure, the non-integer ratio of the capacitors significantly increases layout complexity. Moreover, its search algorithm is radix-restricted.

In [7], a generalized non-binary search algorithm has been presented which avoids radix restriction. However, its implementation is based on the SAR ADC with unary capacitor-array DAC, (as shown in Fig. 2(b)), which suffers from increased complexity, propagation delay and power consumption due to the overhead in required logic circuits [5, 7].

In this paper, a new redundant SAR ADC architecture based on an split capacitive-array DAC with relaxed matching and layout requirements is presented to implement the generalized non-binary search algorithm introduced in [7]. The proposed structure uses a simple switching logic circuit which leads to reduction in power consumption and propagation delay in comparison with the unary implementation making the ADC suitable for energy-efficient high-speed applications. A 10-bit 50 MS/s SAR ADC is designed in a 0.18 μm CMOS process based

A. Arian (✉) · M. Saberi · S. Hosseini-Khayat · R. Lotfi
Ferdowsi University of Mashhad, Mashhad, Iran
e-mail: arian@ieee.org

Y. Leblebici
Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

on the proposed structure. The simulation results at supply voltage of 1.2 V show that the designed SAR ADC consumes power as low as 1.3 mW.

2 Redundant search algorithm

In a redundant search algorithm which realizes an N-bit resolution SAR ADC in M comparison steps ($M \geq N$); the output digital bits are successively determined by comparing the sampled input voltage with M code-dependent voltages produced by the DAC. Assuming that the analog input voltage range is normalized to $[0, 2^N]$, in the kth comparison step, the kth bit, $b(k)$ is found by comparing the input voltage with ref(k) given in [7], as follows:

$$\mathrm{ref}(k) = 2^{N-1} + \sum_{i=2}^{k} s(i-1) \times j(i) \tag{1}$$

where $s(i)$ is equal to 1 if $b(i) =$ "1" or -1 if $b(i) =$ "0", and $j(i)$ is a positive integer value determining the voltage jump of the DAC at ith step. It can be shown that these jumps must satisfy the following [7]:

$$\begin{cases} j(1) = 1 + \sum_{i=2}^{M} j(i) = 2^{N-1} \\ 0 \leq e(i) = 1 - j(i+1) + \sum_{k=i+2}^{M} j(k) \quad 1 \leq i \leq M-1 \end{cases} \tag{2}$$

where $e(i)$ determines the maximum acceptable decision error at the ith comparison step [$e(i = M) = 0$], which still can be compensated due to the redundancy. At the end of the search, an M-bit redundant code is obtained. The output binary code can be calculated from:

$$B_{\mathrm{out}} = \sum_{i=1}^{M} b(i) \times w(i) \tag{3}$$

where $w(i)$ is the weight of the ith bit [i.e. $b(i)$] and we have derived that $w(i)$ can be obtained from:

$$w(i) = \begin{cases} 2j(i+1) & 1 \leq i \leq M-1 \\ 1 & i = M \end{cases}. \tag{4}$$

Fig. 1 shows an example of error compensation procedure for a redundant search algorithm with $N = 4$ and $M = 5$. In Fig. 1(a), for the specified input (denoted by V_{in}), all comparisons have been done correctly. But in Fig. 1(b) there is a wrong decision in the first comparison step; however this error does not exceed the first compensated range. Using (3) and (4); therefore, the search algorithm with redundancy is able to find the correct code of the input for both conditions.

It should be also noted that the redundant search algorithm is not restricted to any certain radix. Each solution of J, $J = [j(1), j(2), \ldots, j(M)]$ satisfying (2), can be used to realize an N-bit M-step redundant SAR ADC. One can select the optimal scheme among them.

3 Proposed architecture

To implement an N-bit, M-step redundant SAR ADC, it is required to generate the reference voltages given by (1) during the comparison steps. The conventional approach based on the unary capacitive-array DAC (see Fig. 2(b)) uses a digital ROM to store the jump values [i.e. $j(1), j(2), \ldots, j(M)$] and, the control logic in each comparison step i works as follows. First, $j(i)$ is read from the ROM. Based on the result of last comparison step, if $b(i-1) = 1$ then $j(i)$ is added to $ref(i-1)$ by an adder and, if $b(i-1) = 0$, then $j(i)$ is subtracted from $ref(i-1)$ by a subtractor, resulting in $ref(i)$ which is needed for the ith comparison. Finally, $ref(i)$ will be applied to the unary-weighted capacitive DAC through a binary-to-thermometer decoder to be compared with the input sampled voltage in analog domain. It should be noted that, this entire procedure must be performed in a fraction of $T_{\mathrm{CLK}}/2$ and the rest of it remains for the DAC to settle around $ref(i)$ within $[ref(i) - e(i), ref(i) + e(i)]$. The propagation delay through this control logic may be so high that it can completely destroy the advantage of using non-binary search method at high speed operation. Furthermore, its large power consumption due to the complex digital circuit (e.g. ROM, adder, subtractor) reduces the energy-efficiency of the converter.

Hence, in this paper a new N-bit M-step redundant architecture based on the split capacitive-array DAC is proposed to reduce the complexity, propagation delay and power consumption of the digital circuitry compared to the conventional unary structure. The proposed architecture, shown in Fig. 2(c) is composed of a subtractor and an adder capacitor sub-arrays. These two sub-arrays have identical capacitors, and the capacitor values for each sub-array is given by $C_k = C_{1,k} = j(k) \times C_{\mathrm{u}}$ (where $2 \leq k \leq M$). In fact, in this structure, the values of $j(i)s$ are stored in the capacitor values, i.e. it uses analog ROM instead of a digital ROM. In addition, the split architecture of the capacitive-array makes it possible to implement adder/subtracter by the DAC itself in the analog domain. When $M = N$, Eq. (2) presents $j(i) = 2^{N-i}$ and thus the redundant search algorithm is translated to the conventional binary search. Therefore, the proposed DAC will turn into a binary split array. The switching scheme of the proposed M-step architecture is similar to the binary split array presented in [8]. In the sampling phase, the input

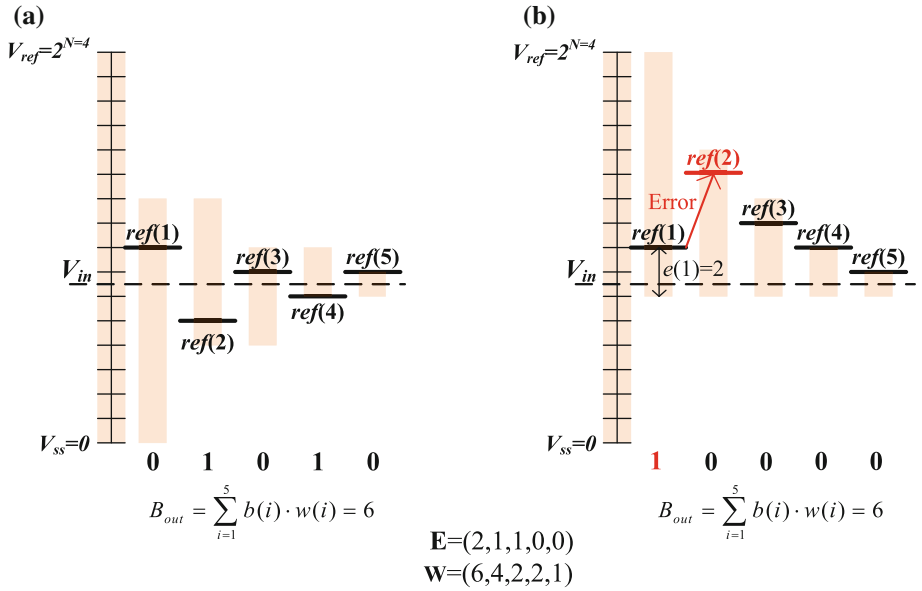

Fig. 1 An example of a redundant search algorithm with $N = 4$, $M = 5$ and the jump vector $J = (8, 3, 2, 1, 1)$. **a** All comparison steps are correct. **b** The decision error in the first comparison step which is within the error tolerance range has been compensated

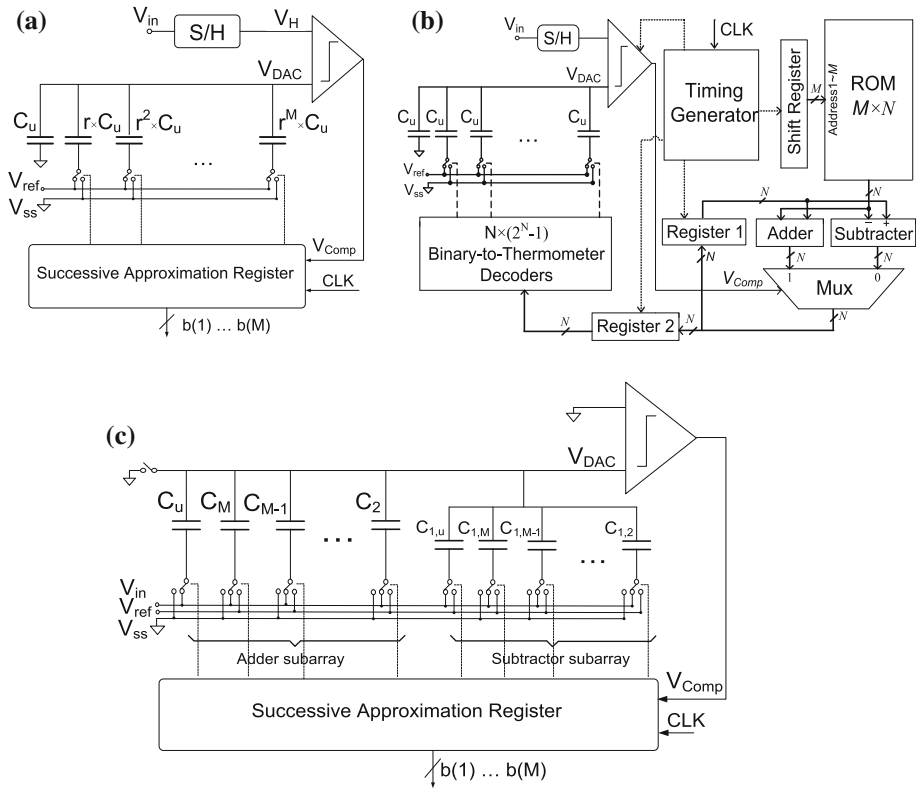

Fig. 2 Schematic of an M-step non-binary SAR ADC using **a** a non-binary scaled capacitive-array DAC, **b** a unary-weighted capacitive-array DAC, **c** the proposed split capacitive-array DAC (where $C_i = C_{1,i} = j(i) \times C_u$ and $C_{1,u} = C_u$)

voltage (i.e. V_{in}) is sampled into all capacitors. During the first step of the conversion phase, the capacitors of the subtractor sub-array ($C_{1,2}$, …, $C_{1,M}$, $C_{1,u}$) are connected to V_{ref} and the other capacitors are connected to the ground. Therefore, on account of (2), the input analog sampled voltage is compared with $ref(1) = 0.5V_{ref} = 2^{N-1}$. According to the result, $b(1)$ will be found and stored in the SAR. In the next steps, in order to determine each $b(k)$, the sampled input voltage must be compared to $ref(k)$, given by (1). Hence, in the kth step, if $b(k-1) = 1$, the kth capacitor of the adder sub-array (i.e. $C_k = j(k) \times C_u$) is connected to V_{ref}, and therefore the input sample is compared to $ref(k) = ref(k-1) + j(k)$. On the other side, if $b(k-1) = 0$ the kth capacitor of the subtractor sub-array (i.e. $C_{1,k} = j(k) \times C_u$) which is already connected to V_{ref} is connected back to the ground and thus the comparison

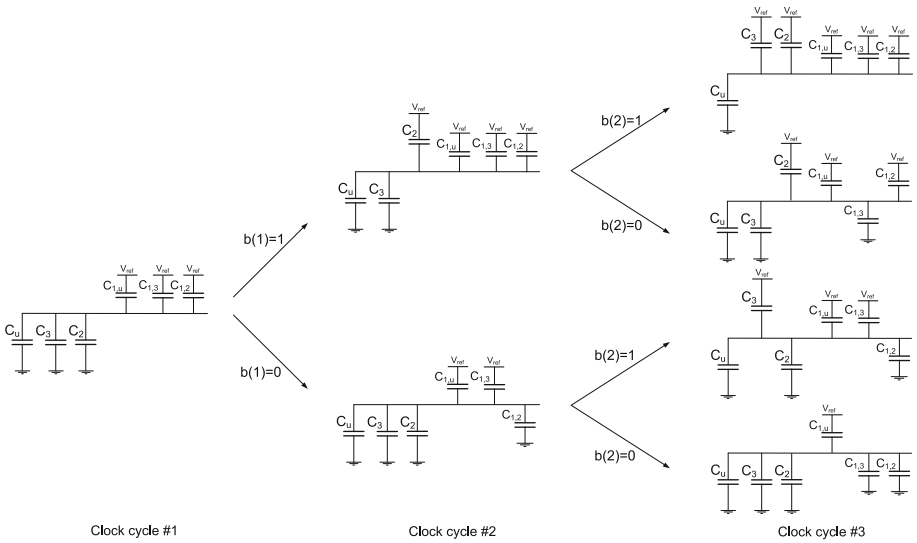

Fig. 3 Switching sequence for a 3-step proposed structure

reference is obtained as $ref(k) = ref(k-1) - j(k)$. This procedure will be repeated until all M bits are found after M comparison steps. Figure 3 shows the switching sequence of the capacitive array in a 3-step proposed DAC. The logic circuit for the proposed M-step non-binary split architecture is the same as M-bit binary split architecture. It is easy to implement and has lower power consumption and propagation delay than those of conventional non-binary ADC enabling high-speed and energy-efficient operation. It should be noted that the total capacitance of the proposed DAC is $2^N \times C_u$, identical to the N-bit conventional binary-weighted counterpart.

4 Simulation results

Using proposed architecture, a 1.2 V 10-bit 11-step, 50 MS/s single-ended redundant SAR ADC was designed and simulated at different process corners of a 0.18 μm CMOS technology. In this implementation, the logic speed is the bottleneck in achieving high-speed operation of the convertor. Hence, the control logic circuit is implemented in full custom dynamic style, which provides faster and also lower power consumption convertor. As mentioned in Sect. 2, there are many choices for vector J in a 10-bit 11-step generalized non-binary search algorithm. Our selection is based on the target of optimal speed. With this consideration, the vector J is obtained as $J = (512, 142, 172, 79, 57, 30, 16, 8, 4, 2, 1)$ resulting in the error compensated ranges vector $E = (228, 26, 40, 5, 2, 0, 0, 0, 0, 0, 0)$. The value of unit capacitor of the DAC (i.e. C_u) is set to 20 fF based on the matching requirements. The conventional dynamic comparator circuit, introduced in [9], was employed in this ADC.

Figure 4 shows the simulated output voltage of the DAC through the conversion phase for the proposed and conventional binary structures at a same high sampling rate. As seen, in the first comparison step, both structures have made wrong decisions for the specified input due to the fact that at this sampling rate neither has sufficient time in the first half of the clock period to settle to $ref(1) = 0.6$ V. However, the proposed non-binary structure has been able to compensate for this wrong decision in the next steps because this error has not exceeded the first compensated range [i.e. $e(1)$]. But the binary structure has failed to track the input and, lost converter precision due to lack of redundancy.

The total power dissipation of the proposed SAR ADC is 1.3 mW with a 1.2 V supply voltage. The power consumption of the designed control logic is 0.2 mW. The proposed redundant DAC uses metal-insulated-metal (MIM) capacitors and consumes a switching power of 0.69 mW while, the comparator takes the rest of the power. It should be noted that the proposed redundant capacitive-array provides 37% lower switching energy consumption over conventional binary-weighted case. Also it introduces better linearity performance in terms of differential non-linearity (DNL) characteristics [10].

To measure the dynamic performance of the ADC, a sine-wave input signal was applied to the convertor. Simulation results show that the ADC achieves a peak SNDR of 59.5 dB corresponding to an effective number of bits (ENOB) of 9.6 bits. The proper operation of the designed ADC in other corner process has been also verified.

Table 1 gives a performance summery of the ADC comparing it with other high speed 10-bit designs. By defining the figure-of-merit (FOM) as $FOM = \text{Power}/2^{\text{ENOB}} \times f_s$, where f_s is the sampling frequency, then the

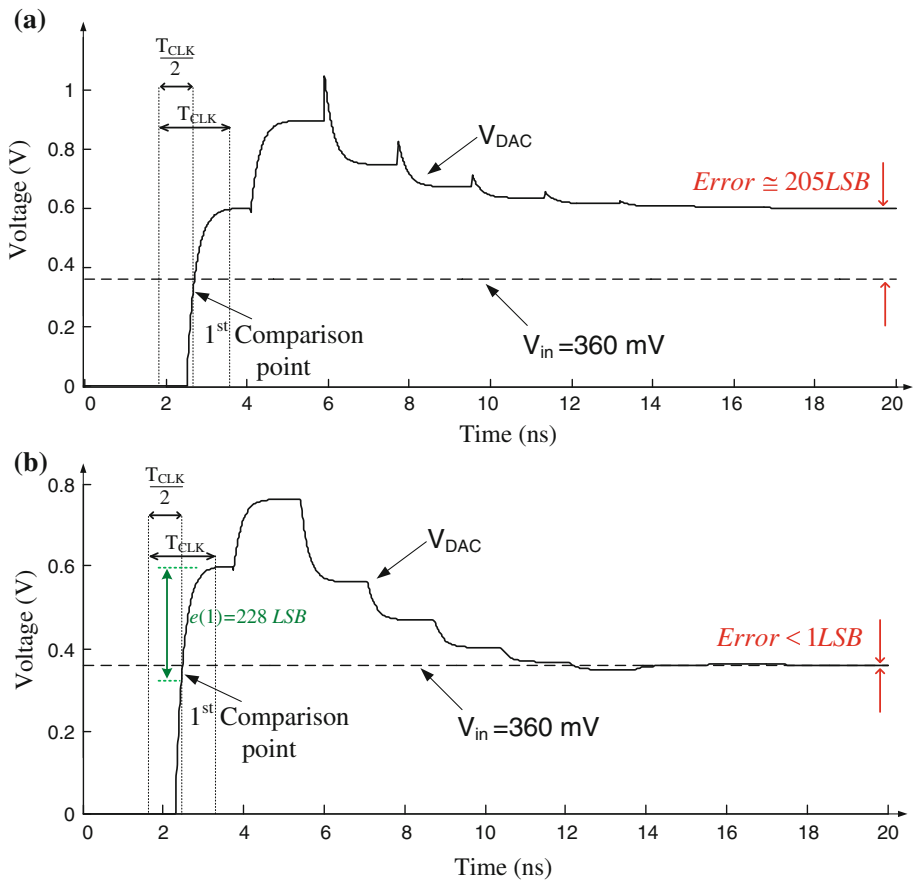

Fig. 4 Simulated operations of the convertors in a high sampling rate **a** conventional binary structure **b** proposed redundant structure

Table 1 Performance summary of the proposed SA-ADC in comparison with other high speed 10-bit SA-ADCs

	JSSC'10 [1]	JSSC'11 [2]	JSSC'10 [3]	ISSCC'10 [4]	This work
Technology	0.13 nm	0.13 μm	90 nm	65 nm	0.18 μm
Supply (V)	1.2	1.2	1.2	1.2	1.2
Sampling rate (MS/s)	50	40	100	100	50
ENOB (bits)	9.18	8.11	9.1	9.51	9.6
Power consumption (mW)	0.826	0.55	3	1.13	1.3
FOM (fJ/c-s)	29	50	55	15.5	33
Simulation/measurement	Measurement	Measurement	Measurement	Measurement	Simulation

design shows an FOM comparable to the state-of-the-art providing the measurement results. As the high-speed digital circuit benefits from technology scaling; the FOM of the proposed structure is also expected to further improve with continued technology scaling.

5 Conclusion

A new high speed non-binary SAR ADC structure has been presented to implement the generalized non-binary search algorithm. The proposed structure benefits from the simplicity of the digital and control logic circuits compared to the conventional non-binary architecture. A 1.2 V, 10-bit 50 MS/s SAR ADC was designed in a 0.18 μm CMOS process to verify the efficiency of the proposed structure. Simulation results confirm that its ENOB is 9.6 bits while consuming only 1.3 mW, and achieving an FOM as low as 33 fJ/conversion-step.

References

1. Liu, C.–C., Chang, S.-J., Huang, G.-Y., & Lin, Y.-Z. (2010). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits, 45*(4), 731–740.
2. Cho, S.-H., Lee, C.-K., Kwon, J.-K., & Ryu, S.-T. (2011). A 550-uW 10-bit 40-MS/s SAR ADC with multistep addition-only

digital error correction. *IEEE Journal of Solid-State Circuits, 46*(8), 1881–1892.
3. Zhu, Y., Chan, C.-H., Chio, U.-F., Sin, S.-W., U, S.-P., Martins, R.-P., et al. (2010). A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. *IEEE Journal of Solid-State Circuits, 45*(5), 1111–1121.
4. Liu, C.-C., Chang, S.-J., Huang, G.-Y., Lin, Y.-Z., Huang, C.-M., Huang, C.-H., Bu, L., & Tsai, C.-C. (2010). A 10 b 100MS/s 1.13 mW SAR ADC with binary-scaled error compensation. In *Proceedings of IEEE ISSCC Digest of Technical Papers* (pp. 386–387). San Francisco.
5. Kuttner, F. (2002). A 1.2 V 10 b 20 M sample/s non-binary successive approximation ADC in 0.13 μm CMOS. In *Proceedings of* IEEE *ISSCC* (pp. 176–177). San Francisco.
6. Gan J., & Abraham, J. (2002). Mixed-signal micro-controller for non-binary capacitor array calibration in data converter. In *Proceedings of IEEE Signals, Systems and Computers Conference* (pp. 1046–1049). Pacific Grove, CA.
7. Ogawa, T., Kobayashi, H., Takahashi, Y., Takai, N., Hotta, M., San, H., et al. (2010). SAR ADC algorithm with redundancy and digital error correction. IEICE TRANS. *Fundamentals, E93-A*(2), 415–423.
8. Ginsburg, B. P., & Chandrakasan, A. P. (2007). 500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array ADC. *IEEE Journal of Solid-State Circuits, 42*(4), 739–746.
9. Kobayashi, T., Nogami, K., Shirotori, T., & Fujimoto, Y. (1993). A current controlled latch sense amplifier and a static power-saving input buffer for low-power architecture. *IEEE Journal of Solid-State Circuits, 28*(4), 523–527.
10. Arian, A., Saberi, M., & Hosseini-Khayat, S. (2011). SAR ADC with redundancy using split capacitive-array DAC. In *ICEE*, Tehran.

Amir Arian received B.S. degree in electrical and electronics engineering from Azad University of Bojnourd, Bojnourd, Iran, in 2007. He is currently working toward the M.S. degree at Ferdowsi University of Mashhad, Mashhad, Iran. His research interests include Nyquist ADC and low-power integrated circuits design. Currently, his research mainly focuses on SA algorithm and design of ultra low-power SAR ADC.

Mehdi Saberi received the B.S. and M.S. degrees (both with honors) in electrical engineering from Ferdowsi University of Mashhad, Mashhad, Iran in 2005 and 2007, respectively. Since then, he has been a Ph.D. student in EE department, Ferdowsi University of Mashhad. As his Ph.D. research program, he is currently working on design of low-power analog-to-digital converters for biomedical applications. Since 2011, he has been with Swiss Federal Institute of Technology, Lausanne (EPFL) as a visiting student.

Saied Hosseini Khayat holds a BS degree in electrical engineering from Shiraz University, Iran, and MS and PhD degrees in electrical engineering, and Washington University in St. Louis, USA. He has held technical positions at Globespan Semiconductor Inc., Redbank, NJ, and Erlang Technologies Inc., St. Louis, MO, USA. His interest and expertise lie in the area of digital circuit and system design, in particular, resource-efficient hardware implementation of DSP, networking and cryptographic algorithms. At present, he is an associate professor at Ferdowsi University of Mashhad, Iran.

Reza Lotfi (M'05) received his B.Sc from Ferdowsi University of Mashhad, I.R. Iran, his M.Sc from Sharif University of Technology, Tehran, I.R. Iran and his Ph.D. from University of Tehran, Tehran, I.R. Iran, all in Electrical Engineering, in 1997, 1999 and 2004, respectively. Since, 2004 he has been with Ferdowsi University of Mashhad, I.R. Iran as assistant professor where he founded the Integrated Systems Lab. From 2008 to 2009, he was with Electronics Research Lab., Delft University of Technology, Delft, The Netherlands as a post-doctoral scientific researcher working on ultra-low-power analog and mixed-signal integrated circuits for biomedical applications. Since 2010, he served as an Associate Editor for the IEEE transactions on circuits and systems—I: Regular Papers. His research interests include low-voltage low-power analog integrated circuit design for biomedical applications as well as high-speed data converters for telecommunication systems.

Yusuf Leblebici (M'90-SM'98-F'10) received the B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, Turkey, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990. Between 1991 and 2001, he was a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000–2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, he has been a Chair Professor at the Swiss Federal Institute of Technology, Lausanne (EPFL), and Director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of five

textbooks: *Hot-carrier reliability of MOS VLSI circuits* (Kluwer Academic Publishers, 1993), *CMOS digital integrated circuits: analysis and design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS multichannel single-chip receivers for multi-gigabit optical data communications* (Springer, 2007), *Fundamentals of high frequency CMOS analog integrated circuits* (Cambridge University Press, 2009), and *Extreme low-power mixed signal IC design: subthreshold source-coupled circuits* (Springer, 2010), as well as more than 200 articles published in various journals and conferences. Dr. Leblebici has served as an Associate Editor of the IEEE transactions on circuits and systems—PART II and the IEEE Transactions on very large scale integrated (VLSI) systems. He has also served as the General Cochair of the 2006 European solid-state circuits conference, and the 2006 European solid state device research conference (ESSCIRC/ESSDERC). He has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.