# Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications

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***Abstract*—In this paper, an in-depth design methodology for fully-integrated tunable low-noise amplifiers for neural recording applications is presented. In this methodology, a modified system design is proposed to optimize the area/noise/linearity performance. A novel linear pseudo-resistor with a wide range of tunability is also proposed. As a case study, a low-noise tunable and reconfigurable amplifier for neural recording applications is designed and simulated in a 0.18 $\mu$m complementary metal–oxide–semiconductor process in all process corners. Simulated characteristics of the amplifier include tunable gain of 54 dB, tunable high-cutoff frequency of 10 kHz, programmable low-cutoff frequency ranging from 4 to 300 Hz, and power consumption of 20.8 $\mu$W at 1.8 V. According to postlayout simulations, integrated input-referred noise of the amplifier is 2.6 $\mu\mathrm{V_{rms}}$ and 2.38 $\mu\mathrm{V_{rms}}$ over the 0.5 Hz–50 kHz frequency range for low-cutoff frequency of 4 and 300 Hz, respectively. The amplifier also provides output voltage swing of 1 $\mathrm{V_{P-P}}$ with total harmonic distortion of -46.24 dB at 300 Hz, and -45.97 dB at 10 kHz.**

***Index Terms*—Biomedical sensor interface, neural recording, pseudo resistor, tunability.**

## I. Introduction

BIO-POTENTIAL amplifiers are among the most critical blocks in neural recording systems used by neuroscientists in various biomedical applications including brain–machine interfaces and neural prostheses. The main challenges in the design of the analog front-end of sensor interface (SI) circuits are derived from the nature of neural signals. Due to their rather small amplitude, neural signals need to be amplified before they are digitized or processed. An integrated front-end amplifier (FEA) should have sufficiently low input-referred noise to allow the detection of neural signals as small as a few tens of micro-Volts in amplitude. Also, the amplifier must have sufficient dynamic range for large-amplitude input signals (1–2 mV). Since the peak amplitude of neural signals varies based on the electrode type and conditions, the gain of the amplifier needs to be programmable. Useful frequency spectrum of neural signals is spread from a few Hertz to a few kilo-Hertz. Neural signals include local field potentials (LFP) containing slowly-varying low-frequency components as well as action potentials (neural spikes) with frequency contents in the 300 Hz–10 kHz range. Furthermore, the electrode-tissue interface usually causes a high dc offset in the input signal, which has to be removed by a high-pass filter not to saturate the amplifier [1], [2].

To minimize attenuation of the input signal, input impedance of the SI circuit needs to be higher than the equivalent impedance of the electrode–tissue interface. Also, the amplifier should have a high common-mode rejection ratio (CMRR) and a high power-supply rejection ratio (PSRR) to minimize any interference from 50/60 Hz power line noise and power supply noise. If tissue cells are exposed to elevated temperatures for a long time, they will be damaged [2]. Thus, the SI circuit needs to operate at low power levels to minimize tissue heating. In addition, the SI circuit should consume small silicon area and use few off-chip components to minimize the implant size [2].

Also, the amplifier circuit parameters, including both active and passive components, may change with process variations. Therefore, bandwidth of the amplifier needs to be tunable as well.

Another design issue in SI circuit is the linearity of the amplifier. Not only the linearity of the resistors, usually implemented employing MOS pseudo-resistors, but also the tracking error of the amplifier affect the linearity of the FEA. Although several attempts have been reported to both decrease the power consumption and increase the signal-to-noise-ratio of biomedical sensor interface systems [1]–[4], only a few works have discussed the linearity of these systems [1], [5].

This paper presents an integrated tunable neural recording sensor interface amplifier. As illustrated in Fig. 1, the amplifier received neural signals from microelectrodes, and delivers the preconditioned signal to the following block in the recording path, which is an analog-to-digital converter (ADC). The structure of the FEA including a low-noise amplifier, a tunable band-pass filter, and a variable gain amplifier (VGA) is modified in order to optimize the noise, linearity, and area performance. The designed FEA amplifies the neural signals in two frequency modes. The frequency band of the first mode is ranging from 300 Hz to 10 kHz. The LFP component of the neural signals, therefore, removed in this configuration. In this mode, the low-

Manuscript received June 16, 2011; revised October 08, 2011; accepted October 16, 2011. Date of publication December 06, 2011; date of current version February 01, 2012. This paper was recommended by Guest Editor M. Sawan.

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Digital Object Identifier 10.1109/JETCAS.2011.2174492

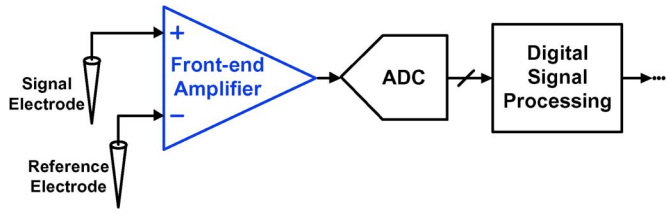


Fig. 1. Block diagram of the recording path in a neural recording system.

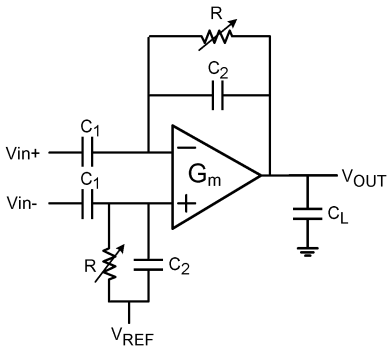


Fig. 2. Schematic of a capacitively-coupled single-stage neural amplifier.

and high-cutoff frequencies and the mid-band gain are tunable. In order to be able to amplify LFP signals (located around a few Hertz to a few hundreds of Hertz) as well as neural spikes, frequency band for the second mode covers a wider range from 4 Hz to 10 kHz. It is worth noting that a low-cutoff frequency of 4 Hz is sufficient for a variety of applications such as most of the useful biomarkers for deep-brain stimulation applications and neural prostheses [6]. In this mode, unlike the low-cutoff frequency (which is fixed in our design), the high-cutoff frequency and mid-band gain are tunable. Also, a novel pseudo-resistor structure is introduced, which enables both coarse tunability of the low-cutoff frequency (4 Hz/300 Hz mode selection) and fine tunability of the low-cutoff frequency (only in the first mode) of the amplifier with sufficient linearity.

The paper is organized as follows. Section II describes the challenges in the design and architecture of the system. In Section III, different alternatives for realizing pseudo resistors are discussed and a tunable yet linear structure is proposed. Section IV reports the simulation results, and Section V concludes the paper.

## II. Sensor Interface Circuit Design Methodology

In this section, design considerations for a fully on-chip low-noise FEA for neural recording applications with low- and high-cutoff frequencies of 4/300 Hz and 10 kHz are discussed. The overall FEA gain should be programmable with a nominal value of 54 dB. Designed in a 0.18-$\mu$m complementary metal–oxide–semiconductor (CMOS) technology with a supply voltage of 1.8 V, output voltage swing of the FEA is chosen to be 1 $V_{p-p}$. Driving capability of the FEA is determined by the following block, which is a successive approximation register (SAR) ADC. In this design, the amplifier should be able to drive a switched capacitor of 20 pF.

In the literature, several reports have been presented to implement FEAs for implantable biomedical devices with both

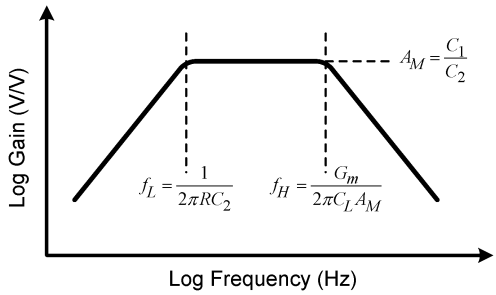


Fig. 3. Frequency response of the amplifier of Fig. 2.

single stage [2], [4], [5], [7]–[9] and multistage architectures [1], [3], [10]–[14] which are mostly capacitively coupled to the preceding microelectrode. The FEA is commonly realized using a single-stage capacitively-coupled amplifier shown in Fig. 2, which is used as a building block of multistage architectures. Fig. 3 demonstrates the gain of the capacitively-coupled amplifier versus frequency. If the low-frequency voltage gain of the operational transconductance amplifier (OTA) of the FEA is much larger than $C_1/C_2$, then the mid-band gain of the FEA $(A_M)$ is approximately equal to $C_1/C_2$ and the low-cutoff frequency of the amplifier is approximately equal to

$$f_L = \frac{1}{2\pi RC_2}. \tag{1}$$

Assuming that $C_1$ is much larger than both $C_2$ and the input parasitic capacitance of the OTA, $C_L$ is larger than both $C_2$ and the output capacitance of the OTA, and that the dominant pole of the OTA is determined at the output node, the high-cutoff frequency of the amplifier is approximately equal to

$$f_H = \frac{G_m}{2\pi A_M C_L} \tag{2}$$

where $G_m$ is the OTA transconductance. The choice of the number of the stages for the amplifier and the specifications of each stage greatly affects the overall system performance.

### A. System Design Challenges

Before dealing with general issues concerning the configuration of the FEA, there is a point regarding the resistors used in FEAs for neural recording that contributes to our discussion here. To design a fully integrated FEA with a rather low-cutoff frequency, very high resistances are needed. To realize such resistances, MOS pseudo-resistors are good candidates occupying very small silicon area [7]. The main drawback of these resistors is their nonlinear behavior discussed in the next section.

As mentioned earlier in this section, one of the key decisions in the design of an FEA is on the number of stages used.

*Single-Stage Configuration:* If the amplifier is designed with a single stage (Fig. 2), since the entire gain needs to be realized using a single stage as

$$A_M = \frac{C_1}{C_2} \tag{3}$$

keeping $C_2$ at minimum, $C_1$ needs to be rather large. This results in low input impedance and large chip area for the SI circuit. It

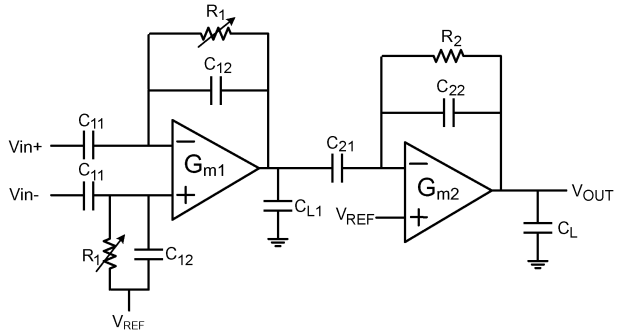


Fig. 4. Schematic of a capacitively-coupled two-stage neural amplifier.

should be noted that although $C_2$ is usually very small, it still needs to be well above neighboring parasitic capacitances.

Furthermore, in the single-stage configuration, linear tracking speed of the FEA output is limited by the effective bandwidth of the input signal [1]. In other words, since the high-cutoff frequency of the amplifier is limited and the load capacitance is relatively large, an extra buffer stage will be needed between the amplifier and the next stage in order for the amplifier to exhibit suitable settling behavior.

*Two-Stage Configuration:* To overcome the problems associated with the single-stage scheme, two-stage configuration was proposed in [1]. In this configuration that is shown in Fig. 4, the first stage is functioning as a tunable band-pass filter that determines both low- and high-cutoff frequencies of the amplifier, and the second stage is a VGA driving the load, i.e., the following ADC block. It can be shown that the total rms thermal noise referred to the input of the amplifier is equal to

$$V_{ni,\mathrm{rms}} \approx \sqrt{\frac{4kT(1+E)}{3(C_{12}+C_{21}+C_{L1})A_M}} \tag{4}$$

where $k$ is Boltzmann's constant, $T$ is the absolute temperature, and $E$ is the architecture-dependent excess noise factor due to the other devices of the OTA. This is, of course, ignoring the flicker noise, the pseudo resistor noise, and the VGA noise, and assuming that the transconductance of the first stage OTA is equal to that of the input-pair transistors of the OTA (that is valid for many structures). Assuming that the area of the amplifier is dominated by the capacitors of Fig. 4, the layout area will be proportional to the total capacitance of the amplifier

$$C_T = 2C_{11} + 2C_{12} + C_{L1} + C_{21} + C_{22}. \tag{5}$$

Deriving $C_{12}+C_{21}+C_{L1}$ from (4) and substituting it into (5), total capacitance of the amplifier is achieved as a function of input-referred noise, mid-band gain, $C_{12}$ and $C_{22}$. Hence, the optimum mid-band gain that minimizes the total capacitance for given input-referred noise, $C_{12}$ and $C_{22}$ can be calculated [2]. As a numeric example, for a practical $V_{ni,\mathrm{rms}}$ of 2.5 $\mu$V and $C_{12}=C_{22}=200$ fF, an approximate mid-band gain of 50 V/V for the first stage is needed to minimize the total capacitance. This leads to $C_{L1}+C_{21}=17.5$ pF, $C_{11}=10$ pF and $C_T=38.1$ pF. If a total mid-band gain of 500 is desirable, the input capacitor of the VGA will be 2 pF and a 15.5 pF capacitor should be placed at the output of the first stage as the load $(C_{L1})$. This additional capacitor has been used in [7], [11], and [15]. Because of setting the high-cutoff frequency in the first stage, a large load or compensation capacitor for the first stage is needed. This, however, leads to increased circuit area.

The high-cutoff frequency is recommended not to be realized in the first stage. This is to avoid an additional capacitor in the first stage for this purpose. It is not preferred to set the high-cutoff frequency in the second stage either, because it reduces settling speed of the amplifier. As a result, it is proposed to insert an intermediate stage between the first and the second stages in order to set the high-cutoff frequency of the amplifier.

*Three-Stage Configuration:* It was explained that in a well-designed three-stage amplifier, it is the second stage that sets the high-cutoff frequency. Using this intermediate stage can also contribute to lowering the input referred noise of the amplifier. The reason is as follows: The low-cutoff frequency can be realized using a tunable pseudo-resistor. Below a certain frequency, referred to as the noise corner frequency, $f_{\mathrm{corner}}$, hereafter, the noise contribution from the pseudo-resistors used in the circuit dominates the thermal noise of the OTA [2]. Among the pseudo resistors used in the amplifier, the one that sets the low-cutoff frequency of the amplifier dominantly causes a large value for $f_{\mathrm{corner}}$ and consequently a large amount of noise power (specifically where the low-cutoff frequency is set to 300 Hz). To reduce the noise contribution of this tunable pseudo-resistor, the low-cutoff frequency is recommended not to be set by the first stage. The tunable pseudo-resistor is not used in the third stage either. This is because of the large voltage swing and consequently the nonlinear operation it would experience which will be explained in the following section. Therefore, the second stage is a suitable place to set the low-cutoff frequency of the amplifier.

Gain tunability can be implemented in each one of the stages using a variable input or feedback capacitor. Variability of an input capacitor has two drawbacks: first, to realize a rather large gain, the input capacitor needs to be much larger than the feedback capacitor. As a result, a variable input capacitor occupies larger area than the case where the feedback capacitor is variable. Secondly, the capacitor at the input of each stage performs as the load for the previous stage. Variation of a capacitor at the input of each stage, therefore, affects the behavior of the preceding stage. In each stage, the feedback capacitor is smaller than the load capacitor and, therefore, does not affect the circuit performance. The second stage is not suitable to realize the tunability of the gain. This is because the low-cutoff frequency of the amplifier depends on the second stage feedback capacitor. The third stage is, therefore, the best place to realize a tunable gain since the effect of the variations of the gain of this stage on the input-referred noise of the entire system is much less than that of the other stages.

### B. The Proposed Structure

The structure proposed for a neural amplifier is shown in Fig. 5. The SI circuit consists of three stages: a low-noise amplifier (LNA), a band-pass filter (BPF), and a variable gain amplifier (VGA).

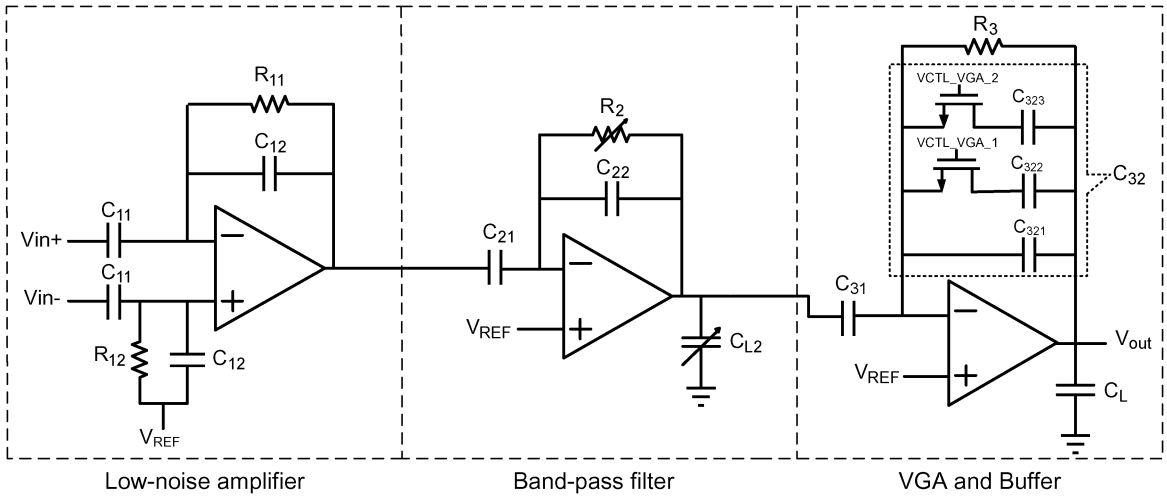


Fig. 5. Schematic of the proposed three-stage amplifier.

At the input of the first stage, a differential neural signal is capacitively coupled to the amplifier. This is to reject the dc polarization of the signals received from the electrodes. The capacitance ratio of $C_{11}/C_{12}$ is used to set the gain $(G_1)$ using a negative feedback loop. $R_{11}$ and $R_{12}$ are large fixed (i.e., nontunable) pseudo-resistors. The low-cutoff frequency of this stage [i.e., $1/(2\pi.R_{11}C_{12})$] is much lower than that of the overall system. $V_{\rm REF}$ is a reference voltage that sets the common-mode voltage components at both the input and output of the OTA through $R_{11}$ and $R_{12}$. The OTA and the pseudo-resistors are the main sources of the first-stage noise, significantly contributing to the overall input-referred noise of the amplifier. A single-stage amplifier is used as the first stage OTA. The OTA noise can be minimized by increasing the transconductance of the OTA (i.e., $G_{m1}$) and proper transistor sizing. Therefore, the high-cutoff frequency of the first stage is larger than the neural signal bandwidth. Also the flicker noise power is minimized by using PMOS transistors with large enough gate areas as input devices. To minimize the noise contribution by the pseudo-resistors, $f_{\rm corner}$ must be lowered as much as possible. According to [2], $f_{\rm corner}$ is obtained as

$$f_{\rm corner} \approx \frac{1}{2\pi C_{11}} \sqrt{\frac{3G_{m1}}{2R_{11}(1+E_1)}} \tag{6}$$

which is inversely proportional to $C_{11}\sqrt{R_{11}}$. Thus, both $C_{11}$ and $R_{11}$ need to be chosen as large as possible. Note that there is a trade-off between $f_{\rm corner}$ and the input impedance of the amplifier.

The second stage of the amplifier is a tunable band-pass filter removing the low- and high-frequency content of the neural signal. Employing the tunable pseudo-resistor, $R_2$, the low-cutoff frequency of the overall system [i.e., $1/(2\pi.R_2C_{22})$] is made tunable using two digital bits. The structure of this pseudo-resistor will be explained in the following section. The capacitor $C_{L2}$ is implemented using two metal–insulator–metal (MIM) capacitors and two switches. The high-cutoff frequency of the entire system is tuned using two other digital bits. A current-mirror amplifier [2] is used as the second stage OTA.

The third stage is a VGA loaded by the rather large input capacitance of an ADC. The gain of this stage $(G_3)$ is equal to $C_{31}/C_{32}$, where $C_{32}$ is the equivalent feedback capacitance that is controlled by two digital bits. $R_3$ is a large fixed pseudo-resistor that sets the input common-mode voltage of the OTA. For the third stage, a two-stage OTA is used. In order to minimize the tracking error of the closed-loop amplifier, high-transconductance OTA should be used. So, the high-cutoff frequency of this stage is set larger than the input neural signal bandwidth.

As for the distribution of the power among the three stages, it should be noted that the first stage is a low-noise amplifier and consumes the most power to satisfy the noise requirement. The second stage has much less contribution in the total input-referred noise and thus consumes much less power. Finally, since the third stage has negligible noise contribution but must drive a large capacitive load (the ADC input capacitance), its power consumption lies somewhere between those of the first and the second stages. It is worth noting that when the amplifier does not have to drive a large switched-capacitor load, the third stage will no longer be needed, and the amplifier can be implemented using two stages.

The optimum distribution of the voltage gain over the three stages has been derived using a MATLAB code as $G_1 = 50$, $G_2 = C_{21}/C_{22} = 2$, and $G_3 = 5$ to minimize the input-referred noise and area. By realizing the gain of the entire amplifier in three stages using the ratios of the capacitors, one can readily conclude that the area of the entire SI circuit, dominated by the capacitors, will be reduced [10].

## III. Pseudo-Resistor Implementation

As explained in the previous section, high-valued resistors are used in all the three stages of the proposed amplifier. Pseudo-resistors are suitable candidates for implementing such large resistances with acceptable area. The first and the last stages need fixed pseudo-resistors, and the second stage needs a tunable pseudo-resistor for controlling the low-cutoff frequency of the amplifier.

Several electrical and physical issues should be considered in the design of pseudo-resistors, including simple implementation, small chip area, and small parasitic capacitance. They

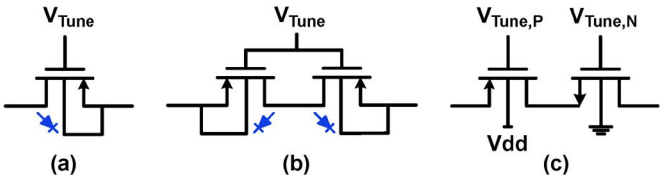


Fig. 6. Voltage-controlled pseudo-resistor structures: (a) gate-voltage controlled MOSFET, (b) gate-voltage-controlled back-to-back MOSFETs (BBMOS), and (c) complementry structure.

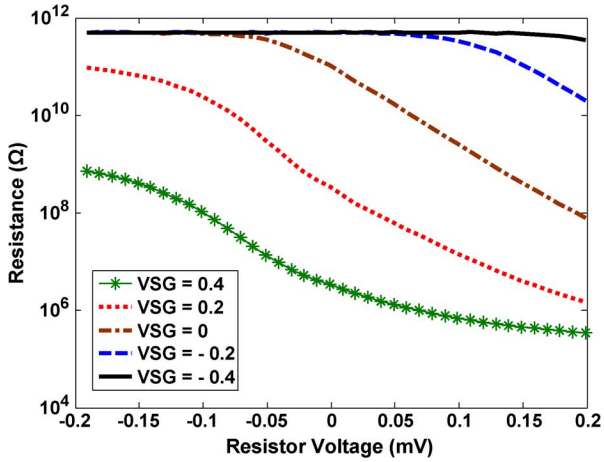


Fig. 7. Resistance variations versus the voltage across the resistor of Fig. 6(a).

should also have minimal effect on the total system characteristics in terms of noise and distortion. In order to reduce the distortion imposed by these resistors, they should have a linear characteristic exhibiting symmetric variation around the quiescent point. Besides, the variations of the resistance over the entire voltage swing range and over the frequency band should be low. Also, the resistance should be minimally sensitive to process variations, OTA offset, and dc common-mode variations. Note that tunable pseudo-resistors need to be equipped with one or more simple digital-to-analog converters (DAC) to be digitally tuned.

### A. *Tunable Pseudo Resistors*

There are various types of structures for implementing tunable pseudo-resistors. The first type employs voltage-controlled resistors. One of the simplest structures for this type is the gate-voltage-controlled MOSFET shown in Fig. 6(a) [4]. This structure is easy to implement and easily tunable by using only one simple DAC. It has a low added parasitic capacitance and very low added noise. Also the equivalent resistance in this structure can be tuned over a wide range by varying the $\mathrm{V_{SG}}$ of the transistor from positive to negative values.

If the equivalent resistance is set to be very high by using a suitable negative $\mathrm{V_{SG}}$, the drain-source leakage current would be very low. In this case, the drain-bulk junction (as shown in Fig. 6) of the transistor contributes considerably in the operation of the device [16] and can even dominate the device behavior. This results in a small variation of the equivalent resistance around the quiescent point, as shown in Fig. 7. In order to make the resistance characteristic approximately symmetric, the resistor structure can be modified to the form presented in Fig. 6(b), which operates as two back-to-back diodes in this situation.

On the other hand, as shown in Fig. 7, if the equivalent resistance is set at a moderate value by using a small negative or a positive $\mathrm{V_{SG}}$, the drain-source leakage current affects the operation of the device. As a result, equivalent resistance characteristic will not be symmetric around the quiescent point and the resistance experiences large variations over the resistor voltage swing range. In order to set the low-cutoff frequency of the second stage at 300 Hz, the equivalent resistance of the associated pseudo resistor needs to be at a moderate value of about a few giga-Ohms and so the pseudo-resistor characteristic is not symmetric. Therefore, by using this architecture, the linearity of the amplifier at around the low-cutoff frequency of 300 Hz will be degraded. The resistor, however, has little impact on the linearity at high frequencies. For example, in this case, the total harmonic distortion (THD) of the entire circuit is $-46.5$ dB at the input frequency of 10 kHz but it is about $-20$ dB at around the low-cutoff frequency (300 Hz). Also the resistance is sensitive to process variations, OTA offset and common-mode voltage variations.

The second voltage-controlled structure is a complementary scheme composed of one NMOS and one PMOS transistor as shown in Fig. 6(c) [8]. This structure is more complicated than a single transistor because two separate control voltages, $V_{\mathrm{Tune},P}$ and $V_{\mathrm{Tune},N}$, are needed to tune the resistor. The designer can adjust these two voltages for achieving symmetric variations around the quiescent point. But this symmetry is very sensitive to process variations and any other changes in the OTA common-mode voltage as well as its offset voltage. Therefore, although a resistor of this type exhibits low added parasitic capacitance, very low added noise, and a good linearity both in low and high frequencies at the tuned point, it can hardly be a suitable choice in a realistic design.

The next type of tunable pseudo-resistors is the current-controlled resistors. The simplest structure of this type is the current-controlled single-transistor shown in Fig. 8(a) [5]. The current-controlled transistor structure is simple to implement and can be easily tuned. It has low added parasitic capacitance and noise. Resistance variations around the quiescent point is, however, not completely symmetric leading to poor linearity at low frequencies (simulated value of THD is higher than $-10$ dB around the low-cutoff frequency of 300 Hz). Although this structure is sensitive to process variations, it is not sensitive to OTA dc common-mode variations and offset. Based on this feature, a symmetric and low-sensitive cross-coupled structure is proposed in [1]. This structure, shown in Fig. 8(b), can be easily implemented and tuned. It shows roughly symmetric resistance variations around the quiescent point in all process corners and thus a good linearity. Also, the sensitivity of this resistor structure to process variations is low. Finally, this structure is insensitive to common-mode variations and the offset of the OTA.

Despite the desired operation of the cross-coupled pseudo-resistor in terms of sensitivity, variations of the resistance around the quiescent point is not completely symmetric, resulting in an

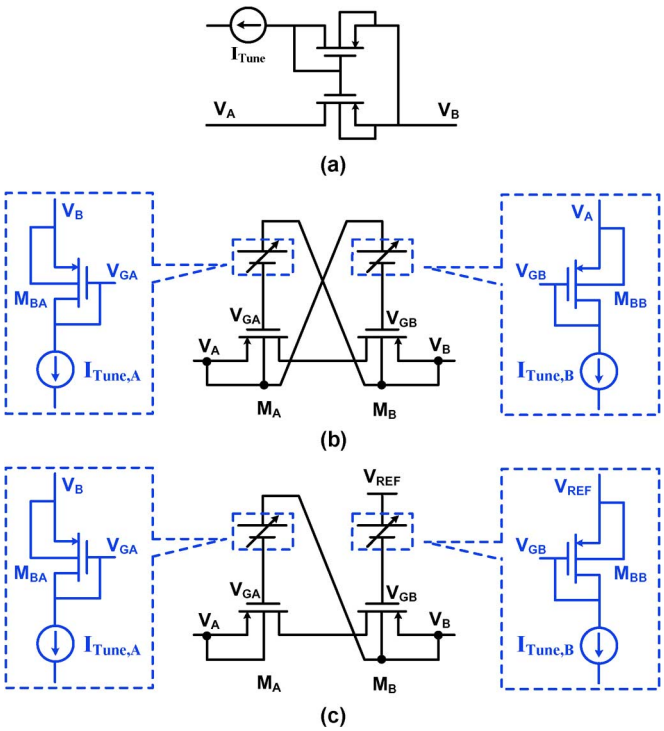


Fig. 8. Current-controlled pseudo-resistors: (a) current-controlled single transistor, (b) cross-coupled structure, and (c) pseudo cross-coupled structure.

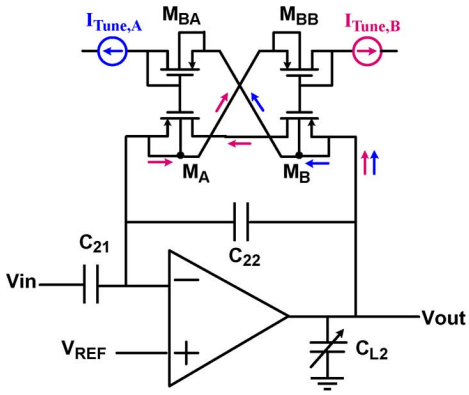


Fig. 9. Second-stage amplifier employing a cross-coupled pseudo-resistor to tune the low-cutoff frequency.

unwanted increase in the THD value. Furthermore, this structure imposes a high amount of excess noise to the amplifier. To illustrate the problem, suppose that the node $\mathrm{V_A}$ in Fig. 8(b) is connected to the inverting input of the OTA and the node $\mathrm{V_B}$ is connected to the output of the OTA, as shown in Fig. 9. Then, the current $I_{\mathrm{Tune},B}$ is drawn from the OTA output via the resistor.

The dc current flow through the transistors $\mathrm{M_A}$ and $\mathrm{M_B}$ increases their transconductance dramatically, consequently increasing the current noise spectral density of these transistors. Also, the effect of the noise power of the biasing transistors ($\mathrm{M_{BA}}$ and $\mathrm{M_{BB}}$) on the total output noise increases, as it is directly proportional to the transconductance of the transistors $\mathrm{M_A}$ and $\mathrm{M_B}$. These two issues lead to more than 40% increase in the resistor noise voltage when referred to the input of the stage. On the other hand, the dc current flow through the resistor

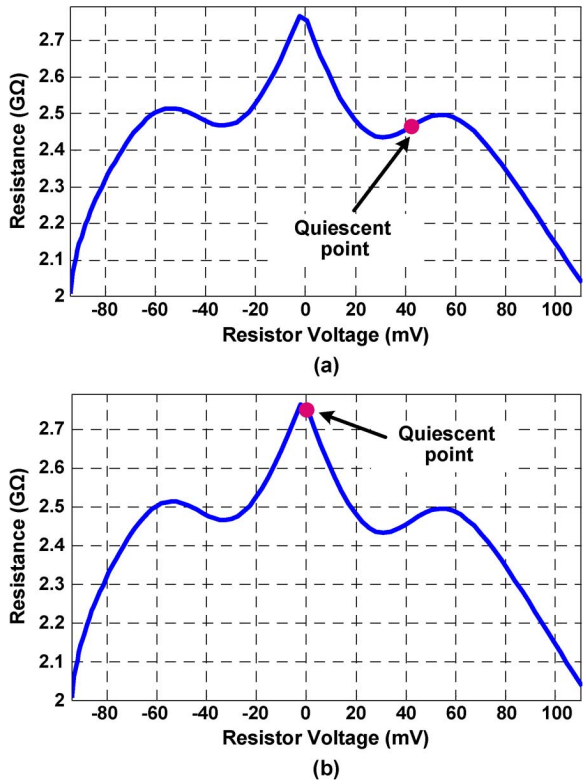


Fig. 10. Resistance variations of the pseudo resistor versus the voltage across the resistor for (a) cross-coupled structure, and (b) pseudo cross-coupled structure.

leads to a voltage difference between the OTA input and the output common-mode voltages. In order to reduce this voltage difference to tens of milli-volts, $I_{\mathrm{Tune},B}$ should be chosen small enough (down to few tens of pico-amperes). This makes the design of the stable DAC hardly possible. In addition, the dc voltage across the resistor degrades the resistor linearity. In order to illustrate the problem, the simulated resistance is plotted in Fig. 10(a) as a function of the voltage difference across the resistor. As it can be seen, resistance variations around the zero voltage are symmetric and any dc voltage across the resistor (even in the order of few tens of millivolts) will result in asymmetry.

To avoid any dc current flow into the resistor, the modified structure shown in Fig. 8(c) can be used. Since $V_A$ is the voltage at the input node of the OTA with very small transient variations, the control voltage of $\mathrm{M_B}$ can be connected to a fixed dc voltage, $V_{\mathrm{REF}}$, equal to the dc level of $V_A$. This pseudo cross-coupled structure offers all the advantages of the cross-coupled structure of Fig. 8(b). Using this biasing structure, no dc current flows through the resistor and thus no dc voltage appears across the resistor. Therefore, as shown in Fig. 10(b), the resistor has a symmetric characteristic around the quiescent point and hence it is more linear compared with the resistor shown in Fig. 8(b). By using this structure, the THD of the system is improved from $-33.78$ dB to $-43.61$ dB at the low-cutoff frequency of 300 Hz and from $-44.05$ dB to $-46.41$ dB at around 10 kHz. Also, since no dc current flows through the transistors $\mathrm{M_A}$ and $\mathrm{M_B}$, their transconductances are very small and the resistor has much lower added noise. The pseudo cross-coupled structure is,

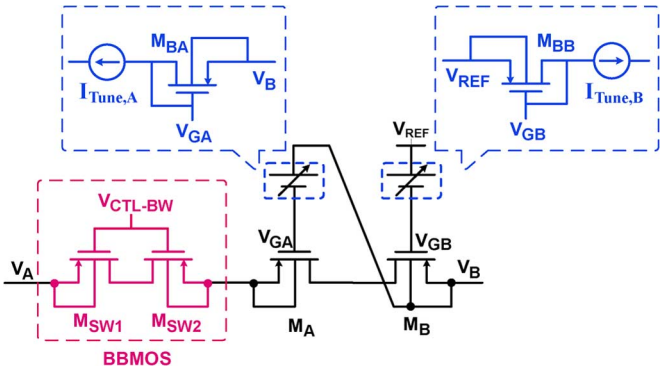


Fig. 11. Proposed pseudo-resistor structure.

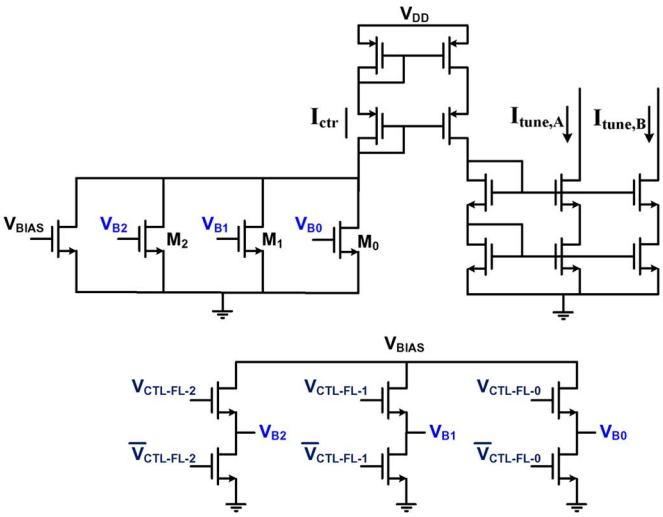


Fig. 12. DAC structure used for fine tuning of the low-cutoff frequency.

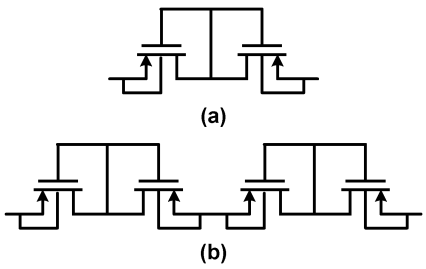


Fig. 13. (a) Nontunable pseudo-resistor. (b) Multiple resistors in series.

however, somewhat sensitive to the OTA offset, which can be overcome by designing a low-offset and high-gain OTA. Note that all of the simulated values mentioned above have been obtained by simulating a structure similar to what proposed in sub-Section II-A as the test bench in 0.18 $\mu$m CMOS technology.

In order to decrease the low-cutoff frequency of the amplifier by increasing the resistance value, the $V_{SG}$ for transistors $M_A$ and $M_B$ should be decreased. Using the current-controlled structures, the $V_{SG}$ value of the transistors can be decreased down to zero in an extreme case. Even for a zero gate-source voltage, due to the large leakage current of the transistors in 0.18 $\mu$m technology, the resistance of the device is not higher

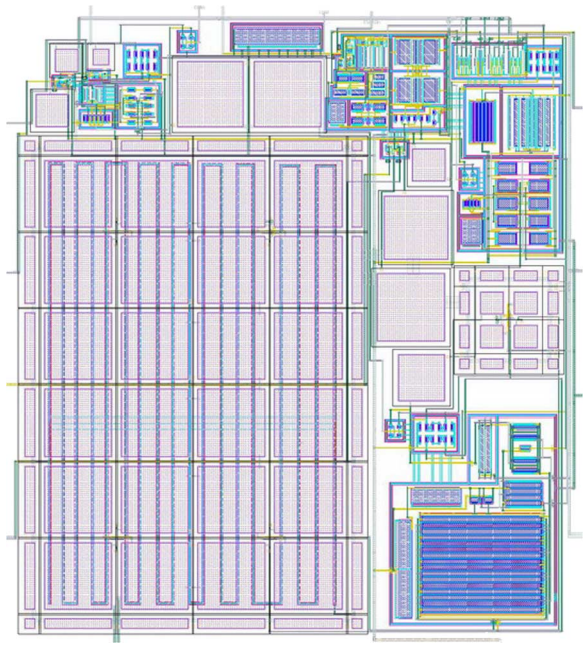

Fig. 14. Layout of the front-end amplifier with the size of 260 $\mu$m $\times$ 235 $\mu$m.

TABLE I
GAIN TUNABILITY AT TYPICAL CASE (TT), 37 °C

| Mode | | Gain | $f_L$ (Hz) | $f_H$ (kHz) |
|---|---|---|---|---|
| 00 | switch on | 748.2 | 301.9 | 9.82 |
| | switch off | 761.1 | 4.89 | 9.39 |
| 01 | switch on | 495.6 | 302.2 | 9.92 |
| | switch off | 509.4 | 4.14 | 9.44 |
| 10 | switch on | 594.8 | 302.2 | 9.88 |
| | switch off | 607.7 | 4.76 | 9.45 |
| 11 | switch on | 424.4 | 302.1 | 9.95 |
| | switch off | 433.4 | 4.62 | 9.51 |

than hundreds of giga-Ohms. As a result, the low-cutoff frequency cannot be reduced to below several Hertz. Therefore, in order to achieve such small low-cutoff frequencies and at the same time have a suitable linearity over the entire frequency band, a new structure is proposed and employed as follows.

The structure shown in Fig. 11 is proposed to implement a linear pseudo-resistor with a wide range of tunability to be used in the second stage of the amplifier. In this structure, a pseudo cross-coupled resistor is used in series with a voltage-controlled MOSFET structure. This MOSFET structure, comprising two back-to-back MOSFETs (BBMOS), is used as a switch for the coarse tuning of the low-cutoff frequency. By setting the control bit, $V_{CTL-BW}$, to logic "0", the BBMOS switch will be on, exhibiting small on-resistance in series with the large resistance of $M_A$ and $M_B$. This negligible small on-resistance does not affect the resistance linearity behavior because the overall voltage swing on this resistance is a very small portion of the total voltage swing of the stage. In this state, the low-cutoff frequency is adjusted to be around 300 Hz.

By turning off the BBMOS switch (setting the $V_{CTL-BW}$ control bit to logic "1"), the large off-resistance of BBMOS will

TABLE II
LOW-CUTOFF FREQUENCY TUNABILITY AT DIFFERENT PROCESS CORNERS, 37 °C

| Corner | Mode | | $f_L$ (Hz) |
|---|---|---|---|
| FF | 00 | switch on | 300.3 |
| | switch off | | 10 |
| FS | 01 | switch on | 301.7 |
| | switch off | | 3.82 |
| TT & SF | 10 | switch on | 299.4 – 303.2 |
| | switch off | | 4.15 - 7.63 |
| SS | 11 | switch on | 299.2 |
| | switch off | | 2.6 |

TABLE III
HIGH-CUTOFF FREQUENCY TUNABILITY AT DIFFERENT PROCESS CORNERS, 37 °C

| Corner | Mode | | $f_H$ (kHz) |
|---|---|---|---|
| SS & SF | 00 | switch on | 10 - 11.3 |
| | | switch off | 9.57 - 10.8 |
| TT | 01 | switch on | 9.95 |
| | | switch off | 9.47 |
| FF & FS | 11 | switch on | 10.1 - 8.84 |
| | | switch off | 9.65 - 8.45 |

appear in series with the resistances of $M_A$ and $M_B$, making it possible to adjust the low-cutoff frequency as small as below a few Hertz (around 4 Hz in this work). By tying $V_{CTL-BW}$ to the supply voltage, which means a large negative source-gate voltage of $-0.9$ V ($V_{DD} = 1.8$ V and $V_{REF} = 0.9$ V) for $M_{SW1}$ and $M_{SW2}$, BBMOS acts as a series combination of two back-to-back diodes with a symmetric characteristic. Therefore, the proposed resistor will show a superior linearity behavior over a wide range of resistance values.

Fine tuning of the low-cutoff frequency is realized by using a simple two-bit current DAC, controlling the resistance of the pseudo cross-coupled resistor. The DAC structure is shown in Fig. 12, in which the lower circuit generates the gate voltages required for the reference current generator in the upper circuit. The signals $V_{CTL-FL-(0-2)}$ are three control voltages prepared by a decoder circuit receiving the two control bits at the input. Mirroring the control current ($I_{ctr}$) before applying to the bias transistors ($M_{BA}$ and $M_{BB}$) may lead to a lower sensitivity of this current to the leakage currents of the turned-off switches ($M_0 - M_2$). Also, by using this structure, both of the control currents ($I_{tune,A}$ and $I_{tune,B}$) can be provided by using one DAC and the output resistance of the current sources will be improved.

### *B. Fixed Pseudo Resistors*

The amplifier also needs fixed pseudo-resistors for implementing the first and the last stages. The value of these resistors determines the low-cutoff frequency of the above stages.

It should be noted that the impedance of the feedback resistor will be very smaller than the impedance of the feedback capacitor after a specific frequency (that is much larger than the low-cutoff frequency e.g., $10.f_L$). Therefore, in wide-band neural amplifiers (such as this work) the effect of the nonlinear feedback resistor can be neglected for most frequencies of the band. When the low-cutoff frequency of the entire system is set at 300 Hz, the low-cutoff frequency of the first and the third stages are designed to be much lower than the second stage. This means that the resistors of the first and third stages are set to be much larger than the resistor of the second stage and so the fixed resistors linearity does not have a sensible effect on

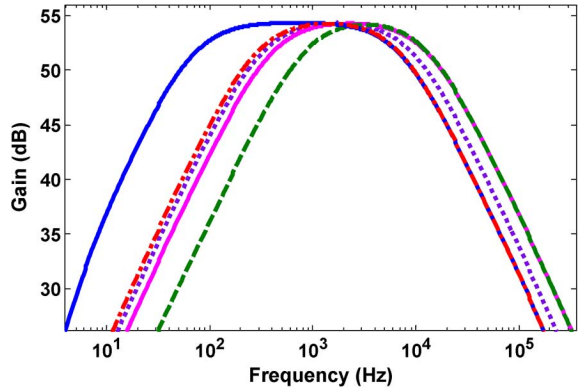


Fig. 15. Bandwidth control in typical case (TT) and large low-cutoff frequency for different settings.

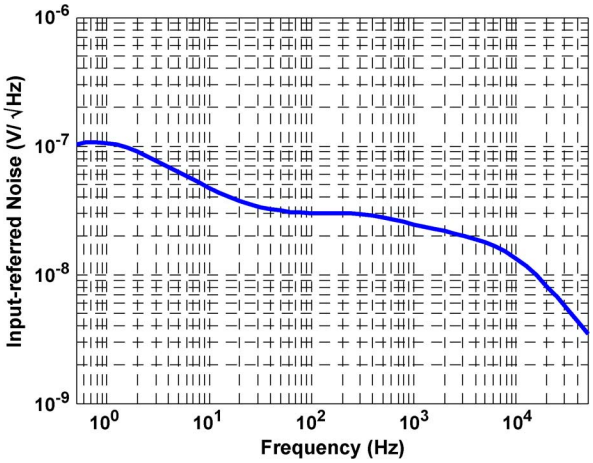


Fig. 16. Input-referred noise of the amplifier for typical case (TT), $f_L = 300$ Hz, $f_H = 10$ kHz, and Gain $= 54$ dB.

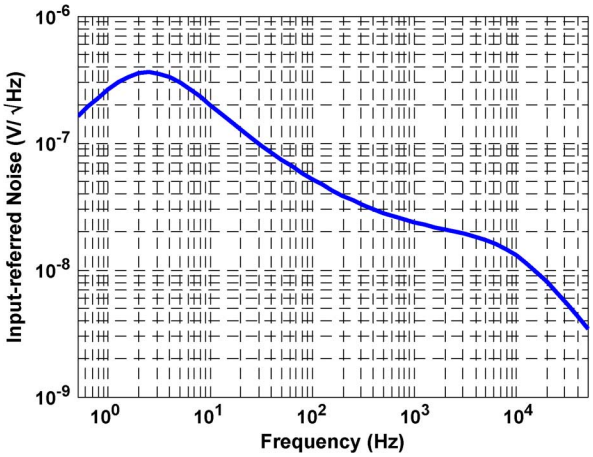


Fig. 17. Input-referred noise of the amplifier for typical case (TT), $f_L = 4$ Hz, $f_H = 10$ kHz, and Gain $= 54$ dB.

TABLE IV
PERFORMANCE COMPARISON WITH OTHER DESIGNS

| Parameter | | [7] | [8] | | | [11] | [18] | [19] | [20] | [21] | This work | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Technology | | 1.5 μm | 1.5 μm | | | 0.35 μm | 0.18 μm | 0.13 μm | 0.18 μm | 0.5 μm | 0.18 μm | | |
| Supply voltage | | ±2.5 V | ±1.7 V | | | 1.5 V | 1.8 V | 0.8 V | 1.6 V | 3 V | 1.8 V | | |
| Output Swing | | N/A | 1.8 Vpp | | | N/A | N/A | N/A | N/A | N/A | 1 Vpp | | |
| Amplifier Gain (dB) | | 39.5 | 39.3, 45.6 (Tunable) | | | 51.9 – 65.6 (Tunable) | 39.4 | 49 | 19.1 / 37.5 (Tunable) | 67.8 / 78 (Tunable) | 52.5 – 57.5 (Tunable) | | |
| Amplifier Bandwidth (Hz) | | 0.025 – 7.2k | 0.015 – 4k (Tunable) | | | 1.1– 12k (Tunable) | 10 – 7.2k (Tunable) | 100 – 6.2k (Tunable) | 100 – 8k (Tunable) | 0.1– 8 k (Tunable) | 4 / 300 – 10 k (Tunable) | | |
| Power consumption | | 80 μW | 27.2 μW | | | 26.9 μW | 7.92 μW | 0.64 μW | 69 μW | 75 μW | 20.8 μW | | |
| Input-referred Noise | | 2.2μVrms (0.5Hz-50kHz) | 3.6μVrms (20Hz-10kHz) | | | 3.12μVrms (0.5Hz-50kHz) | 3.5μVrms (10Hz-100kHz) | 14μVrms | 2.36μVrms | 4.08μVrms (1Hz – 10kHz) | 2.6 / 2.38 μVrms (0.5Hz-50kHz) | | |
| Noise efficiency factor | | 4 | 4.9 | | | 4.64 | 3.35 | 6.5 | 6.59 | 8.45 | 3.38 / 3.07 | | |
| Linearity | Frequency (Hz) | N/A | 10 | 100 | 1k | N/A | 1k | N/A | N/A | N/A | 4 | 300 | 10k |
| | Swing (Vpp) | 16.7m (input) | 23m (input) | 19m (input) | 17.4m (input) | N/A | 5.7m (input) | 1 m (input) | N/A | N/A | 1 (output) | 1 (output) | 1 (output) |
| | THD (dB) | -40 | -40 | -40 | -40 | N/A | -40 | < - 47.96 | N/A | N/A | -37.45 | -46.24 | -45.97 |
| CMRR | | ≥ 83 dB | N/A | | | ≥ 56 dB | 70.1 dB | 59 dB | 79 dB | 134 dB | 88 dB | | |
| PSRR | | ≥ 85 dB | N/A | | | ≥ 65 dB | 63.8 dB | 71 dB | 62 dB | 62.7 dB | 85 dB | | |
| Total Capacitor | | 40.4 pF * | 40.8 pF | | | 94.1 pF | 25.25 pF * | N/A | 12.6 pF | N/A | 24.1 pF | | |
| Sim. / Meas. | | Meas. | Meas. | | | Meas. | Meas. | Meas. | Meas. | Meas. | Post-layout Simulation | | |

*Large load capacitor that sets the high cutoff frequency is not included.

the in-band signal. But when the low-cutoff frequency is adjusted at around 4 Hz, the low-cutoff frequency of the first and third stages also contribute in determining the overall system low-cutoff frequency. So, the linearity of the resistors used in the first and especially in the third stage, also affects the total system linearity. In both the first and the third stages of the amplifier, nontunable high-valued pseudo-resistors are used. One of the best structures for implementing these resistors is a series combination of nontunable pseudo-resistors shown in Fig. 13(a). This structure is easy to implement, has a low added parasitic capacitance, and adds very low noise to the amplifier. Equivalent resistance of this structure shows symmetric variations around the quiescent point in all the process corners leading to the desired linearity. Linearity of the equivalent resistor can be further improved by connecting multiple resistors in series [as in Fig. 13(b)]. This is simply because of the reduced voltage variations across each resistor leading to the improvement of the linearity of each one of the resistors in series. A double resistor series structure is used for implementing the two resistors used in the first stage, and a triple resistor structure is used for the third stage.

## IV. SIMULATION RESULTS

The tunable amplifier presented in this paper was designed and simulated in TSMC 0.18 $\mu$m CMOS process in typical process conditions as well as in all the four process corners. Note that the temperature of the implantable SI circuit is almost constant [2]. The layout view of the proposed three-stage amplifier chip is shown in Fig. 14 and the post-layout simulation results are presented as follow. Table I shows the gain tunability using two bits in the range of 52.5–57.5 dB for large and small low-cutoff frequency modes (where BBMOS is on and off, respectively). Also, the results present a very small variation of the low- and high-cutoff frequencies with different voltage gains. The simple DAC used for the second stage pseudo-resistor is tuned in the process corners to have a nearly constant low-cutoff frequency in 300 Hz frequency mode demonstrated in Table II. The tuning of the low-cutoff frequency is optimized for 300 Hz in all the process corners due to the large variation of the low-cutoff frequency for this case. The high-cutoff frequency is kept almost constant using switchable capacitors. The values for high-cutoff frequency in all the process corners

are shown in Table III for both small and large low-cutoff frequency modes. Fig. 15 illustrates different bandwidths for the amplifier that can be achieved for different low- and high-cutoff frequency in the typical case (TT).

Spectral density of the input-referred noise of the entire amplifier is shown in Figs. 16 and 17 for large and small low-cutoff frequency modes, respectively. According to the simulations, total input-referred noise voltage of the amplifier is 2.38 $\mu\mathrm{V_{rms}}$ over 0.5 Hz–50 kHz frequency range for the case where $\mathrm{f_L} = 300$ Hz. This value is 2.6 $\mu\mathrm{V_{rms}}$ for the case where $\mathrm{f_L} = 4$ Hz. If the noise integration interval is changed to the frequency band (i.e., $\mathrm{f_L}$ to $\mathrm{f_H}$) these two values are changed to 1.84 $\mu\mathrm{V_{rms}}$ and 2.13 $\mu\mathrm{V_{rms}}$, respectively. Simulation results indicate a THD of $-37.45$ dB at 4 Hz (where $\mathrm{f_L} = 4$ Hz) and $-46.24$ dB at 300 Hz (where $\mathrm{f_L} = 300$ Hz) and $-45.97$ dB at 10 kHz while the amplifier provides an output swing of 1 $\mathrm{V_{p-p}}$. Also, distortion stays below 1% THD for inputs less than 3.9 $\mathrm{mV_{PP}}$ at the input frequency of 300 Hz.

Monte-Carlo simulations were also performed to verify the sensitivity of the circuit to the device mismatches. The variations in the mid-band gain as well as in low- and high-cutoff frequencies were adequately small.

Simulated specifications for the entire system are compared to other works in Table IV. The proposed system architecture exhibits very low input-referred noise voltage. Noise efficiency factor (NEF), a figure of merit to compare the noise, supply current, and bandwidth of neural amplifiers, is obtained from [17]

$$\mathrm{NEF} = V_{ni,\mathrm{rms}}\sqrt{\frac{2I_{\mathrm{tot}}}{\pi \cdot U_t \cdot 4kT \cdot BW}} \tag{7}$$

where $I_{\mathrm{tot}}$ is the total amplifier supply current, $U_t$ is the thermal voltage $kT/q$, and $BW$ is the amplifier bandwidth. This work achieves an NEF of 3.07 for the case where $\mathrm{f_L} = 300$ Hz and the input-referred noise power is integrated over 0.5 Hz–50 kHz frequency range. This value is 3.38 for the case where $\mathrm{f_L} = 4$ Hz and the input-referred noise power is integrated over the same frequency range. If the noise integration interval is changed to the frequency band (i.e., $\mathrm{f_L}$ to $\mathrm{f_H}$) these two values are changed to 2.37 and 2.78, respectively. Such values for the NEF are reasonable for a three-stage amplifier with a fast-settling ADC driver and a large load of 20 pF. The linearity performance as well as the CMRR and PSRR of this work are comparable to other reports in the entire frequency band. Also, using three-stage architecture has led to a small total capacitor and thus small chip area. The total capacitance in this work is 62% of the total capacitance in [7] and [8] and 27% of the total capacitance in [11].

## V. Conclusion

Challenges in the design of low-noise tunable amplifiers employed in neural-recording sensor interface circuits were discussed and an in-depth analysis was presented. Furthermore, a three-stage amplifier comprising an LNA, a band-pass filter, and a VGA was demonstrated to minimize the area, reduce the total input-referred noise while preserving the linearity behavior of the circuit and driving a large input capacitance of the following ADC. The amplifier has a dual-mode selection (small/large low-cutoff frequency) and a linear behavior in these two modes, benefiting from the linear behavior of a novel tunable pseudo-resistor proposed in this work. The mid-band gain and high cutoff frequency of the amplifier are tunable as well.

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