

An Analytical Gate Tunneling Current Model for MOSFETs¹

Iman Abaspur Kazerouni[^] and Seyed Ebrahim Hosseini

Electrical and Computer Department, Sabzevar Tarbiat Moallem University, Tohidshahr, Sabzevar, Iran

[^]e-mail: imanabaspur@gmail.com

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Abstract—Gate tunneling current of MOSFETs is an important factor in modeling ultra small devices. In this paper, gate tunneling in present-generation MOSFETs is studied. In the proposed model, we calculate the electron wave function at the semiconductor–oxide interface and inversion charge by treating the inversion layer as a potential well, including some simplifying assumptions. Then we compute the gate tunneling current using the calculated wave function. The proposed model results have an excellent agreement with experimental results in the literature.

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1. INTRODUCTION

Progress in MOS/VLSI technology is accomplished by a constant trend to decrease the gate oxide thickness. This serves two main purposes:

- (1) to increase the transistor transconductance, which in turn improves the circuit speed, and
- (2) to avoid short-channel effects [1].

Doping concentration must be increased in short channel MOSFETs in order to reduce depletion region width. Thus in these MOSFETs the substrate doping concentration is increased proportional to oxide thickness decrease. These two effects result in a very high electric field at the oxide–semiconductor interface, which causes severe band bending in the semiconductor near the interface, creating a potential well structure. The carrier energy is quantized in this potential well [2]. Some of the carriers can pass the oxide and arrive at gate electrode. Hence, gate tunneling phenomenon occurs and the resulting gate current affects MOSFET performance.

In [3, 4], a simple analytical equation has been obtained for calculation of the gate tunneling current by assumption of a trapezoid potential well. Lee and Hu [5] came up with a semiempirical model. They do not take into account the energy levels due to confined carriers in potential well. In Lin and Kuo [6] and Liu et al. [7] models, these energy levels have been also neglected.

In 2008, Mondal et al. [8] presented a model in which confined carriers and their effects have been considered. They achieved an equation for electron wave function, which is dependent on the width of the potential well. One of the effects of carrier confinement and subsequent energy quantization is that the

shape of the carrier distribution in the semiconductor is changed.

In this paper, we present a novel model for gate tunneling current density based on the idea of [8]. In the proposed model, electron wave function at interface is calculated using basic equations and some simplifications regarding the potential well structure. Then an equation is proposed for gate tunneling current which predicts the gate current for various doping levels, gate bias and oxide thicknesses. This paper is originated as follows. Section 2 presents a compact expression for the electron wave function, inversion charge and available carriers for tunneling. In Section 3 the gate tunneling current density is derived. Sections 4 and 5 present simulation results of the proposed model and summary, respectively.

2. PROPOSED MODEL

2.1. Simplifying Assumptions

In this paper, a silicon *n*-channel MOSFET (NMOS) has been investigated. Figure 1 shows a cross-sectional view of an NMOS structure under strong inversion. The band bending in the semiconductor near the interface has a soft slope (Fig. 2a). In different researches, the band profile within an inver-

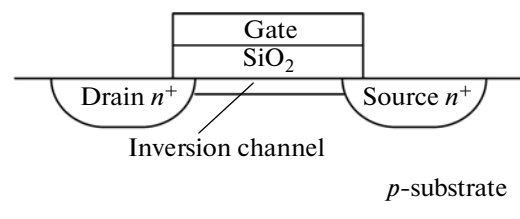


Fig. 1. Cross-sectional view of an *n*-channel MOSFET.

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sion layer has been considered with different shapes such as trapezoid [9], parabola [10] and rectangular [8].

In this investigation we assume a rectangular potential well approach. This simplifies mathematical calculations considerably. Since ultimate gate tunneling current is important, the well parameters must be adjusted. For further simplification, the well is considered symmetric with a depth ΔE_c and a width $2L$ [8]. Because ΔE_c and $q\phi_s$ (ϕ_s is the surface potential) are much larger than the ground-state energy level E_1 (measured with respect to the conduction band energy at the interface denoted by $E_c(0)$), this assumption is agreeable. Most of inversion layer electrons, which play the main role in current transport, are in the first quantized energy level. Figure 2b shows the final potential well upon using simplifications.

2.2. Electron Wave Function

In the popular triangular-well approximation the energy E_1 of the ground state equals [8]:

$$E_1 = 0.75 \left(\frac{\hbar^2}{2m_e} \right)^{1/3} \left\{ \left[\frac{9\pi}{8\epsilon_s} qQ_r \right] \left[1 + \ln \left(\frac{qN}{Q_r} \right) \right] \right\}^{2/3}, \quad (1)$$

where m_e , \hbar and ϵ_s are effective mass of the electrons in the semiconductor, reduced Planck's constant and relative permittivity of the semiconductor, respectively. For the assumed rectangular well approach the width $2L$ is adjusted warranting $E_{1, \text{rectangular}} = E_{1, \text{triangle}}$. The effective masses of the electrons in the oxide and in the semiconductor channel have been taken as $m_e = 0.5m_0$ and $m_{\text{ox}} = 0.98m_0$, respectively, where m_0 is the rest mass of an electron. The term N is inversion layer charge and expressed as

$$N = [\epsilon_{\text{on}}(V_{\text{GB}} - \phi_{\text{ms}} - \phi_s)/(qt_{\text{ox}})] - N_{\text{dep}},$$

where ϵ_{ox} and t_{ox} are the relative permittivity and thickness, respectively, of the oxide, ϕ_{ms} is the metal–semiconductor work function difference, and N_{dep} is the concentration of the depletion ions per unit area. Q_r is a reference surface charge density, which is given by:

$$Q_r = \sqrt{2q\epsilon_s N_A} [\phi_s + \phi_t \exp(6)]^{1/2}. \quad (2)$$

It is assumed that once the system reaches strong inversion, the surface potential ϕ_s gets essentially pinned at $(2\phi_F + 6\phi_t)$ [11], where ϕ_F is the bulk potential, given by $\phi_F = \phi_t \ln(N_A/n_i)$, with t being the thermal voltage, N_A is the substrate doping concentration, and n_i is the semiconductor intrinsic carrier concentration.

The time-independent Schrödinger equation in one dimension is:

$$\left(-\frac{\hbar^2 d^2}{2m(x)dx^2} + E_c(x) \right) \psi(x) = E_1 \psi(x), \quad (3)$$

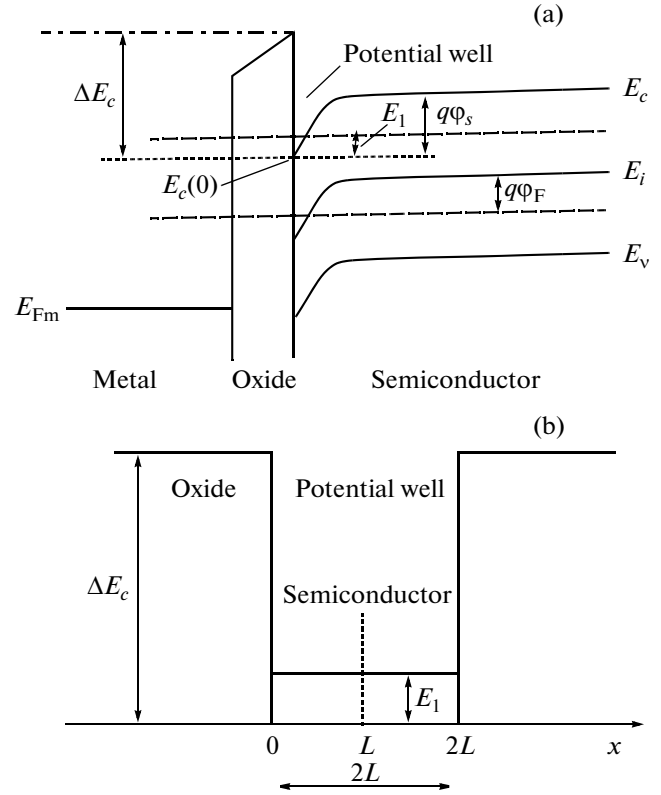


Fig. 2. (a) band diagram of the NMOS structure and (b) the obtained symmetric rectangular potential well after simplifications.

where $\psi(x)$ is the electron wave function. A solution of Eq. (3) for the ground state in the proposed potential well (Fig. 2b) will be:

$$\psi(x) = \begin{cases} \alpha \cos[K(x-L)], & 0 < x < 2L \\ \alpha \cos(KL) \exp(-k|x-L|) \exp kL, & x < 0, \quad x > 2L \end{cases} \quad (4)$$

where K and k are the wave numbers:

$$K = \sqrt{\frac{2m_e E_1}{\hbar^2}} \quad \text{and} \quad k = \sqrt{\frac{2m_e (\Delta E_c - E_1)}{\hbar^2}}.$$

In order to keep the well symmetrical the unique mass value $m(x) = m_e$ was used in Eq. (3). The interrelation between L , K and k is:

$$2L = \frac{2}{K} \arctan \left(\frac{k}{K} \right). \quad (5)$$

In Eq. (4), the coefficient α determines the magnitude of the wave function. The gate tunneling current increases with an increase in the wave function at an oxide–semiconductor interface. For the infinite ΔE_c ,

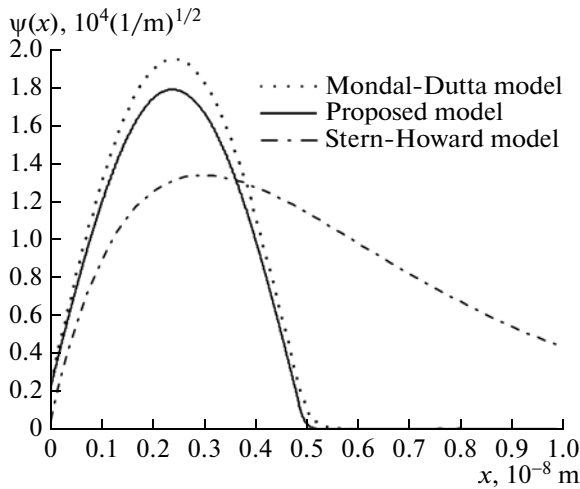


Fig. 3. The electron wave function for a NMOS with $N_A = 4 \times 10^{14} \text{ cm}^{-3}$, $t_{\text{ox}} = 2.3 \text{ nm}$ and $V_{\text{GB}} = 0.62 \text{ V}$ obtained from the proposed model (solid), the Stern–Howard [15] model (dash-dotted line) and the Mondal–Dutta model [8] (dotted).

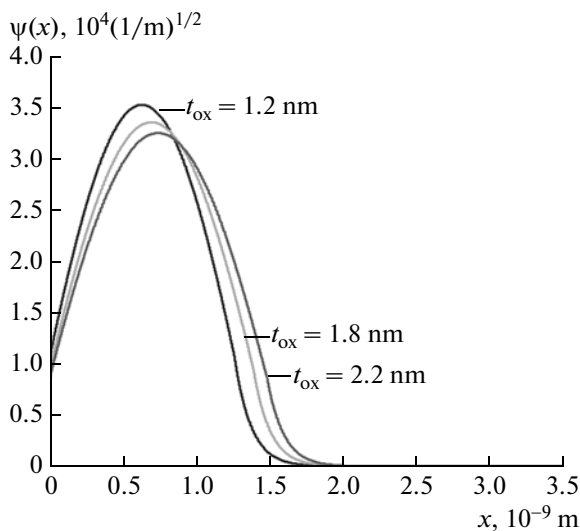


Fig. 4. Electron wave functions based on proposed model for devices with $N_A = 10^{17} \text{ cm}^{-3}$, $V_{\text{GB}} = 0.93 \text{ V}$.

the value of α would equal $L^{-1/2}$. For the finite barrier the corrections should be made as:

$$\alpha = \eta L^{-1/2}, \tag{6}$$

where $\eta < 1$. The factor η depends on the well width $2L$, but our simulation experience shows that one can approximately put $\eta = 0.88$ for all practical cases.

3. GATE TUNNELING CURRENT

Under the inversion condition, electron leakage from the inversion layer into the metal dominates the gate current.

In this section, the gate tunneling current density is obtained using the tunneling probability according to the calculated wave function in previous section. The height of the potential barrier and the amount of carriers in the device are important parameters in the tunneling probability. Based on WKB approximation tunneling probability (P_T) is expressed as:

$$P_T = \exp\left(-2 \int_{-t_{\text{ox}}}^0 k_{\text{ox}}(x) dx\right), \tag{7}$$

where k_{ox} is the wave number of electrons in the oxide [12] and can be expressed as:

$$k_{\text{ox}}(x) = \sqrt{\frac{2m_{\text{ox}}}{\hbar^2}(\Delta E_c - E_1 + qF_{\text{ox}}x)}, \tag{8}$$

where F_{ox} is the constant electric field across the oxide. The expression for $k_{\text{ox}}(x)$, as given by Eq. (8), is substituted in the expression for P_T . After simplifications, the tunneling probability can be obtained as:

$$P_T = \exp\left(\frac{4}{3} \sqrt{\frac{2qF_{\text{ox}}m_{\text{ox}}}{\hbar^2}} \times \left\{ \left(-t_{\text{ox}} + \frac{\Delta E_c - E_1}{qF_{\text{ox}}}\right)^{3/2} - \left(\frac{\Delta E_c - E_1}{qF_{\text{ox}}}\right)^{3/2} \right\}\right). \tag{9}$$

The general expression for the total charge density Q within the semiconductor is given by the equation:

$$Q = \frac{\epsilon_{\text{ox}}(V_{\text{GB}} - \Phi_{\text{ox}} - \Phi_s)}{t_{\text{ox}}}. \tag{10}$$

Now based on [8], the gate tunneling current density can be given by:

$$J = \left| \left(Q - \sqrt{2q\epsilon_s N_A \Phi_s}\right) |\psi(0)|^2 \frac{V_f P_T}{V_{\text{GB}} \sqrt{m_m}} \right|, \tag{11}$$

where $V_f (= 1 \text{ V})$ is a fitting parameter and m_m is the effective mass of electrons in the metal, $(2E_1/m_m)^{1/2}$ is defined as electron velocity at the oxide-metal interface. The gate tunneling current density has been achieved using the electron wave function at $x = 0$. It is to be noted that this value depends on the gate voltage and the oxide width. Comparison of the simulation results of the gate tunneling current density with experimental results [13, 14] shows an acceptable match between them.

4. SIMULATION RESULTS

Figure 3 shows electron wave function for a NMOS structure with $N_A = 4 \times 10^{14} \text{ cm}^{-3}$, $t_{\text{ox}} = 2.3 \text{ nm}$ and $V_{\text{GB}} = 0.62 \text{ V}$. The results of Stern–Howard model

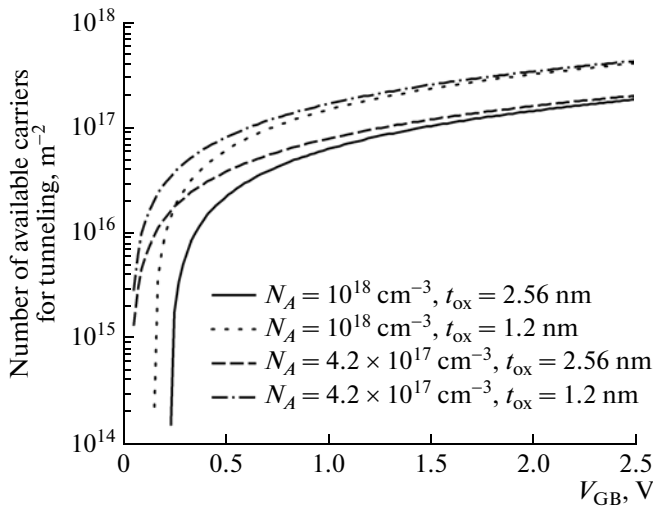


Fig. 5. The number of electrons for various substrate doping concentrations and oxide widths.

[15] and Mondal–Dutta model [8] are also shown in Fig. 3 for comparison. Typical value of the conduction band discontinuity ΔE at the interface to 3.2 eV (for Si–SiO₂ systems), whereas near the onset of strong inversion, the surface potential ϕ_s typically ranges around 1 V or so.

In Stern–Howard model, wave function penetration into the oxide barrier is not considered. In that model the value of wave function at oxide–semiconductor is zero but in the proposed model and Mondal–Dutta model, the wave function profile shows a nonzero value at the oxide–semiconductor interface, corresponding to the rectangular well structures.

Figure 4 shows the wave function profiles for three NMOSs with $N_A = 1 \times 10^{17} \text{ cm}^{-3}$, $V_{GB} = 0.93 \text{ V}$, $t_{ox} = 1.2 \text{ nm}$, $t_{ox} = 1.8 \text{ nm}$ and $t_{ox} = 2.2 \text{ nm}$. The magnitude of the wave function at the peak and across the interface decrease with an increase in the oxide thickness, which is expected.

The number of electrons available for tunneling from the semiconductor into the metal gate (N) is shown as a function of the gate-to-body voltage in Fig. 5. The carrier concentration in the inversion layer has been calculated in presence of quantum effects and in strong inversion state. Figure 5 shows the number of electrons for various substrate doping and oxide widths. The concentration of the depletion ions per unit area (N_{dep}) decreases as the substrate doping concentration (N_A) decreases and this causes the number of electrons available for tunneling (N) to increase.

The results of the proposed model and experimental data for a NMOS structure with $N_A = 8.5 \times 10^{17} \text{ cm}^{-3}$ and $t_{ox} = 1.83 \text{ nm}$, are shown in Fig. 6. Also included is the comparison of the experimental results borrowed from [13, 14] with the proposed model for

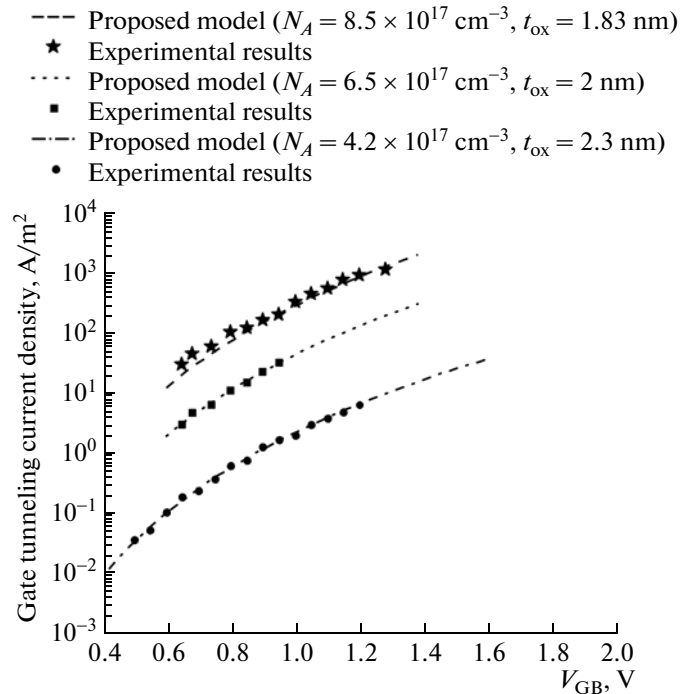


Fig. 6. Results of proposed model and experimental for three MOSFETs.

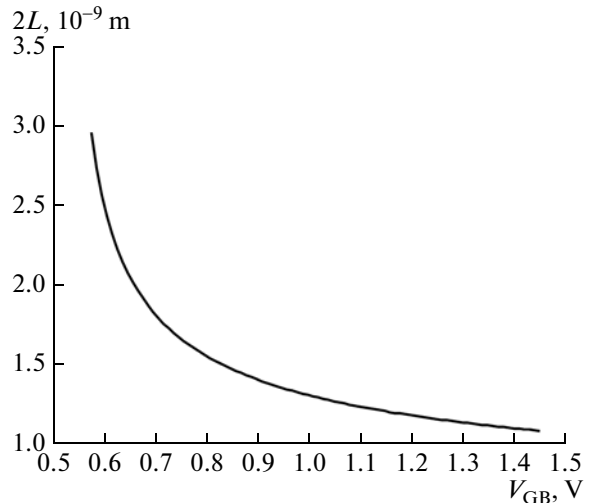


Fig. 7. Inversion layer thickness $2L$ as a function of the applied gate-to-body voltage V_{GB} for a device having $N_A = 8.5 \times 10^{17} \text{ cm}^{-3}$ and $t_{ox} = 2.3 \text{ nm}$.

$t_{ox} = 2.3 \text{ nm}$ and $N_A = 4.2 \times 10^{17} \text{ cm}^{-3}$ and for $t_{ox} = 2 \text{ nm}$ and $N_A = 6.5 \times 10^{17} \text{ cm}^{-3}$.

The variations of N_A within a relatively narrow range in Fig. 6 are practically unimportant, so that a large difference between the currents for three samples is due to different insulator thicknesses. A theory-to-experiment agreement is seen to be quite satisfactory.

Figure 7 shows the inversion layer thickness $2L$ as a function of the applied gate-to-body voltage V_{GB} for a device having $N_A = 8.5 \times 10^{17} \text{ cm}^{-3}$ and $t_{ox} = 2.3 \text{ nm}$. A large number of simulations performed for varying substrate doping and oxide thickness evidences that $2L$ decreased with an increase in the substrate doping as well as with the gate voltage.

5. CONCLUSIONS

In this paper, we have presented a novel model for obtaining the electron wave function at the oxide–semiconductor interface and the gate tunneling current density based on the tunneling probability. In this model, a symmetric rectangular potential well has been considered using some simplifications.

Comparison of the simulation results of the gate tunneling current density with experimental results shows an acceptable match between them. For example with $t_{ox} = 2.3 \text{ nm}$ the magnitude of the mean error is less than 1% which is perfectly acceptable. It must be noted that this error may vary for different gate-bulk voltages (V_{GB}) and the oxide thicknesses.

Beyond a numerical convenience the rectangular well model is profitable for analyzing the charge distribution trends expected with a variation of the structure parameters and bias condition.

REFERENCES

1. B. Majkusiak, IEEE Trans. Electron Dev. **37**, K1087 (1990).
2. S. M. Sze and K. Ng Kwok, *Physics of Semiconductor Devices* (Wiley, New York, 2007).
3. K. F. Schuegraf, C. C. King, and C. Hu, Dig. Symp. VLSI, K18 (1992).
4. K. F. Schuegraf and C. Hu, IEEE Trans. Electron Dev. **41**, K761 (1994).
5. W. C. Lee and C. Hu, IEEE Trans. Electron Dev. **48**, K1366 (2001).
6. C. H. Lin and J. B. Kuo, Solid State Electron. **53**, K1191 (2009).
7. Xiaoyan Liu, Jinfeng Kang, and Ruqi Han, Solid State Commun. **125**, K219 (2003).
8. Imon Mondal, K. Aloke, and K. Dutta, IEEE Trans. Electron. Dev. **55**, K1682 (2008).
9. M. Depas, B. Vermeire, P. W. Mertens, R. L. van Meirhaeghe, and M. M. Heyns, Solid State Electron. **38**, K1465 (1995).
10. Jin He, M. Chan, X. Zhang, and Y. Wang, IEEE Trans. Electron. Dev. **53**, K2082 (2006).
11. Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. (McGraw-Hill, New York, 1999).
12. A. Ghatak and S. Lokanathan, *Quantum Mechanics: Theory and Application* 5th ed. (McMillan, New Delhi, India, 2004).
13. R. Clerc, P. O'Sullivan, K. G. McCarthy, G. Ghibaudo, G. Pananakakis, and A. Mathewson, Solid State Electron. **45**, K1705 (2001).
14. R. Clerc, G. Ghibaudo, and G. Pananakakis, Solid State Electron. **46**, K1039 (2002).
15. F. Stern, Phys. Rev. B: Condens. Matter **5**, K4891 (1972).