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A novel SiC MESFET with recessed P-Buffer layer

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Abstract. *We report, for the first time, a silicon carbide (SiC) based metal semiconductor field effect transistor (MESFET) which has a recessed p-buffer layer into the channel region near the source and a recessed channel into the p-buffer layer region near the drain under the gate. The length and thickness of the channel recess into the p-buffer layer are larger than the p-buffer recess into the channel. We call this new structure as Recessed P-Buffer (RPB) SiC MESFET. The proposed structure has the narrower channel near the source and thicker channel near the drain in comparison with the Conventional-Recessed Gate (CRG) SiC MESFET. The narrow channel at the source side of the proposed structure, improves maximum DC-transconductance, gate-source capacitance, cut off frequency, and maximum DC output conductance compared to the CRG structure. Also, due to the thick channel at the drain side, the channel saturation drain current is higher than that in the CRG structure.*

INTRODUCTION

SiC material semiconductor field effect transistors (MESFETs) have recieved increased attention in the recent years due to their high operating voltage, high power density and high frequency performance. These enable wider band width operation, and lower the size and weight of systems compared to those using conventional technologies based on Si and GaAs. Even though the electron mobility in SiC is much lower than that in GaAs, good microwave performance can be obtained with submicron gate devices, which ope-rate at high electric fields driving the electrons into their saturation velocity that is nearly twice that in GaAs. However, short-channel length coupled with larger drain voltage applied to the MESFETs will result in short-channel effects, in particular the drain-induced barrier lowering (DIBL) effect, which will degrade the device performance in a form of threshold voltage shift and high output conductance.

The SiC MESFETs technology is a candidate for high power microwave applications. Its wide bandgap and high thermal conductivity offer several advantages compared to Si- and GaAs - based technologies. SiC MESFETs are very well-suited for high voltage, high power and high temperature applications due to its superior material properties especially high critical electrical field, high electron saturation velocity, and high thermal conductivity [1-6].

In order to improve the DC and RF characteristics of the conventional recessed gate SiC MESFET, in this paper we propose a new structure which has a recessed p-buffer layer into the channel region near the source and a recessed channel region into the p-buffer layer near the drain under the gate. The length and thickness of the channel recess into the p-buffer layer are larger than the p-buffer recess into

the channel. We investigate the changes that occur in the DC and RF characteristics of proposed structure in comparison with the conventional recessed gate structure.

1. DEVICE STRUCTURE

Fig. 1(a) and (b) show the schematic cross-section of the RPB and CRG[7],[8] structures. Two structures have the same sizes. But the RPB structure has two p-buffer and channel recessed region under the gate with different lengths and thicknesses. According to this figure, the length and thickness of the recessed p-buffer to the channel region are 0.3µm and 0.05µm respectively while the length and thickness of the recessed channel to the p-buffer layer region are 0.4µm and 0.15µm respectively.

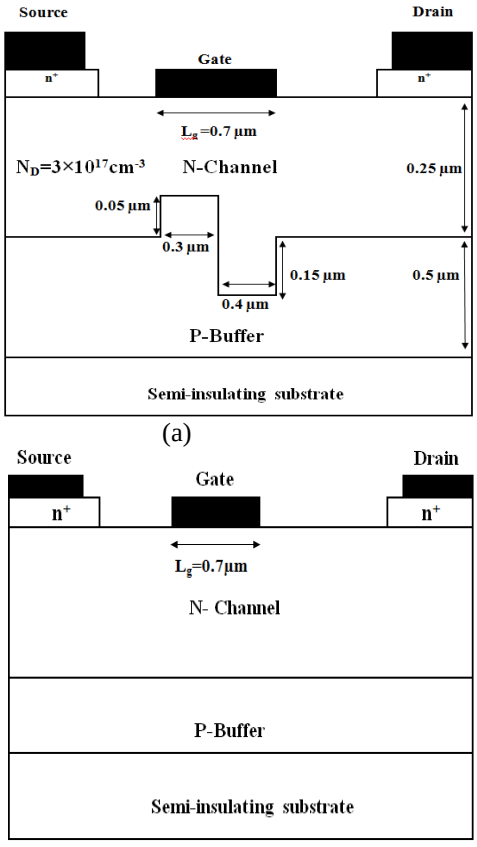

Fig. 1. Schematic cross-section of the (a) recessed p-buffer and (b) CRG structures[7] .

The dimensions of two structures are as follows: gate length L_g=0.7 µm, gate-drain spacing L_{gd} = 1 µm, gate-source spacing L_{gs} = 0.5µm, channel thickness 0.25 µm, and channel doping N_d = $3\times10^{17}cm^{-3}$. The doping and thickness of the P-buffer layer are 1.4 $\times10^{15}cm^{-3}$ and 0.5 µm, respectively. The substrate is semi-insulating. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV. The devices are simulated using two dimensional ATLAS software[9] with SiC material parameters[10-12].

2. RESULTS AND DISCUSSION

2.1 DC Trans- Conductance

Simulation results in the fig. 2 illustrate that the proposed structure increases the maximum DC trans-conductance at V_{DS}=5V and V_{GS}=0V. The recessed p-buffer layer into the channel region, reduces the channel thickness under the gate near the source. Therefore, narrower channel under the gate in the source side, increases vertical electrical field in the channel from the gate-source voltage and then increases the maximum DC trans-conductance. According to this figure, the maximum DC transconductance of the RPB structure is about 15% larger than that of the CRG structure. However, the threshold voltage has the negative shift in the proposed structure in comparison with the CRG structure.

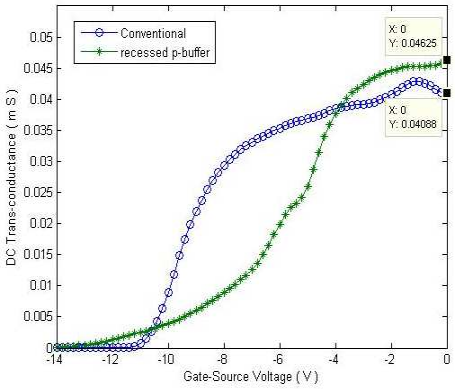

Fig. 2. DC Trans-conductance as a function of the gate-source voltage for two structures at V_{DS}=5V.

2.2 Gate-Source Capacitance

Fig. 3 shows the gate-source capacitance as a function of the frequency for two structures at V_{DS}=30V and V_{GS}=0V. As is shown in this figure, the RPB structure has smaller gate-source capacitance compared to CRG structure. It is clear from the fig. 1 that the proposed structure has narrower channel under the gate in the source side. Therefore, depletion layer extension to the source is reduced which decreases the gate-source capacitance.

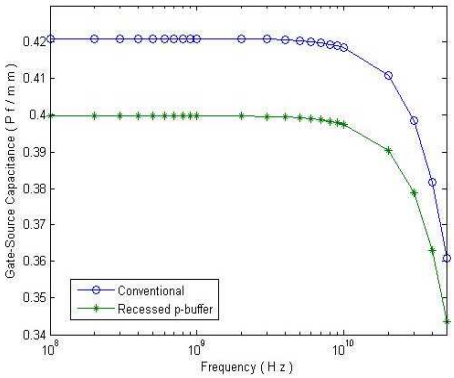

Fig. 3. Gate-source capacitance as a function of the frequency for two structures at V_{DS}=30V and V_{GS}=0V.

2.3 Cut-off and Maximum Oscilation Frequency

Two important high frequency parameters for a transistor are cut-off frequency (f_T) and maximum oscilation frequency (f_{max}). These two parameters can be calculated from the below equations[8] where g_m is the maximum DC trans-conductance and c_{gs} is the gate-source capacitance.

$$f_T = \frac{g_m}{2\pi C_{gs}} \quad (1)$$

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g}} \quad (2)$$

Two above equations show that a larger g_m/c_{gs} ratio, improves the f_T and f_{max}. Simulation results in the figs. 2 and 3 illustrate that the proposed structure has larger g_m and smaller c_{gs} in comparison with the conventional recessed gate structure. Therefore, the RPB structure has larger g_m/c_{gs} ratio and then has larger f_T and f_{max}. Also, it is clear that a smaller channel thickness under the gate in the source side compared to channel thickness under the gate in the drain side can be used to improve the high frequency performance of the conventional recessed gate SiC MESFET.

2.4 Drain Current

Fig. 4 shows the simulated drain currents with respect to the drain voltages for two structures at V_{GS}=0V. As can be seen in the figure, the proposed structure improves the saturated drain current. To allow for high drain current, a large product of the channel doping and thickness (N × a) is required [7]. Therefore, the channel thickness under the gate is an important factor in the drain current. It can be seen from the fig. 1(a) that the recess depth of the p-buffer layer into the channel in the source side is smaller than the recess depth of the channel into the p-buffer layer in the drain side. According to fig.1, the channel thickness under the gate in the drain side has been increased significantly in comparison with the source side but the drain current improvement is slightly. Therefore, the effect of channel thickness under the gate in the source side is more than that of the drain side. Simulation results in the fig. 5 show that the breakdown voltage points for two structures. According to this figure, the breakdown voltage of the proposed structure is smaller compared to CRG structure. Thicker channel under the gate in the drain side, reduces the maximum electrical field in the channel at the gate corner near the drain which increase the breakdown voltage slightly.

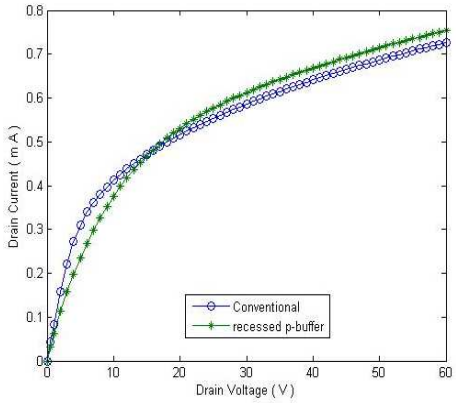

Fig. 4. simulated curves of drain currents as a function of drain voltages for two structures at V_{GS}=0V.

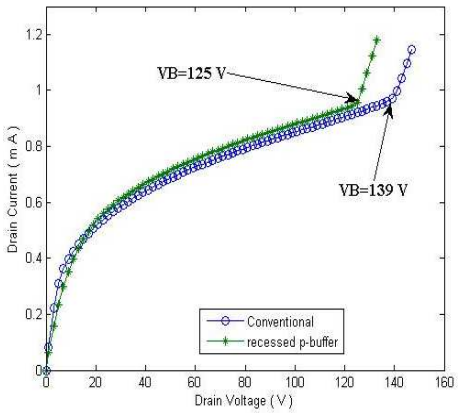

Fig. 5. Drain current versus drain voltages showing breakdown voltage point for two structures at V_{GS}=-1V.

2.5 DC Output Conductance

Fig. 6 shows the DC output conductance for two structures at V_{GS}=-1V. It can be seen from the figure that the RPB structure has smaller DC output conductance in linear region than CRG structure. The channel thickness under the gate in the source side of the RPB structure is smaller than that of the CRG structure which increases control of carrier transfer in the channel with gate-source voltage. Therefore, dependence of drain current to drain voltage is decreased and then the DC output conductance will be reduced. The maximum DC output conductance for the RPB structure is about 35% less than that of the CRG structure.

CONCLUSION

DC and RF characteristics of a conventional recessed gate and a recessed p-buffer layer SiC MESFET are simulated. The Drain current, DC output conductance, DC trans-conductance, gate-source capacitance, cut-off and maximum oscilation frequency for two structures are studied in detailes. Simulation results demonstrate that the RPB structure improves saturated drain current, maximum DC trans-conductance, maximum DC output conductance, gate-source capacitance, cut-off and maximum oscilation frequency compared to CRG structure. Howevere, RPB structure reduces breakdown voltage slightly.

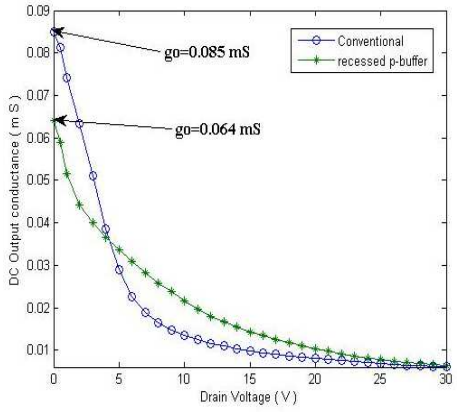

Fig. 6. DC output conductance as a function of the drain-source voltage for two structures at V_{GS}=-1V.

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