A Linear Tunable Amplifier for Implantable Neural Recording Applications

Hamidreza Rezaee-Dehsorkh, Nassim Ravanshad, Reza Lotfi, Khalil Mafinezhad
Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
{hr_rezaee, n_ravanshad, rlotfi}@ieee.org, mafinezhad@um.ac.ir

***Abstract*— A fully integrated tunable low-noise amplifier for neural recording applications is presented that is highly linear over the entire signal band. A modified system design is presented to optimize the area/noise/linearity performance. A novel pseudo-resistor with improved linearity is also proposed. This design, simulated in a 0.18-µm CMOS process, consumes 41.4 µW from a 1.8-V supply. The simulated integrated input-referred noise is 2.61 μV_{rms} over 300 Hz to 10 kHz. The amplifier also provides an output swing of 1 V_{P-P} with a total harmonic distortion of -43.61 dB at 300 Hz and -46.41 dB at 10 kHz.**

I. INTRODUCTION

Bio-potential amplifier is one of the most critical blocks in neural recording systems used by neuroscientists in various biomedical applications including brain–machine interface and neural prostheses. The main challenges in the design of the analog front-end of sensor interface (SI) circuits are derived from the nature of neural signals. Due to the small amplitude of neural signals, amplification must be performed before these signals can be digitized or analyzed. An integrated front-end amplifier (FEA) for neural signals must have sufficiently low input-referred noise to detect signals as small as a few tens of micro-volts in amplitude. Also the amplifier must have sufficient dynamic range for large-amplitude input signals (1-2 mV). The input impedance of the SI must be higher than the equivalent impedance of the electrode-tissue interface. The frequencies of neural signals span from a few hertz to a few kilo hertz. Therefore, the amplifier must amplify the signals in the band of interest while introducing a large enough dynamic range. Furthermore, the electrode-tissue interface usually inserts a high DC offset in the input signal which has to be removed by a high-pass filter not to saturate the amplifier [1]-[3]. Also, the amplifier should have a high common-mode and power-supply rejection ratios to minimize any interference from 50/60 Hz power line noise and power supply noise. If tissue cells are exposed to elevated temperatures for a long time, they will be destroyed. Thus, the SI circuit must operate at low power levels to minimize tissue heating. In addition, the SI circuit should consume little silicon area and use few off-chip components to minimize the size [3].

Since the peak amplitude of the neural signals varies based on the electrode type and conditions, the gain of the amplifier must be programmable. Also, the amplifier circuit parameters, e.g. the values of the resistors and the parameters of the operational transconductance amplifier (OTA) may change with process variations. Therefore, the bandwidth of the amplifier must be tunable as well. Note that the temperature of the implantable SI circuit is almost constant [3].

Another design issue in SI circuit is the linearity of the amplifier. Not only the linearity of the resistors, usually implemented employing MOS pseudo-resistors, but also the tracking error of the amplifier affect the linearity of the FEA. Although several attempts have been reported to decrease the power consumption and increase the signal-to-noise-ratio (SNR) of biomedical sensor interface systems [1]-[4], only a few works have discussed the linearity of these systems [2, 5].

This paper presents an integrated tunable neural recording sensor interface amplifier. The structure of the FEA including a low-noise amplifier, a tunable band-pass filter and a variable gain amplifier (VGA) is modified in order to optimize the noise, linearity and area performance. Also a novel pseudo cross-coupled tunable pseudo-resistor structure is introduced for the adjustment of low-cutoff frequency of the amplifier.

The paper is organized as follows: section II describes the challenges in the system architecture and design, proposed pseudo cross-coupled resistor and its comparison with the previous works. Section III reports the simulation results, and section IV concludes the paper.

II. SENSOR INTERFACE CIRCUIT DESIGN

In this section, design considerations of a low-noise front-end amplifier for neural recording system with low- and high-cutoff frequencies of 300 Hz and 10 kHz will be discussed. The overall system gain should be programmable with a nominal value of 54 dB. Using a 0.18 µm CMOS technology with a supply voltage of 1.8 V, the output swing is chosen to be 1 V_{p-p}. Since the output of the amplifier is digitized using a successive approximation register (SAR) analog-to-digital converter (ADC), the amplifier should be able to drive a switched capacitor of 20 pF.

In literature several reports have been presented to implement FEAs for implantable biomedical devices both in single-stage [3, 4, 5, 7, 8] and multi-stage architecture [1, 2, 6]. The capacitively-coupled amplifier that is employed in the stages of the amplifier shown in Fig.1 is commonly used to achieve good trade-offs between the performance, power, and area and to make the design of tunable and reconfigurable band-pass filters easier [2]. The choice of the number of the stages of the amplifier and the specifications of each stage greatly affects the overall system performance. The system design methodology proposed in this paper will be discussed in sub-section A. Furthermore, since the resistance of the employed resistors in such low-frequency applications is extremely high, realizing the resistors is another design challenge. MOS pseudo-resistors that occupy very small area are good candidates for the real resistors [7]. The main

978-1-61284-857-0/11/$26.00

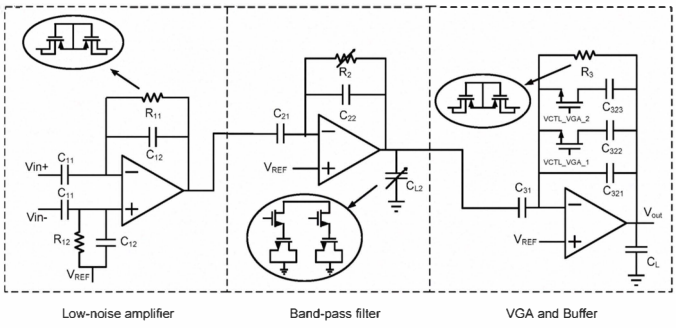

Figure 1. Schematic of the proposed three-stage amplifier.

drawback of using pseudo-resistors is the non-linearity which will be explained in sub-section B.

A. System Design

If the amplifier is realized using a single stage, because of the large voltage swing of the pseudo-resistor, the linearity behavior of the pseudo-resistor is degraded. In addition, since the entire gain should be realized using a single stage (where the gain is determined by the ratio of the input and the feedback capacitors), the input capacitor of the single-stage amplifier will be large, decreasing the input impedance of the SI circuit and increasing the chip area. Furthermore, in the single-stage amplifier approach, the linear tracking speed of the front-end output is limited by the effective bandwidth of the input signal [2]; i.e. since the high-cutoff frequency of the amplifier is limited and the load capacitor is relatively large, in order for the amplifier to have suitable settling behavior, additional buffer is required to drive the load capacitor.

To overcome the above-mentioned problems, two-stage amplifier was proposed in [2]. In this structure, the input-referred noise power of the first stage, inversely proportional to the load capacitance [3], must be small. Hence, a large load or compensation capacitor for the first stage is needed [7], leading to additional circuit area.

Therefore, the high-cutoff frequency can not be realized in the first and last stages. Thus, an intermediate stage should be inserted between the first and last stages that sets the high-cutoff frequency of the system. The proposed structure is shown in Fig. 1. The SI circuit consists of a low-noise amplifier (LNA), a band-pass filter, and a variable gain amplifier (VGA) the output of which is fed to a successive-approximation ADC.

At the first stage, the input differential signal is capacitively fed to the inputs of this stage from the electrodes to reject the dc polarization of the electrodes. The capacitor ratio of C_{11}/C_{12} is used to set the gain (G_1) using a negative feedback loop. R_{11} and R_{12} are large non-tunable pseudo-resistors. The low-cutoff frequency of this stage ($1/(2\pi R_{11}C_{12})$) is much lower than low-cutoff frequency of the overall system. V_{REF} is a reference voltage that sets the input and the output common-mode voltages of the OTA through R_{11} and R_{12}. The main sources of the first-stage noise which has a significant contribution in the overall input-referred noise of the amplifier are the OTA and pseudo-resistors. The OTA noise can be minimized by increasing the transconductance of the OTA (i.e. G_m). So, the high-cutoff frequency of the first stage ($G_mC_{12}/2\pi C_{L1}C_{11}$) [3] is larger than the neural signal bandwidth. Below a particular frequency (f_{corner}), the noise contribution from the pseudo-resistors will dominate [3]. To minimize the noise contribution from the pseudo-resistors, f_{corner} must be minimized as much as possible. Since f_{corner} is inversely proportional to $C_{11}\sqrt{R_{11}}$ [3], C_{11} and R_{11} must be as large as possible. Note that there is a trade-off between f_{corner} and the input impedance of the amplifier.

The second stage of the amplifier is a tunable band-pass filter removing the low- and high-frequency content of the neural signals. The low-cutoff frequency of the overall system (obtained from $1/(2\pi R_2C_{22})$) is tunable employing a tunable pseudo-resistor as R_2 using two digital bits. The structure of this pseudo-resistor will be explained in the following sub-section. C_{L2} consists of two MOSCAPs and two switches tuning the high-cutoff frequency of the entire system by two other digital bits. A current-mirror amplifier is used as the second stage OTA.

The pseudo-resistor that sets the low-cutoff frequency of the entire system leads to a large value for f_{corner} and thus a large amount of noise power. To reduce the noise contribution of this pseudo-resistor, the low-cutoff frequency must be set by the next stages. But upper stages have larger voltage swing across non-linear pseudo-resistor. Thus, there is a trade-off between the system linearity and noise power. Therefore, the second stage is a suitable place to set the low-cutoff frequency of the system.

The third stage is a VGA and buffer. The gain of this stage (G_3) is equal to C_{31}/C_{32} where C_{32} is the equivalent feedback capacitance that is controlled by the last two digital bits. R_3 is a large non-tunable pseudo-resistor that sets the input common-mode voltage of the OTA. For both the first and the third stages, two-stage amplifiers are used as the OTAs. In order to minimize the amplifier tracking error, the transconductance of OTA must be increased. So, the high-cutoff frequency of this stage is more than the neural signal bandwidth. Note that the gain tuning can be implemented in each of the stages using a variable input or feedback capacitor in that stage. Using a variable input capacitor has two drawbacks: first, the input capacitor is much larger than the feedback capacitor and thus a variable input capacitor occupies larger area than the case where the feedback capacitor is variable; second, the input capacitor of each stage is the load of previous one and its variations impacts the circuit behavior. The feedback capacitor of each stage is smaller than the load capacitor of it and does not affect the circuit performance. The second stage is not suitable for implementation of the gain tuning because low-cutoff frequency of the amplifier depends on its feedback capacitor. The third stage is therefore the best place to realize the gain tuning because the effect of the gain variation of this stage on the input-referred noise of the entire system is minimum.

The optimum distribution of the voltage gain in the three stages has been derived using a MATLAB code as $G_1=50$, $G_2=C_{21}/C_{22}=2$ and $G_3=5$. By realizing the gain of the entire amplifier in three stages using the ratios of the capacitors, one

can readily conclude that the area of the entire SI circuit dominated by the capacitors will be reduced [6].

B. Proposed Tunable Pseudo-Resistor

Several design issues should be considered in the design of tunable pseudo-resistors. They should be simple to implement and also occupy a small chip area. They should also have minimal effect on the total system characteristics by providing minimum added parasitic capacitance, noise and distortion. In order to reduce the distortion imposed by these resistors, they should have a linear characteristic by having a symmetric variation around the common-mode voltage. Besides, the variation of the resistance over the entire swing range and in the frequency band should be low. Also the resistance should be minimally sensitive to process variations, OTA offset and common-mode variations. Note that tunable pseudo-resistors need one or more digital-to-analog converters (DAC) to be digitally tuned.

There are various types of structures for implementing tunable pseudo-resistors. The first type employs voltage-controlled resistors. The simplest structure of this type is a gate-voltage controlled MOSFET as shown in Fig. 2 (a) [4]. This structure is easy to implement and easily tunable by using only one DAC. Also it has a low added parasitic capacitance and very low added noise. But the equivalent resistance in this architecture is not symmetric around the common-mode voltage and its variation in the swing range is high. So the linearity of the system that uses this architecture is poor, especially at low frequencies. But the resistor has little impact on the linearity at high frequencies. For example, by using this structure in our system, the total harmonic distortion (THD) of the entire circuit is degraded from -46.5 dB at the input frequency of 10 kHz to about -20 dB at around 300 Hz. Also the resistance is sensitive to process variations, OTA offset and common-mode voltage variations.

The second voltage-controlled architecture is a complementary structure composed of one NMOS and one PMOS transistor as shown in Fig. 2 (b) [8]. This structure is more complicated than a single transistor because two separate control voltages, i.e. $V_{Tune,P}$ and $V_{Tune,N}$ are needed to tune the resistor. The designer can adjust these two control voltages for achieving a symmetric variation around the common-mode voltage. But this symmetry is very sensitive to process and common-mode voltage variations and also the OTA offset. Therefore, although the resistor has a low added parasitic capacitance, very low added noise and a good linearity both in low and high frequencies at the tuned point, it can hardly be a good choice in realistic design.

The next type of tunable pseudo-resistors is current-controlled resistors. The simplest structure of this type is a current-controlled single transistor shown in Fig. 2 (c) [5]. The current-controlled transistor structure is simple to implement and can be easily tuned. It has low added parasitic capacitance and noise. But the resistance variation around the common-mode voltage is not completely symmetric and so its linearity is poor at low frequencies (simulated value of THD is higher than -10 dB around 300 Hz). Although this structure is sensitive to process and OTA offset, it is not sensitive to common-mode variations. Using this capability, a symmetric

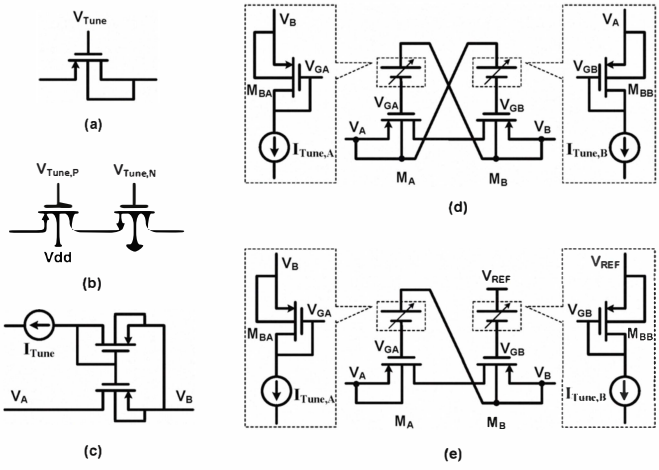

Figure 2. Pseudo-resistors: (a) voltage-controlled transistor, (b) complementry structure, (c) current-controlled transistor, (d) cross-coupled structure, and (e) pseudo cross-coupled structure.

and low-sensitivity structure is proposed in [2]. This cross-coupled structure is shown in Fig. 2 (d). This structure can be easily implemented and tuned by using two similar DACs. It shows a roughly symmetric variation around the common-mode voltage in all process corners and thus a good linearity. Also, the sensitivity to the process variations is small. Finally, this structure is insensitive to common-mode variations and the offset of the OTA.

Despite the good operation of cross-coupled pseudo-resistor regarding the sensitivity, the variation of the resistance around the common-mode voltage is not completely symmetric, resulting in an unwanted increase in the THD value. Also, this structure imposes a high amount of excess noise to the amplifier. To illustrate the problem, suppose that the node V_A in Fig. 2 (d) is connected to the negative input node of the OTA and the node V_B is connected to the output of the OTA. Then the current $I_{Tune,B}$ is drawn from the OTA output via the resistor. This event leads to a voltage difference between the OTA input and the output common-mode voltages. In order to reduce this voltage difference to tens of milli-volts, $I_{Tune,B}$ should be selected small, even in the order of few tens of pico-amperes; making the design of the stable DAC hardly possible.

In order to show how a dc voltage across the resistor will degrade the resistor linearity, in Fig. 3 the simulated resistance is plotted as a function of the voltage difference across the resistor. As it can be seen, the resistance variation around the zero voltage is symmetric and any dc voltage across the resistor (even in the order of few tens of milli-volts) will result in asymmetry.

On the other hand, the dc current flow through the transistors M_A and M_B increases their transconductance dramatically and so increases the current noise spectral density of the these transistors. Also the effect of the noise power of the biasing transistors (M_{BA} and M_{BB}) on the total output noise increases; because it is directly proportional to the transconductance of the transistors M_A and M_B. These lead to more than 40 % increase of the resistor noise voltage when referred to the input of the stage.

To avoid any DC current flow into the resistor, a new structure shown in Fig. 2 (e) is proposed. Since V_A is the input node of the OTA which has very small transient variations, the control voltage of M_B can be connected to a DC voltage with a value equal to the DC level of V_A such as V_{REF}. This pseudo cross-coupled structure offers all the advantages of the cross-coupled structure. Using this biasing structure, no dc current flows through the resistor and thus no dc voltage appears across the resistor. Therefore, the resistor has a symmetric characteristic around the common-mode voltage and so it is more linear. Also, because there is no dc current flowing through the transistors M_A and M_B, their transconductances are very small and the resistor has much lower added noise. By using this structure, the THD of the system is improved from -33.78 dB to -43.61 dB at 300 Hz and from -44.05 dB to -46.41 dB at around 10 kHz and the input-referred noise voltage of the entire circuit is reduced from 2.65 μV_{rms} to 2.61 μV_{rms}. The pseudo cross-coupled structure is somewhat sensitive to the OTA offset, which can be overcome by designing a low-offset OTA. Note that all of the simulated values mentioned above have been obtained by simulating the proposed structure of sub-section A as test bench.

III. Simulation Results

The tunable amplifier presented here has been designed and simulated in TSMC 0.18 µm CMOS process in all process corners. The DAC of the second stage pseudo-resistors is tuned in the process corners to have a nearly constant low-cutoff frequency. Also the high-cutoff frequency is kept constant using switchable MOSCAPs. Furthermore, the gain is tunable using two other bits in the range of 52 dB to 57 dB. The simulation results of the entire system are compared to other works in Table I. Using the proposed system architecture leads to very low input-referred noise voltage. Noise efficiency factor (NEF) [3] is a figure of merit to compare the noise, supply current and bandwidth of the biomedical amplifiers. This work has an NEF of 4.73 that is reasonable for a three-stage amplifier with a large bandwidth output buffer and large load of 20 pF. The linearity performance of this work is comparable to other reports in the entire frequency band. Also, using three-stage architecture has led to a small total capacitor (and thus small area) while having high gain.

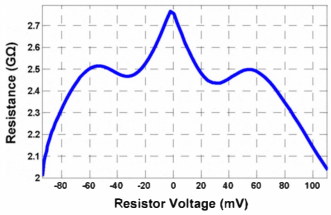

Figure 3. Resistance variation of the cross-coupled pseudo-resistor vs. the voltage across the resistor.

IV. Conclusion

An integrated tunable neural recording sensor interface circuit has been demonstrated. A system architecture that employs an LNA, a band-pass filter, and a VGA was introduced to optimize the area, reduce the total input-referred noise, and increase the linearity of the circuit. A novel pseudo cross-coupled tunable resistor has also been proposed that effectively improves the THD over 300 Hz to 10 kHz frequency range at 1 V_{p-p} output swing. The sensor interface amplifier consumes 41.4 µW power with a 1.8 V supply.

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TABLE I. Performance Comparison With Other Designs

Parameter		Harrison [7]	Ghovanloo [8]			Zou [2]	This work	
Technology		1.5 µm	1.5 µm			0.35 µm	0.18 µm	
Supply voltage		±2.5 V	±1.7 V			1 V	1.8 V	
Output Swing		–	1.8 Vpp			1 Vpp	1 Vpp	
Pre-amplifier Gain		39.5 dB	39.3, 45.6 dB {Tunable}			45.6 - 60 dB (Tunable)	52 - 57 dB (Tunable)	
Pre-amplifier Bandwidth		0.025Hz – 7.2kHz	0.015 – 4kHz (Tunable)			4.5mHz – 292Hz (Tunable)	300 Hz – 10 kHz (Tunable)	
Power consumption		80 µW	27.2 µW			445-895 nW	41.4 µW	
Input-referred Noise		2.2 µVrms (0.5Hz-50kHz)	3.6 µVrms (20Hz-10kHz)			2.5 µVrms (0.05Hz-460Hz)	2.61 µVrms (300Hz-10kHz)	
Noise efficiency factor		4	4.9			3.26	4.73	
Linearity	Frequency	–	10Hz	100Hz	1kHz	–	300Hz	10kHz
	Swing (peak-to-peak)	16.7mV (input)	23mV (input)	19mV (input)	17.4mV (input)	1V (output)	1V (output)	1V (output)
	THD	-40 dB	-40 dB	-40 dB	-40 dB	-44.4 dB	-43.61 dB	-46.41 dB
CMRR		≥ 83 dB	–			≥ 71.2 dB	75.2 dB	
PSRR		≥ 85 dB	–			≥ 84 dB	84.46 dB	
Total Capacitor		40.4 pF	40.8 pF			–	23 pF	
Simulation / Measurement		Measurement	Measurement			Measurement	Simulation	