

# Design-Oriented Study of Advanced Synchronous Reference Frame Phase-Locked Loops

Saeed Golestan, *Member, IEEE*, Mohammad Monfared, *Member, IEEE*, and Francisco D. Freijedo

**Abstract**—In grid-connected applications, the synchronous reference frame phase-locked loop (SRF-PLL) is a commonly used synchronization technique due to the advantages it offers such as ease of implementation and robust performance. Under ideal grid conditions, the SRF-PLL enables a fast and accurate phase/frequency detection; however, unbalanced and distorted grid conditions highly degrade its performance. To overcome this drawback, several advanced PLLs have been proposed, such as the multiple reference frame-based PLL, the dual second-order generalized integrator-based PLL, and the multiple complex coefficient filter-based PLL. In this paper, a comprehensive design-oriented study of these advanced PLLs is presented. The starting point of this study is to derive the small-signal model of the aforementioned PLLs, which simplifies the parameter design and the stability analysis. Then, a systematic design procedure to fine tune the PLLs parameters is presented. The stability margin, the transient response, and the disturbance rejection capability are the key factors that are considered in the design procedure. Finally, the experimental results are presented to support the theoretical analysis.

**Index Terms**—Dual second-order generalized integrator (DSOGI), multiple complex coefficient filter (MCCF), multiple reference frame (MRF), phase-locked loop (PLL), synchronous reference frame (SRF), synchronization, three-phase grid-connected converters.

## I. INTRODUCTION

PROPER synchronization with the utility grid is one of the most important aspects in the control of grid connected power converters. Various synchronization techniques have been proposed in the literature. The zero-crossing detection methods [1], [2], the space-vector filtering method [3], the artificial-neural-network-based method [4], the recursive weighted least-squares estimation algorithm [5], the discrete Fourier transform and its modifications [6], [7], the methods based on the concept of adaptive notch filtering [8], [9], the Kalman filtering technique [10], the frequency-locked-loop-based methods [11], [12],

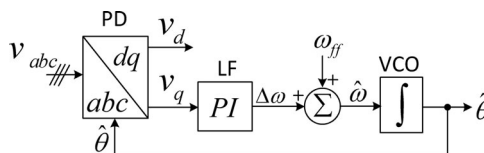


Fig. 1. Basic scheme of a conventional SRF-PLL.

and the phase-locked loop (PLL)-based algorithms [13]–[31] are among the existing synchronization techniques.

In grid-connected applications, the PLLs are the most widely used synchronization techniques. A PLL is a nonlinear closed-loop feedback control system which synchronizes its output signal in frequency, as well as in phase, with an input signal. A basic PLL consists of three building blocks: a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO). The main difference among the different PLLs typically lies in how the PD block is implemented.

For three-phase grid-connected power converters, a variety of PLLs have been developed recently; the most popular being the synchronous reference frame PLL (SRF-PLL). Fig. 1 illustrates the basic scheme of a conventional SRF-PLL. In this PLL, the three-phase input voltages are transformed to the  $dq$  synchronous reference frame by applying a combination of Clark and Park transformations. Using a feedback loop, the angular position of the  $dq$  reference frame is regulated in such a way that either the  $d$ - or  $q$ -axis component (depending on the transformation) becomes zero. Under ideal grid conditions, the SRF-PLL yields a satisfactory performance both in terms of the phase/frequency tracking capability and the dynamic response. However, under adverse grid conditions, i.e., when the grid voltage is unbalanced and/or harmonically distorted, it presents a degraded performance: high amplitude steady-state oscillations in the estimated phase/frequency arise. This problem can be mitigated by reducing the SRF-PLL's bandwidth at the expense of the dynamic response; however, this measure may not be an acceptable solution in some applications, such as grid-connected distributed generation systems [27], and low-voltage ride-through technologies [32], [33]. Another way to alleviate the aforementioned problem is to include additional low-pass filters (LPFs) in the control loop [34]. In this case, the careful design of the order and the cutoff frequency of the LPF must be done to provide a satisfactory compromise between the speed of response and the disturbance rejection capability.

For accurate phase/frequency estimation under unbalanced and/or distorted grid conditions, several advanced PLLs have been proposed in recent years, as alternatives to the conventional SRF-PLL. Their common idea, typically, is to employ the

Manuscript received January 17, 2012; revised April 2, 2012; accepted May 30, 2011. Date of current version September 27, 2012. This work was supported by the Abadan Branch, Islamic Azad University. Recommended for publication by Associate Editor K.-B. Lee.

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Digital Object Identifier 10.1109/TPEL.2012.2204276

specific “filtering” techniques to extract the fundamental-frequency positive-sequence component which is then fed to a conventional SRF-PLL. For instance, to prevent the double-frequency detection errors, caused by the fundamental-frequency negative-sequence component, a decoupled double synchronous reference frame PLL (DDSRF-PLL) is presented by Rodriguez *et al.* [22]. Another approach presented by Xiao *et al.* [23] is a multiple reference frame based PLL (MRF-PLL). The MRF-PLL utilizes the same idea of the DDSRF-PLL, except that it has a more straightforward implementation. Alternative approach reported by Rodriguez *et al.* [24] is a dual second-order generalized integrator based PLL (DSOGI-PLL), which works based on the instantaneous symmetrical components (ISC) theory in the stationary ( $\alpha\beta$ ) reference frame. A more recent structure presented by Guo *et al.* [25] is a multiple complex-coefficient-filter-based PLL (MCCF-PLL). The complex-coefficient filters (CCFs) have the unique characteristic of both frequency and sequence selectivity, meaning that, they can make the distinction between the negative and positive sequences for the same frequency.

The available design approaches for tuning of these advanced PLLs (i.e., MRF-PLL, DSOGI-PLL, and MCCF-PLL), all follow a common procedure as follows: 1) The dynamics of the filtering technique used to extract the fundamental positive-sequence component are neglected; i.e., the same small-signal model as the conventional SRF-PLL is considered for these more complex PLLs. This measure is justified by assuming a much faster dynamics for the filtering technique than the SRF-PLL. 2) The design instructions suggested for the conventional SRF-PLL are then employed to determine the LF parameters.

The main drawback of the aforementioned tuning approach is that the PLL small-signal model does not include the dynamics of the filtering technique and, therefore, is not accurate. On the other hand, the design instructions available for the conventional SRF-PLL (second-order PLL) are not able to extract the maximum benefits out of the potentialities of these more complex PLLs.

Focusing on the grid-connected applications, a comprehensive design-oriented study of advanced three-phase SRF-PLLs, such as the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL, is presented in this paper. To achieve this goal, the complete small-signal models for the PLLs under study are first derived. These models simplify the stability analysis and the parameter design. Based on the derived models, a systematic design procedure to fine tune the PLLs parameters is then suggested. The stability margin, the transient response, and the disturbance rejection capability are the key factors that are considered in the design procedure.

## II. SMALL-SIGNAL MODELING

The main focus in this section is to derive the small-signal model of the PLLs under study (the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL). To simplify the understanding of the procedure and provide a base for comparison, the small-signal model for a conventional SRF-PLL with additional LPFs (here, referred to as LSRF-PLL) is derived first. The derived

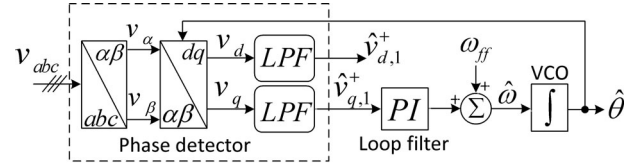


Fig. 2. Basic scheme of the LSRF-PLL.

model for the LSRF-PLL is then extended to the PLLs under study. To derive the small-signal models, a quasi-locked state is assumed [14].

### A. LSRF-PLL

Fig. 2 illustrates the basic scheme of the LSRF-PLL, in which:

- 1)  $\hat{\theta}$  is the estimated angle;
- 2)  $\hat{\omega}$  is the estimated frequency;
- 3)  $v_{abc}$  is the three-phase input voltage system;
- 4)  $\omega_{ff}$  is the nominal frequency and, throughout this paper, is considered to be  $2\pi 50$  rad/s.

The three-phase input voltages of the PLL are assumed to be unbalanced and harmonically distorted, as expressed in (1), where  $V_h^+$  ( $V_h^-$ ) and  $\phi_h^+$  ( $\phi_h^-$ ) are the amplitude and the phase angle of the  $h$ th harmonic component of the positive-(negative-) sequence of the input voltages, respectively:

$$\begin{aligned}
 v_a(t) &= \sum_{h=1}^{+\infty} [V_h^+ \cos(h\omega t + \phi_h^+) + V_h^- \cos(h\omega t + \phi_h^-)] \\
 v_b(t) &= \sum_{h=1}^{+\infty} \left[ V_h^+ \cos\left(h\omega t + \phi_h^+ - \frac{2\pi}{3}\right) \right. \\
 &\quad \left. + V_h^- \cos\left(h\omega t + \phi_h^- + \frac{2\pi}{3}\right) \right] \\
 v_c(t) &= \sum_{h=1}^{+\infty} \left[ V_h^+ \cos\left(h\omega t + \phi_h^+ + \frac{2\pi}{3}\right) \right. \\
 &\quad \left. + V_h^- \cos\left(h\omega t + \phi_h^- - \frac{2\pi}{3}\right) \right]. \quad (1)
 \end{aligned}$$

Applying the Clark ( $abc$ -to- $\alpha\beta$ ) transformation to the three-phase input voltages yields

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = [T_{\alpha\beta}] \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} v_\alpha^+(t) \\ v_\beta^+(t) \end{bmatrix} + \begin{bmatrix} v_\alpha^-(t) \\ v_\beta^-(t) \end{bmatrix} \quad (2)$$

where

$$[T_{\alpha\beta}] = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_{\alpha}^{+}(t) \\ v_{\beta}^{+}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h=1}^{+\infty} v_{\alpha,h}^{+}(t) \\ \sum_{h=1}^{+\infty} v_{\beta,h}^{+}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h=1}^{+\infty} V_h^{+} \cos(h\omega t + \phi_h^{+}) \\ \sum_{h=1}^{+\infty} V_h^{+} \sin(h\omega t + \phi_h^{+}) \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} v_{\alpha}^{-}(t) \\ v_{\beta}^{-}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h=1}^{+\infty} v_{\alpha,h}^{-}(t) \\ \sum_{h=1}^{+\infty} v_{\beta,h}^{-}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h=1}^{+\infty} V_h^{-} \cos(h\omega t + \phi_h^{-}) \\ -\sum_{h=1}^{+\infty} V_h^{-} \sin(h\omega t + \phi_h^{-}) \end{bmatrix}. \quad (5)$$

Applying the Park ( $\alpha\beta$ -to- $dq$ ) transformation to (2) gives

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = [T_{dq}] \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \begin{bmatrix} v_d^{+}(t) \\ v_q^{+}(t) \end{bmatrix} + \begin{bmatrix} v_d^{-}(t) \\ v_q^{-}(t) \end{bmatrix} \quad (6)$$

where

$$[T_{dq}] = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix}, \hat{\theta} = \hat{\omega}t + \hat{\phi}_1^{+} \quad (7)$$

$$\begin{aligned} \begin{bmatrix} v_d^{+}(t) \\ v_q^{+}(t) \end{bmatrix} &= \begin{bmatrix} \sum_{h=1}^{+\infty} v_{d,h}^{+}(t) \\ \sum_{h=1}^{+\infty} v_{q,h}^{+}(t) \end{bmatrix} \\ &= \begin{bmatrix} \sum_{h=1}^{+\infty} V_h^{+} \cos[(h\omega - \hat{\omega})t + \phi_h^{+} - \hat{\phi}_1^{+}] \\ \sum_{h=1}^{+\infty} V_h^{+} \sin[(h\omega - \hat{\omega})t + \phi_h^{+} - \hat{\phi}_1^{+}] \end{bmatrix} \\ \begin{bmatrix} v_d^{-}(t) \\ v_q^{-}(t) \end{bmatrix} &= \begin{bmatrix} \sum_{h=1}^{+\infty} v_{d,h}^{-}(t) \\ \sum_{h=1}^{+\infty} v_{q,h}^{-}(t) \end{bmatrix} \\ &= \begin{bmatrix} \sum_{h=1}^{+\infty} V_h^{-} \cos[(h\omega + \hat{\omega})t + \phi_h^{-} + \hat{\phi}_1^{+}] \\ -\sum_{h=1}^{+\infty} V_h^{-} \sin[(h\omega + \hat{\omega})t + \phi_h^{-} + \hat{\phi}_1^{+}] \end{bmatrix}. \end{aligned} \quad (8)$$

Under a quasi-locked condition (i.e.,  $\omega = \hat{\omega}$ , and  $\phi_1^{+} \approx \hat{\phi}_1^{+}$ ), (6) can be rewritten as

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \cong \underbrace{\begin{bmatrix} \bar{v}_d \\ \bar{v}_q \end{bmatrix}}_{\text{dc terms}} + \underbrace{\begin{bmatrix} \tilde{v}_d(t) \\ \tilde{v}_q(t) \end{bmatrix}}_{\text{disturbance terms}} \quad (10)$$

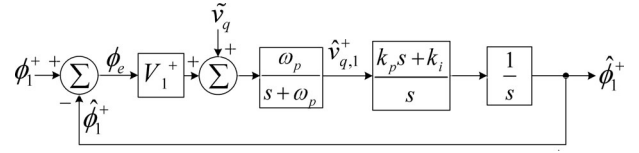


Fig. 3. Small-signal model of the LSRF-PLL.

where

$$\begin{aligned} \bar{v}_d &= v_{d,1}^{+} \approx V_1^{+} \\ \bar{v}_q &= v_{q,1}^{+} \approx V_1^{+} \underbrace{(\phi_1^{+} - \hat{\phi}_1^{+})}_{\phi_e} \end{aligned}$$

$$\begin{aligned} \tilde{v}_d(t) &= \sum_{h=2}^{+\infty} v_{d,h}^{+}(t) + \sum_{h=1}^{+\infty} v_{d,h}^{-}(t) \\ \tilde{v}_q(t) &= \sum_{h=2}^{+\infty} v_{q,h}^{+}(t) + \sum_{h=1}^{+\infty} v_{q,h}^{-}(t). \end{aligned} \quad (11)$$

Evidently, the mean value of  $v_d$  gives an estimation of the amplitude of fundamental positive-sequence component, and the mean value of  $v_q$  gives information about the phase estimation error. These information may be extracted by passing  $v_d$  and  $v_q$  through the LPF, as shown in Fig. 2. The LPF is considered to be of first order as follows:

$$\text{LPF}(s) = \frac{\omega_p}{s + \omega_p} \quad (12)$$

where  $\omega_p$  is the cutoff frequency.

Based on the previous analysis, the PD output signals (i.e.,  $\hat{v}_{d,1}^{+}$  and  $\hat{v}_{q,1}^{+}$ ) can be approximated in the Laplace domain as

$$\hat{v}_{d,1}^{+}(s) \approx \frac{\omega_p}{s + \omega_p} [V_1^{+} + \tilde{v}_d(s)] \quad (13)$$

$$\hat{v}_{q,1}^{+}(s) \approx \frac{\omega_p}{s + \omega_p} [V_1^{+} \phi_e(s) + \tilde{v}_q(s)]. \quad (14)$$

To minimize the phase error  $\phi_e$  and further attenuate the disturbance components,  $\hat{v}_{q,1}^{+}$  is passed through the LF (here, a proportional-integral (PI) controller). The nominal frequency (i.e.,  $\omega_{ff}$ ) is then added to the LF output signal, to reduce the control effort and expedite the initial lock-in process [28]. The resulting signal (i.e.,  $\hat{\omega}$ ) is integrated afterward to generate the estimated angle  $\hat{\theta}$ .

Based on the above information, and considering the LF transfer function as  $PI(s) = k_p + k_i/s$ , (where  $k_p$  and  $k_i$  are the proportional and integral gains, respectively), the small-signal model of the LSRF-PLL can be derived as shown in Fig. 3.

Under the frequency-locked condition, the fundamental negative-sequence component of the input voltage appears as a disturbance input to the PLL linearized model, pulsating at twice the input voltage fundamental frequency [see (9)]. In the same way, the input voltage harmonics, which dominantly are non-triplen odd harmonics (e.g., 5th<sup>-</sup>, 7th<sup>+</sup>, 11th<sup>-</sup>, 13th<sup>+</sup>, etc.), are sensed by the linearized model as even harmonic components (i.e., 6th<sup>±</sup>, 12th<sup>±</sup>, etc.) [29]. Thus, the disturbance input

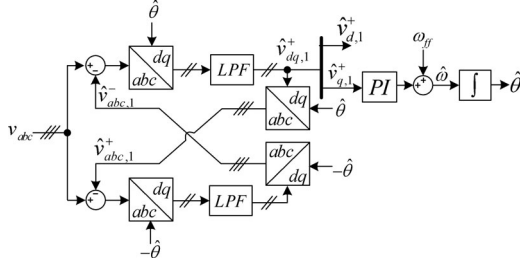


Fig. 4. Basic scheme of the MRF-PLL.

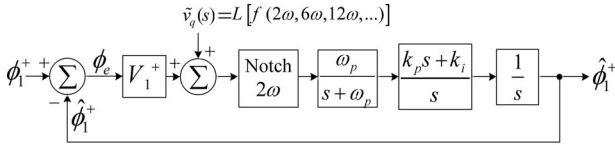


Fig. 5. Small-signal model of the MRF-PLL.

to the PLL linearized model (i.e.,  $\tilde{v}_q$ ) can be considered as

$$\tilde{v}_q(s) = L[f(2\omega, 6\omega, 12\omega, \dots)] \quad (15)$$

where  $L$  is the Laplace operator.

### B. MRF-PLL

Fig. 4 illustrates the MRF-PLL, proposed by Xiao *et al.* [23]. The MRF-PLL utilizes the same idea of the DDSRF-PLL [22], except that it has a more straightforward implementation.

MRF-PLL employs two synchronous reference frames rotating at the same angular speed, but in opposite directions, and a decoupling network in the natural abc reference frame to extract and separate the fundamental-frequency positive/negative-sequence components. In this way, the steady-state detection error caused by the fundamental negative-sequence component is eliminated.

In the MRF-PLL, as shown in Fig. 4, an estimation of the fundamental-frequency negative-sequence components (i.e.,  $\hat{v}_{abc,1}^-$ ) is subtracted from the input voltages. From the control point of view, it is equivalent to passing the input voltages through a sort of notch filters tuned at the fundamental frequency of negative sequence (see the Appendix for the proof). The resulting signals are then transformed to the dq reference frame, and passed through the LPFs. Keep in mind that the physical meaning of the frame transformation is the frequency displacement of the frequency response equal to the rotating speed of the synchronous reference frame [35]. Based on this point, the MRF structure in the dq reference frame can be approximated by an LPF cascaded with a notch-filter tuned at  $2\omega$ .

Based on the previous analysis, and what was stated in the previous section, the small-signal model of the MRF-PLL can be derived as shown in Fig. 5.

The notch filter with a notch gain at  $2\omega$  completely cancels the double-frequency disturbance input to the model, but introduces some limitations on the dynamic performance of the PLL. The reason is that, to achieve a robust performance, the PLL open-loop bandwidth ( $BW_{OL}$ ) must be sufficiently smaller than  $2\omega$ .

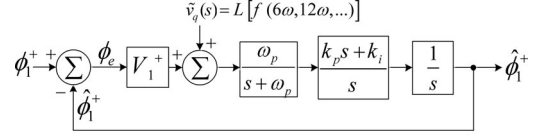


Fig. 6. Simplified small-signal model of the MRF-PLL.

For a  $BW_{OL}$  sufficiently smaller than  $2\omega$ , the notch filter has a negligible effect on the PLL dynamic performance. As a consequence, the small-signal model of the MRF-PLL can be simplified as depicted in Fig. 6. Notice that the double-frequency disturbance input to the model has been eliminated.

It should be pointed out that under highly distorted grid conditions, the MRF decoupling network can be simply extended to include the low-order harmonics, but at the cost of increased computational burden [36]. In this case (here, referred to as extended MRF-PLL), the same small-signal model as that shown in Fig. 6 can be considered for the PLL. The only difference is the disturbance input to the model, which is determined according to the number of the harmonic components that are compensated.

### C. DSOGI-PLL

Fig. 7(a) illustrates the general structure of the DSOGI-PLL, proposed by Rodriguez *et al.* [24]. The SOGI scheme is shown in Fig. 7(b), and its characteristic transfer functions are as follows:

$$D(s) = \frac{v'(s)}{v(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \quad (16)$$

$$Q(s) = \frac{qv'(s)}{v(s)} = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \quad (17)$$

where  $k$  is the damping factor, and  $v'$  and  $qv'$  are the filtered direct and in-quadrature versions of the input signal  $v$ , respectively.

The operating principle of the DSOGI-PLL is based on the ISC theory on the  $\alpha\beta$  reference frame as follows: the three-phase input voltages are transformed to the stationary ( $\alpha\beta$ ) reference frame by applying the Clark transformation. Two SOGI-based quadrature signal generators are then employed to provide the filtered direct and in-quadrature versions of  $v_\alpha$  and  $v_\beta$ , i.e.,  $v'_\alpha$ ,  $v'_\beta$ ,  $qv'_\alpha$ , and  $qv'_\beta$ , respectively. The positive-sequence calculator (PSC) block accepts these signals as inputs and extracts the positive-sequence  $\alpha\beta$  components using the ISC theory on the  $\alpha\beta$  domain [24]. The resulting signals (i.e.,  $\hat{v}_{\alpha,1}^+$  and  $\hat{v}_{\beta,1}^+$ ) are then fed to a conventional SRF-PLL to extract the phase angle and frequency information. The estimated frequency is fed back to the DSOGI/PSC structure to make it frequency adaptive.

In the following, it is demonstrated that from the control point of view, the DSOGI-PLL and the MRF-PLL are equivalent to each other. Thus, the same small-signal model as that of the MRF-PLL can be used for the DSOGI-PLL.



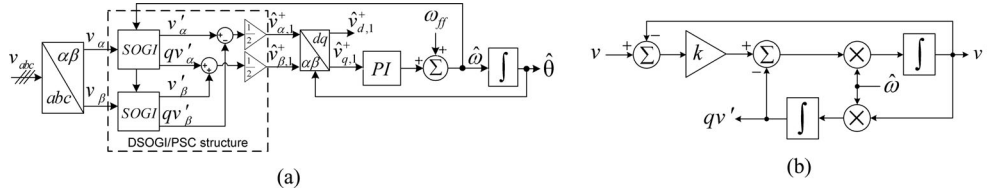


Fig. 7. DSOGI-PLL. (a) Basic structure. (b) SOGI block.

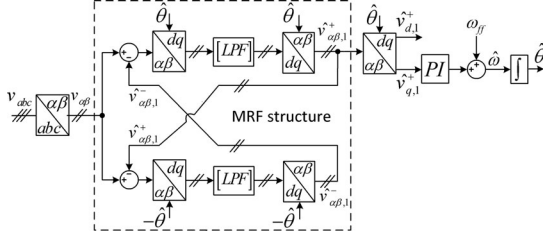


Fig. 8. Alternative representation of the MRF-PLL.

To simplify the analysis, let us redraw the MRF-PLL, as shown in Fig. 8, where

$$[\text{LPF}(s)] = \begin{bmatrix} \frac{\omega_p}{s + \omega_p} & 0 \\ 0 & \frac{\omega_p}{s + \omega_p} \end{bmatrix}.$$

By comparing Figs. 7(a) and 8, one can see that the only difference between the two PLL structures lies in the PD block. If it is demonstrated that the transfer function from the unbalanced input voltage vector (i.e.,  $[v_{\alpha\beta}]$ ) to the positive-sequence component extracted by the MRF structure is the same as that of the DSOGI/PSC structure, then the equivalence of two PLL structures is proven.

First, let us determine the input-to-output transfer function of the DSOGI/PSC structure, which is

$$\begin{aligned} [\hat{v}_{\alpha\beta,1}^+(s)] &= \frac{1}{2} \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} [v_{\alpha\beta}(s)] \\ &= \frac{1}{2} \frac{k\hat{\omega}}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \begin{bmatrix} s & -\hat{\omega} \\ \hat{\omega} & s \end{bmatrix} [v_{\alpha\beta}(s)]. \end{aligned} \quad (18)$$

Now, we determine the input-to-output transfer function of the MRF structure. From Fig. 8, we can obtain

$$[\hat{v}_{\alpha\beta,1}^+(t)] = [T_{dq}]^t \{ [\text{LPF}(t)] * \{ [T_{dq}] \{ [v_{\alpha\beta}(t)] - [\hat{v}_{\alpha\beta,1}^-(t)] \} \} \} \} \quad (19)$$

$$[\hat{v}_{\alpha\beta,1}^-(t)] = [T_{dq}] \{ [\text{LPF}(t)] * \{ [T_{dq}]^t \{ [v_{\alpha\beta}(t)] - [\hat{v}_{\alpha\beta,1}^+(t)] \} \} \} \} \quad (20)$$

where the superscript  $t$  denotes the transpose operation, and the asterisk (\*) denotes the convolution operation.

By taking the Laplace transform from the both sides of (19) and (20), we can obtain

$$[\hat{v}_{\alpha\beta,1}^+(s)] = [H(s)] \{ [v_{\alpha\beta}(s)] - [\hat{v}_{\alpha\beta,1}^-(s)] \} \quad (21)$$

$$[\hat{v}_{\alpha\beta,1}^-(s)] = [H(s)]^t \{ [v_{\alpha\beta}(s)] - [\hat{v}_{\alpha\beta,1}^+(s)] \} \quad (22)$$

where

$$[H(s)] = \frac{\omega_p}{(s + \omega_p)^2 + \hat{\omega}^2} \begin{bmatrix} s + \omega_p & -\hat{\omega} \\ \hat{\omega} & s + \omega_p \end{bmatrix}. \quad (23)$$

Substituting (22) into (21) yields

$$\{ [I] - [H(s)][H(s)]^t \} [\hat{v}_{\alpha\beta,1}^+] = [H(s)] \{ [I] - [H(s)]^t \} [v_{\alpha\beta}]. \quad (24)$$

Using simple mathematical relations, it can be shown that

$$[H(s)][H(s)]^t = [H(s)]^t[H(s)] = \frac{\omega_p^2}{(s + \omega_p)^2 + \hat{\omega}^2} [I]. \quad (25)$$

Using (25), and after some simple mathematical manipulations, (24) can be expressed as

$$[\hat{v}_{\alpha\beta,1}^+(s)] = \frac{\omega_p}{s^2 + 2\omega_p s + \hat{\omega}^2} \begin{bmatrix} s & -\hat{\omega} \\ \hat{\omega} & s \end{bmatrix} [v_{\alpha\beta}(s)]. \quad (26)$$

Comparing (18) and (26), one can see that for  $\omega_p = k\hat{\omega}/2$ , the DSOGI/PSC and MRF structures are two equivalent systems. In other words, they perform the same function (i.e., sequence separation) on the different reference frames. Thus, the same small-signal model as that of the MRF-PLL can be used for the DSOGI-PLL.

It should be noted that due to the variations of the input frequency (and hence the estimated frequency), the equivalency condition (i.e.,  $\omega_p = k\hat{\omega}/2$ ) may not be exactly satisfied. However, since the grid frequency is typically allowed to change in a narrow band (e.g.,  $47 \text{ Hz} < \omega < 52 \text{ Hz}$ , as defined in [37]), selecting  $\omega_p = k\omega_{ff}/2$  gives rise to a very similar properties for both PLL techniques, as it will be shown later in Section IV.

It is worth remarking that under highly distorted grid conditions, the performance of the DSOGI-PLL can be simply improved by adding extra SOGI blocks tuned at the proper frequencies [11]. In this case, the DSOGI-PLL turns to the multiple-SOGI PLL (MSOGI-PLL).

#### D. MCCF-PLL

Fig. 9(a) illustrates the general structure of the MCCF-PLL, proposed by Guo *et al.* [25]. The submodules of the MCCF structure are shown in Fig. 9(b).

The operating principle of this synchronization technique is based on using CCFs, which have a long history of use, particularly in the field of communications [38]. Contrary to the real-coefficient filters, CCFs have the unique characteristic of both frequency and sequence (polarity) selectivity, meaning that they can make the distinction between the negative and positive sequences (polarities) for the same frequency [25].

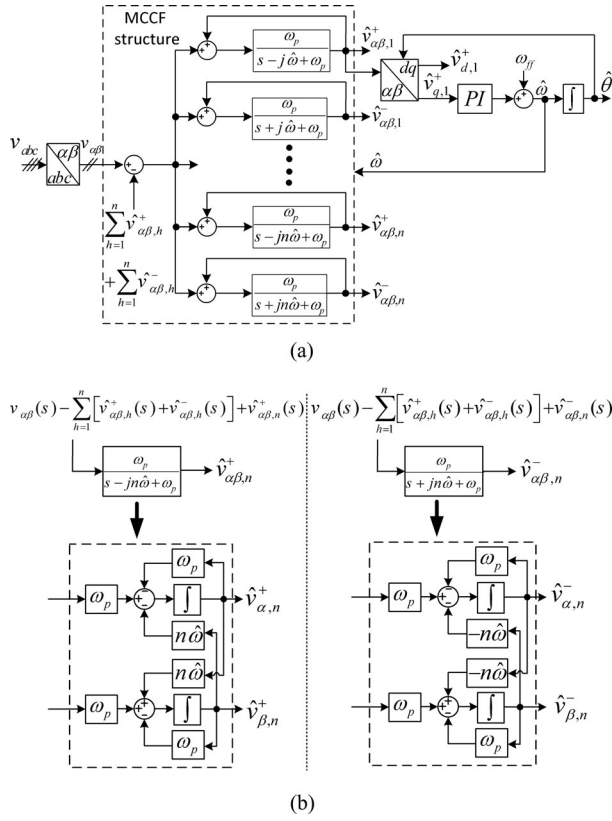


Fig. 9. MCCF-PLL. (a) Basic structure. (b) Submodule structure of the MCCF.

The MCCF structure shown in Fig. 9(a) is composed of several CCFs, working in a collaborative way, each of which is responsible for extracting a selected sequential component from the input voltage. Under unbalanced but relatively low distorted grid conditions, a two-module (TM) system of the MCCF structure (tuned at  $\pm\omega$ ) is recommended in [25]. However, under highly distorted grid conditions, the synchronization performance with the TM structure may not be acceptable. In this case, a multiple-module (MM) system is recommended in [25]. Notice that to deal with the frequency variations, the estimated frequency is fed back to the MCCF structure.

Based on Fig. 9(a), we can derive the equations for the estimated fundamental positive-sequence component as (27) and (28). Based on Fig. 9(b), and performing some mathematical manipulations, we can rewrite (27) and (28) as (29) and (30), respectively. Substituting (29) into (30), and (30) into (29), and rearranging the results into matrix form, give (31). Following a similar procedure, we can also derive (32):

$$\hat{v}_{\alpha,1}^+(s) = \frac{\omega_p}{s - j\hat{\omega} + \omega_p} \times \left( v_{\alpha}(s) - \sum_{h=1}^n [\hat{v}_{\alpha,h}^+(s) + \hat{v}_{\alpha,h}^-(s)] + \hat{v}_{\alpha,1}^+(s) \right) \quad (27)$$

$$\hat{v}_{\beta,1}^+(s) = \frac{\omega_p}{s - j\hat{\omega} + \omega_p} \times \left( v_{\beta}(s) - \sum_{h=1}^n [\hat{v}_{\beta,h}^+(s) + \hat{v}_{\beta,h}^-(s)] + \hat{v}_{\beta,1}^+(s) \right) \quad (28)$$

$$\hat{v}_{\alpha,1}^+(s) = \frac{\omega_p}{s + \omega_p} \left( v_{\alpha}(s) - \sum_{h=2}^n \hat{v}_{\alpha,h}^+(s) - \sum_{h=1}^n \hat{v}_{\alpha,h}^-(s) \right) - \frac{\hat{\omega}}{s + \omega_p} \hat{v}_{\beta,1}^+(s) \quad (29)$$

$$\hat{v}_{\beta,1}^+(s) = \frac{\omega_p}{s + \omega_p} \left( v_{\beta}(s) - \sum_{h=2}^n \hat{v}_{\beta,h}^+(s) - \sum_{h=1}^n \hat{v}_{\beta,h}^-(s) \right) + \frac{\hat{\omega}}{s + \omega_p} \hat{v}_{\alpha,1}^+(s) \quad (30)$$

$$\begin{bmatrix} \hat{v}_{\alpha,1}^+(s) \\ \hat{v}_{\beta,1}^+(s) \end{bmatrix} = \underbrace{\frac{\omega_p}{(s + \omega_p)^2 + \hat{\omega}^2} \begin{bmatrix} s + \omega_p & -\hat{\omega} \\ \hat{\omega} & s + \omega_p \end{bmatrix}}_{[H(s)]} \times \begin{bmatrix} v_{\alpha}(s) - \sum_{h=2}^n \hat{v}_{\alpha,h}^+(s) - \sum_{h=1}^n \hat{v}_{\alpha,h}^-(s) \\ v_{\beta}(s) - \sum_{h=2}^n \hat{v}_{\beta,h}^+(s) - \sum_{h=1}^n \hat{v}_{\beta,h}^-(s) \end{bmatrix} \quad (31)$$

$$\begin{bmatrix} \hat{v}_{\alpha,1}^-(s) \\ \hat{v}_{\beta,1}^-(s) \end{bmatrix} = \underbrace{\frac{\omega_p}{(s + \omega_p)^2 + \hat{\omega}^2} \begin{bmatrix} s + \omega_p & \hat{\omega} \\ -\hat{\omega} & s + \omega_p \end{bmatrix}}_{[H(s)]^t} \times \begin{bmatrix} v_{\alpha}(s) - \sum_{h=1}^n \hat{v}_{\alpha,h}^+(s) - \sum_{h=2}^n \hat{v}_{\alpha,h}^-(s) \\ v_{\beta}(s) - \sum_{h=1}^n \hat{v}_{\beta,h}^+(s) - \sum_{h=2}^n \hat{v}_{\beta,h}^-(s) \end{bmatrix} \quad (32)$$

Comparing (31) and (32) with (21) and (22), respectively, the following can be concluded.

- 1) The TM system of the MCCF structure (tuned at  $\pm\omega$ ) and the MRF structure are two equivalent systems. Thus, the same linearized model as that of the MRF-PLL (see Fig. 6) can be used for the MCCF-PLL (TM).
- 2) In the case of using the MM system, again, the same linearized model as that of the MRF-PLL can be used for the MCCF-PLL. The only difference is the disturbance input to the linearized model, which is determined according to the number of modules used in the MCCF structure. For example, in the case of using four modules tuned at  $\pm\omega$ ,  $-5\omega$ , and  $+7\omega$ , the disturbance input to the linearized model becomes

$$\tilde{v}_q = L[f(12\omega, 18\omega, \dots)] \quad (33)$$

### III. PARAMETERS DESIGN GUIDELINES

In this section, a systematic design procedure to fine tune the parameters of the PLLs under study is presented. Since all PLLs have identical small-signal models, with the only difference in the disturbance input to the model, the design procedure presented in the following sections is valid for all PLLs, unless otherwise stated. The stability margin, the transient response,

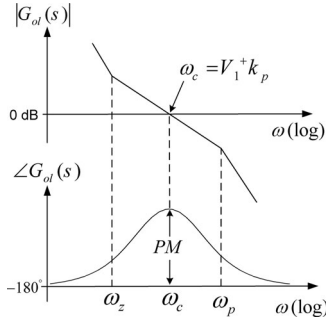


Fig. 10. Logarithmic plot of the open-loop transfer function.

and the disturbance rejection capability are the key factors that are considered in the design procedure.

### A. Stability

The main focus in this section is to establish a criterion based on the extended symmetrical optimum method [39], [40], so that the maximum possible phase margin is achieved. This method is a standard procedure for designing type-2 control systems with an open-loop transfer function as

$$G_{ol}(s) = k \frac{(s + \omega_z)}{s^2(s + \omega_p)}. \quad (34)$$

The main idea of this approach is that to achieve the maximum possible phase margin, the crossover frequency should be at the geometric mean of corner frequencies [40], [41]. Application of this method to the PLL-based frequency synthesizers can be found in [42].

Based on Fig. 3 (or Fig. 6), supposing  $\omega_z = k_i/k_p$ , the open-loop transfer function of the PLL can be obtained as

$$G_{ol}(s) = \left. \frac{\hat{\phi}_1^+(s)}{\phi_e(s)} \right|_{\tilde{v}_q(s)=0} = \frac{V_1^+ k_p \omega_p (s + \omega_z)}{s^2 (s + \omega_p)}. \quad (35)$$

Based on (35), the PM can be simply determined as

$$PM = \underbrace{\tan^{-1}(\omega_c/\omega_z)}_{\phi_z} - \underbrace{\tan^{-1}(\omega_c/\omega_p)}_{\phi_p} \quad (36)$$

where  $\omega_c$  is the crossover frequency and is given by

$$\omega_c = V_1^+ k_p \frac{\cos(\phi_p)}{\sin(\phi_z)}. \quad (37)$$

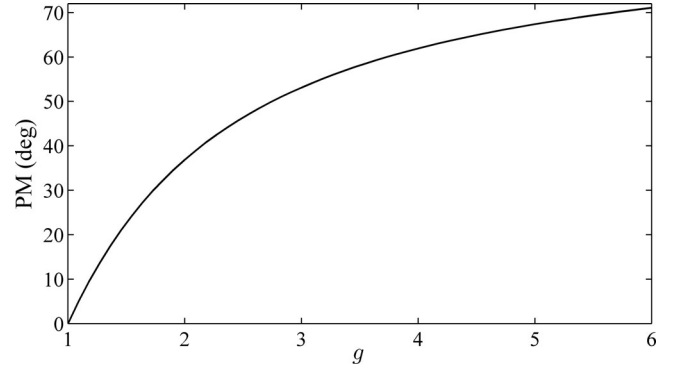
Differentiating (36) with respect to the crossover frequency and equating it to zero, i.e.,  $\partial PM/\partial \omega_c = 0$ , give

$$\omega_c = \sqrt{\omega_z \omega_p}. \quad (38)$$

Replacing (38) into (37) yields

$$\omega_c = V_1^+ k_p \quad (39)$$

meaning that for given values of  $\omega_p$  and  $\omega_z$ , the phase margin is maximum if  $\omega_c = V_1^+ k_p$ . This is graphically illustrated in Fig. 10.


 Fig. 11. Phase margin as a function of  $g$ .

From (38) and (39), and supposing  $\omega_p = g^2 \omega_z$ , where  $g$  is a constant, we obtain

$$\begin{cases} k_p = \omega_c/V_1^+ \\ \omega_z = \omega_c/g \\ \omega_p = g\omega_c. \end{cases} \quad (40)$$

An interesting deduction from (40) is that, in an optimum manner, the number of degrees of freedom is reduced by one. In other words, the PLL parameters (i.e.,  $k_p$ ,  $k_i$ , and  $\omega_p$ ) can be determined by selecting appropriate values for  $g$  and  $\omega_c$ . In the following, we determine the allowable variation range of  $g$  in terms of stability.

Substituting (40) into (36), the PM expression can be rewritten as

$$PM = \tan^{-1} \frac{g^2 - 1}{2g}. \quad (41)$$

Fig. 11 illustrates PM as a function of  $g$ . Usually, a PM within the range of  $30^\circ$  to  $60^\circ$  is recommended [43], which translates to  $1.732 < g < 3.732$ .

### B. Dynamic Response

The main focus in this section is to minimize the PLL settling time in response to the phase and frequency step changes.

By substituting (40) into (35), the open-loop transfer function can be rewritten in the form

$$G_{ol}(s) = \frac{g\omega_c^2 s + \omega_c^3}{s^2(s + g\omega_c)}. \quad (42)$$

The transfer function  $G_{ol}$  describes a type-2 system (i.e., there are two poles at the origin). It means that the PLL follows both phase jump (step input) and frequency jump (ramp input) with zero steady-state error [13].

From Fig. 3 (or Fig. 6), the tracking error transfer function can be obtained as

$$\begin{aligned} G_e(s) &= \left. \frac{\phi_e(s)}{\hat{\phi}_1^+(s)} \right|_{\tilde{v}_q(s)=0} = \frac{1}{1 + G_{ol}(s)} \\ &= \frac{s^2(s + g\omega_c)}{(s + \omega_c)(s^2 + (g-1)\omega_c s + \omega_c^2)}. \end{aligned} \quad (43)$$

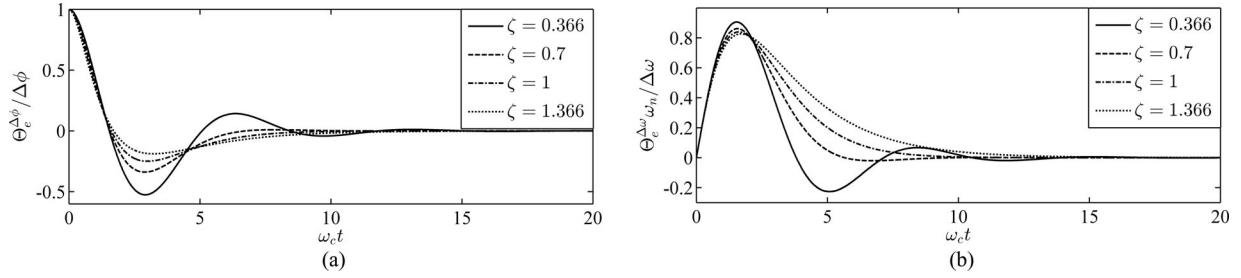


Fig. 12. Transient response for different values of  $\zeta$ . (a) Phase jump. (b) Frequency step.

Assuming  $g = 2\zeta + 1$ , (43) can be rewritten in the form

$$G_e(s) = \frac{s^2(s + (2\zeta + 1)\omega_c)}{(s + \omega_c)(s^2 + 2\zeta\omega_c s + \omega_c^2)}. \quad (44)$$

The phase-error Laplace transform in response to a phase jump ( $\Delta\phi$ ) is

$$\Theta_e^{\Delta\phi}(s) = \frac{\Delta\phi}{s} G_e(s) = \frac{s(s + (2\zeta + 1)\omega_c)\Delta\phi}{(s + \omega_c)(s^2 + 2\zeta\omega_c s + \omega_c^2)}. \quad (45)$$

In a similar way, the phase-error Laplace transforms in response to a frequency step change ( $\Delta\omega$ ) is

$$\Theta_e^{\Delta\omega}(s) = \frac{\Delta\omega}{s^2} G_e(s) = \frac{(s + (2\zeta + 1)\omega_c)\Delta\omega}{(s + \omega_c)(s^2 + 2\zeta\omega_c s + \omega_c^2)}. \quad (46)$$

Taking the inverse Laplace transform from (45) and (46) gives the time domain descriptions for  $\Theta_e^{\Delta\phi}(t)$  and  $\Theta_e^{\Delta\omega}(t)$ , as expressed in (47) and (48), shown at the bottom of the page, respectively [42].

From (47) and (48), it is obvious that for both phase and frequency steps, and for all values of  $\zeta$  (i.e., underdamped ( $\zeta < 1$ ), critically damped ( $\zeta = 1$ ), and overdamped ( $\zeta > 1$ ) cases), the PLL's transient-response speed is directly related to the crossover frequency  $\omega_c$ . In other words, the higher the crossover frequency  $\omega_c$ , the faster the transient response. However, a high value of  $\omega_c$  degrades the noise/disturbance rejection capability of the PLL. Thus, a satisfactory tradeoff has to be found.

Fig. 12(a) and (b) illustrates the PLL transient response to the phase and frequency step changes, respectively, for different

values of  $\zeta$ . For both plots, the horizontal axis is the normalized time  $\omega_c t$ , and the vertical axis is the normalized phase error. The vertical axes normalizing factors are  $1/\Delta\phi$  and  $\omega_c/\Delta\omega$  for the case of phase jump and frequency step, respectively. As can be seen, there is a tradeoff between the overshoot and the settling time. A small value for  $\zeta$  makes the PLL transient response fast but oscillatory. On the contrary, a high value for  $\zeta$  makes the PLL transient response slow with a reduced overshoot. Thus, to achieve a fast transient response with an acceptable overshoot,  $\zeta$  within the range of 0.6 to 1 is recommended.

Using Bode diagrams, it can be shown simply that for this variation range (i.e.,  $0.6 < \zeta < 1$ ),  $\zeta$  has a little effect on the noise/disturbance rejection ability. Based on this, and what was stated in the previous paragraphs, the design procedure is summarized as follows:

- 1) The value of  $\zeta$  is selected so that a desired performance in terms of the transient response is achieved. The shortest possible settling time is our interest in this paper.
- 2) The value of  $\omega_c$  is selected in accordance with the requirements of the noise/disturbance rejection ability. As discussed before, for the case of the MRF-PLL, the DSOGI-PLL, the MCCF-PLL, and their extended versions, there is an upper limit for  $BW_{OL}$  (and hence the crossover frequency  $\omega_c$ ), the purpose of which is to keep away from the influence zone of the notch filter. Extensive simulation studies show that the maximum allowed value for  $\omega_c$  is between one-fifth and one-fourth of the notch frequency (i.e.,  $2\pi 20$  and  $2\pi 25$  rad/s). To determine this range, the worst case condition, i.e., when the grid frequency has

$$\Theta_e^{\Delta\phi}(t) = \begin{cases} \frac{\Delta\phi}{\zeta - 1} [\zeta e^{-\omega_c t} - e^{-\zeta\omega_c t} \cos(\omega_c t \sqrt{1 - \zeta^2})], & \zeta < 1 \\ \Delta\phi e^{-\omega_c t} (1 + \omega_c t - \omega_c^2 t^2), & \zeta = 1 \\ \frac{\Delta\phi}{\zeta - 1} \left[ \zeta e^{-\omega_c t} - \frac{1}{2} e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_c t} - \frac{1}{2} e^{-(\zeta + \sqrt{\zeta^2 - 1})\omega_c t} \right], & \zeta > 1 \end{cases} \quad (47)$$

$$\Theta_e^{\Delta\omega}(t) = \begin{cases} \frac{\Delta\omega}{(1 - \zeta)\omega_c} [\zeta e^{-\omega_c t} + e^{-\zeta\omega_c t} \{-\zeta \cos(\omega_c t \sqrt{1 - \zeta^2}) + \sqrt{1 - \zeta^2} \sin(\omega_c t \sqrt{1 - \zeta^2})\}], & \zeta < 1 \\ \frac{\Delta\omega}{\omega_c} e^{-\omega_c t} (\omega_c t + \omega_c^2 t^2), & \zeta = 1 \\ \frac{\Delta\omega}{(1 - \zeta)\omega_c} \left[ \zeta e^{-\omega_c t} - \frac{\zeta + \sqrt{\zeta^2 - 1}}{2} e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_c t} - \frac{\zeta - \sqrt{\zeta^2 - 1}}{2} e^{-(\zeta + \sqrt{\zeta^2 - 1})\omega_c t} \right], & \zeta > 1 \end{cases} \quad (48)$$



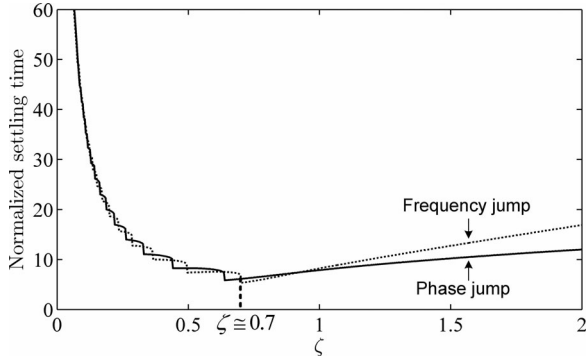


Fig. 13. Normalized simulated settling time as a function of  $\zeta$  for both phase and frequency jumps.

its lowest expected value ( $-15\%$  below the nominal frequency, according to the EN 50160 standard [37]), has been considered. Obviously, for the LSRF-PLL, there is no such a limitation.

Fig. 13 illustrates the normalized simulated settling time of the PLL as a function of  $\zeta$  for both phase jump (solid line) and frequency jump (dotted line). The normalizing factor is the crossover frequency  $\omega_c$ . Clearly, for  $\zeta < 1$ , almost same settling times are observed for both phase and frequency jumps. However, for  $\zeta > 1$ , a longer settling time is observed for the frequency jump. Fortunately, the minimum settling time for both phase and frequency jumps happens approximately at  $\zeta = 0.7$ . Thus, in terms of the settling time,  $\zeta = 0.7$  is optimum. This value of  $\zeta$  also provides a smooth transient response, as clearly shown in Fig. 12.

To make sure that  $\zeta = 0.7$  is also a good choice in terms of stability margin, let us determine the PM for this value of  $\zeta$ . Substituting  $g = 2.4$  (which corresponds to  $\zeta = 0.7$ ) into (41) gives  $\text{PM} = 44.76^\circ$ , which can be interpreted as a perfect stability. Thus, it seems that  $\zeta = 0.7$  is a good choice in terms of both transient response and stability margin.

### C. Disturbance Rejection

The aim of this section is to select the crossover frequency  $\omega_c$ , so that a desired disturbance rejection ability is achieved.

Based on Fig. 3 (or Fig. 6), the disturbance transfer function of the PLL, relating  $\tilde{v}_q(s)$  to  $\hat{\phi}_1^+(s)$ , can be derived as

$$G_d(s) = \left. \frac{\hat{\phi}_1^+(s)}{\tilde{v}_q(s)} \right|_{\phi_1^+(s)=0} = \frac{1}{V_1^+} \frac{g\omega_c^2 s + \omega_c^3}{s^3 + g\omega_c s^2 + g\omega_c^2 s + \omega_c^3}. \quad (49)$$

Fig. 14 displays the Bode magnitude plots of the disturbance transfer function of (49) and the open-loop transfer function of (42) for three different values of  $\omega_c$ , and  $\zeta = 0.7$  ( $g = 2.4$ ), and  $V_1^+ = 1$  pu. As it can be observed, for a given value of  $\omega_c$ , the open-loop and disturbance transfer functions have well-matched amplitudes at disturbance frequencies (i.e.,  $2\omega$ ,  $6\omega$ , ...). Therefore, instead of using the disturbance transfer function  $G_d(s)$ , the open-loop transfer function  $G_{ol}(s)$  can be used to design the crossover frequency  $\omega_c$ .

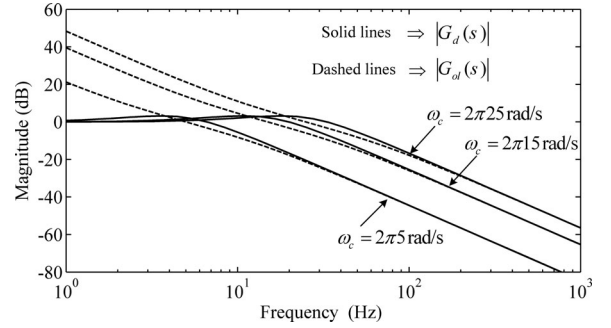


Fig. 14. Bode magnitude plots of the disturbance and open-loop transfer functions for different values of  $\omega_c$ .

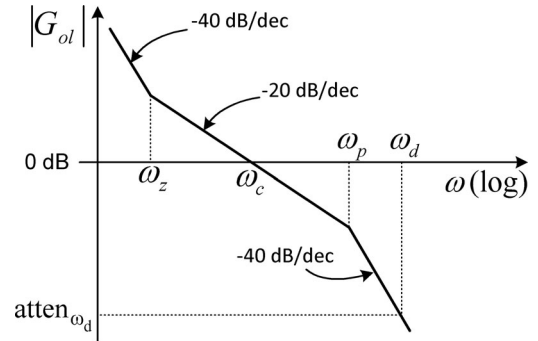


Fig. 15. Logarithmic magnitude plot of the open-loop transfer function.

Let us plot the logarithmic plot of Fig. 10 with more details as presented in Fig. 15, in which  $\omega_d$  is the lowest order disturbance frequency of concern (i.e.,  $2\omega$  for the LSRF-PLL, and  $6\omega$  for the DSOGI-PLL, MRF-PLL, and MCCF-PLL), and  $\text{atten}_{\omega_d} = |G_{ol}(j\omega_d)| \approx |G_d(j\omega_d)|$  is the attenuation provided by the PLLs at this frequency.

From Fig. 15,  $\text{atten}_{\omega_d}$  can be approximated as

$$\begin{aligned} \text{atten}_{\omega_d} = |G_{ol}(j\omega_d)| &\approx -20 \log \frac{\omega_d}{\omega_c} - 20 \log \frac{\omega_d}{\omega_p} \\ &= -20 \log \frac{\omega_d^2}{\omega_p \omega_c}. \end{aligned} \quad (50)$$

Substituting  $\omega_p = g\omega_c$  into (50), and performing some mathematical manipulations, yields

$$\text{atten}_{\omega_d} = -40 \log \left( \frac{\omega_d}{\omega_c \sqrt{g}} \right) \Leftrightarrow \omega_c = \frac{\omega_d}{\sqrt{g}} 10^{\left( \frac{\text{atten}_{\omega_d}}{40} \right)}. \quad (51)$$

From (51), the crossover frequency can be simply determined by selecting an appropriate value for  $\text{atten}_{\omega_d}$ . For the case of the LSRF-PLL,  $\omega_d$  is  $2\omega = 2\pi 100$  rad/s, and  $\text{atten}_{\omega_d}$  is selected to be  $-25$  dB. This selection yields the crossover frequency  $\omega_c$  to be  $2\pi 15.3$  rad/s.

For the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL,  $\omega_d$  is  $6\omega = 2\pi 300$  rad/s. It was mentioned in the previous section that, for these PLLs, the maximum allowed value of  $\omega_c$  is between one-fifth and one-fourth of the notch frequency, i.e.,  $2\pi 20$  and  $2\pi 25$  rad/s. A crossover frequency in the middle of the aforementioned range (i.e.,  $\omega_c = 2\pi 22$  rad/s) gives

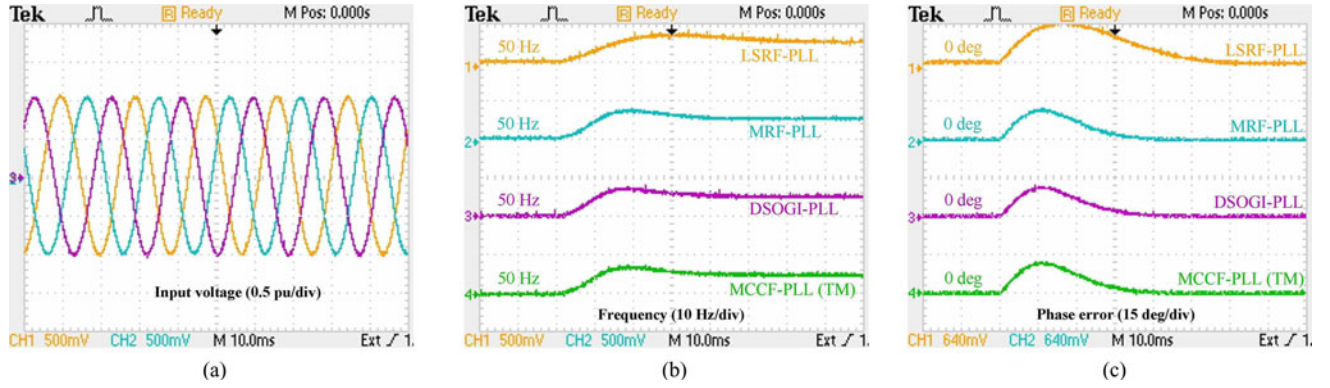


Fig. 16. Experimental results when the input voltage undergoes a frequency step change of 5 Hz. (a) Input voltages. (b) Estimated frequency. (c) Phase error.

TABLE I  
SUMMARY OF EXPERIMENTAL RESULTS

	LSRF-PLL	MRF-PLL	DSOGI-PLL	MCCF-PLL (TM)	Extended MRF-PLL	MSOGI-PLL	MCCF-PLL (MM)
<b>+5Hz frequency step</b>							
Settling time (2% criterion)	≈ 3.1 cycles	≈ 2.1 cycles	≈ 2.2 cycles	≈ 2.1 cycles	≈ 2.1 cycles	≈ 2.2 cycles	≈ 2.1 cycles
Peak phase-error	16.2°	11.9°	11.8°	11.9°	12°	11.8°	12°
Peak frequency deviation	1.7 Hz	2 Hz	1.9 Hz	2 Hz	2 Hz	1.9 Hz	2 Hz
<b>+40° phase jump</b>							
Settling time (2% criterion)	≈ 3.1 cycles	≈ 2.1 cycles	≈ 2.2 cycles	≈ 2.1 cycles	≈ 2.1 cycles	≈ 2.2 cycles	≈ 2.1 cycles
Peak phase-error	13.5°	16.3°	14.9°	16.2°	16.6°	14.7°	16.5°
Peak frequency deviation	8.5 Hz	13.9 Hz	14.2 Hz	13.9 Hz	14 Hz	14.4 Hz	14 Hz
<b>Unbalance and distortion</b>							
steady-state peak-to-peak phase-error	0.7°	0.15°	0.15°	0.15°	≈ 0°	≈ 0°	≈ 0°
steady-state peak-to-peak frequency error	1.5 Hz	0.8 Hz	0.8 Hz	0.8 Hz	≈ 0 Hz	≈ 0 Hz	≈ 0 Hz
<b>Implementation details</b>							
State variables / integrations	2	4	4	4	8	12	8
Multiplications / scaling operations	9	23	15	19	45	31	33
Additions / subtractions	7	19	11	17	43	31	37

$\text{atten}_{\omega_d} = -37.78$  dB, which is quite adequate for most applications. Thus, for these PLLs, the crossover frequency  $\omega_c$  is set to  $2\pi 22$  rad/s.

Based on the designed value for  $\omega_c$  and  $\zeta(g)$ , the parameters of the PLLs can be calculated as follows:

$$\text{LSRF-PLL} \Rightarrow \begin{cases} k_p = \omega_c / V_1^+ = 96.13 \\ k_i = k_p \omega_c = \omega_c^2 / (gV_1^+) = 3850 \\ \omega_p = g\omega_c = 2\pi 36.72 \text{ rad/s} \end{cases} \quad (52)$$

$$\text{Other PLLs} \Rightarrow \begin{cases} k_p = \omega_c / V_1^+ = 138.23 \\ k_i = k_p \omega_c = \omega_c^2 / (gV_1^+) = 7961 \\ \omega_p = g\omega_c = 2\pi 52.8 \text{ rad/s} \\ k = 2\omega_p / \omega_{ff} = 2.11. \end{cases} \quad (53)$$

Notice that to calculate the parameters,  $V_1^+$  was assumed to be unity. This assumption can be simply realized by dividing the signal containing the phase-error information (i.e.,  $\hat{v}_{g,1}^+$ ) by an estimation of the input voltage amplitude prior to being fed into the LF.

#### IV. EVALUATION RESULTS

To verify the suggested design guidelines, the experimental results for the PLLs under study have been presented in this

section. A TMS320F28335 floating point 150-MHz digital signal controller from Texas Instruments has been employed to implement the PLLs. The sampling frequency has been fixed to 10 kHz, and the nominal frequency has been set to 50 Hz. An arbitrary waveform generator based on a DSP card has been utilized to obtain the three-phase voltages. In experiments, to implement the extended MRF-PLL, the MSOGI-PLL, and the MCCF-PLL (MM), in addition to the fundamental negative-sequence component, the 5th<sup>-</sup> and 7th<sup>+</sup> harmonic components have been also included in their filtering structures.

##### A. Frequency Variation

Fig. 16 illustrates the experimental results when the input voltage undergoes a frequency step change from 50 to 55 Hz. As expected, for the case of the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL (TM), almost the same results are achieved. For these PLLs, the estimated frequency is locked to the real one in about two cycles of the fundamental frequency. Very similar results are also obtained with the extended MRF-PLL, the MSOGI-PLL, and the MCCF-PLL (MM) (here not illustrated, but summarized in Table I). For the LSRF-PLL, however, the lockup process takes more time (about three cycles), as shown in Fig. 16.

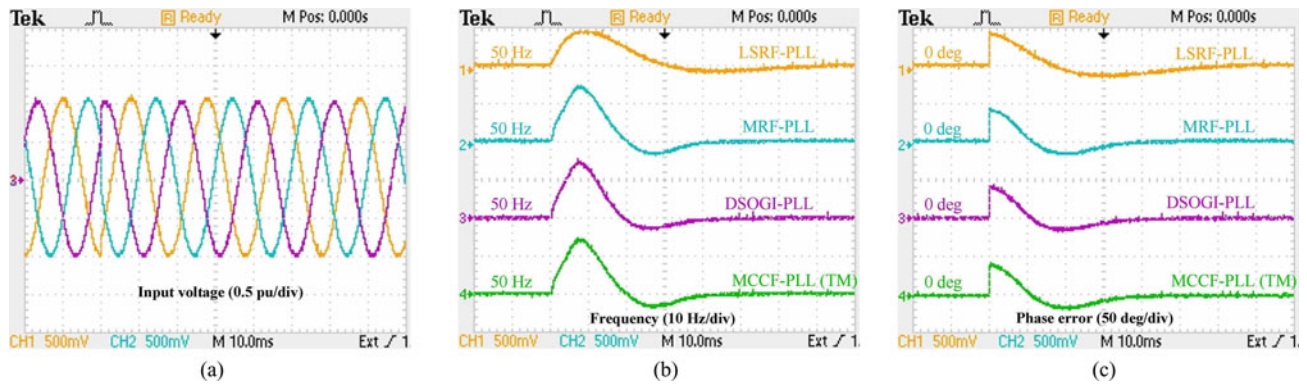


Fig. 17. Experimental results in response to a utility phase jump of  $40^\circ$ . (a) Input voltages. (b) Estimated frequency. (c) Phase error.

TABLE II  
SUMMARY OF ANALYTICALLY PREDICTED RESULTS

	LSRF-PLL	Other PLLs
<b>+5Hz frequency step</b>		
Settling time (2% criterion)	63 ms (3.15 cycles)	44 ms (2.2 cycles)
Peak phase-error	16.03°	11.22°
Peak frequency deviation	1.72 Hz	1.7 Hz
<b>+40° phase jump</b>		
Settling time (2% criterion)	62 ms (3.1 cycles)	43 ms (2.15 cycles)
Peak phase-error	13.54°	13.53°
Peak frequency deviation	8.7 Hz	12.42 Hz

### B. Phase Jump

Fig. 17 illustrates the experimental results in response to a utility phase jump of  $40^\circ$ . Again, a similar performance can be observed for the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL (TM). For these PLLs, the phase-error decays to zero in about two cycles, while for the LSRF-PLL, it lags about three cycles.

To confirm the accuracy of the theoretical analysis, the responses of the derived small-signal model for the PLLs are evaluated to the same test cases as the experiments (i.e., phase jump of  $40^\circ$ , and frequency step change of 5 Hz). These results are summarized in Table II. By comparing the results of Table II with the experimental results summary (listed in Table I), one can see that there is a satisfactory agreement between the analytically predicted and the experimentally measured results.

### C. Unbalanced and Distorted Grid Voltages

In the following, the performance of the PLLs are evaluated when the input voltage is unbalanced and harmonically distorted ( $\vec{V}_1^+ = 1\angle 0^\circ$ ,  $\vec{V}_1^- = 0.1\angle 0^\circ$ ,  $\vec{V}_5^- = 0.1\angle 90^\circ$ , and  $\vec{V}_7^+ = 0.05\angle 0^\circ$ ). In this test, the grid frequency is fixed at 50 Hz.

Fig. 18 illustrates the experimental results in this condition. It can be seen that for the case of the LSRF-PLL, there are relatively large steady-state oscillations in the estimated frequency and phase error, while for the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL (TM), these oscillations are smaller, thanks to the compensation of the fundamental negative-sequence component. The steady-state oscillations are completely eliminated

with the extended MRF-PLL, the MSOGI-PLL, and the MCCF-PLL (MM), as shown in Fig. 18(d) and (e). More detailed information can be found in Table I.

### D. Computational Load

The last row of Table I provides a comparison in terms of the complexity of the implementation among the studied PLLs. In these results, the mathematical operations and the state variables required for the implementation of the LF and VCO are not included, since they are the same for all the PLLs.

## V. CONCLUSION

An in-depth study of the dynamics of the advanced SRF-PLLs, such as the MRF-PLL, the DSOGI-PLL, and the MCCF-PLL, and also their extended versions (which are suitable for highly distorted grid conditions), has been presented in this paper. Through a detailed mathematical analysis, it was shown that all the aforementioned PLLs have identical small-signal models, with the only difference in the disturbance input to the model. As a consequence, a same design method can be employed to tune their parameters. A systematic design procedure to fine tune the PLLs parameters was proposed afterward, which guarantees a fast and smooth transient response, a high disturbance rejection capability, and a robust performance.

## APPENDIX

### NOTCH-FILTER-LIKE BEHAVIOR OF THE MRF STRUCTURE

Here, it is proved that in the MRF structure, subtracting the estimated fundamental negative-sequence components (i.e.,  $\hat{v}_{abc,1}^-$ ) from the input voltages (i.e.,  $v_{abc}$ ) is equivalent to passing the input voltages through a sort of notch filter tuned at the fundamental frequency of negative sequence.

Multiplying both sides of (21) by  $[H(s)]^{-1}$  gives

$$\begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} - \begin{bmatrix} \hat{v}_{\alpha,1}^-(s) \\ \hat{v}_{\beta,1}^-(s) \end{bmatrix} = [H(s)]^{-1} \begin{bmatrix} \hat{v}_{\alpha,1}^+(s) \\ \hat{v}_{\beta,1}^+(s) \end{bmatrix}. \quad (54)$$



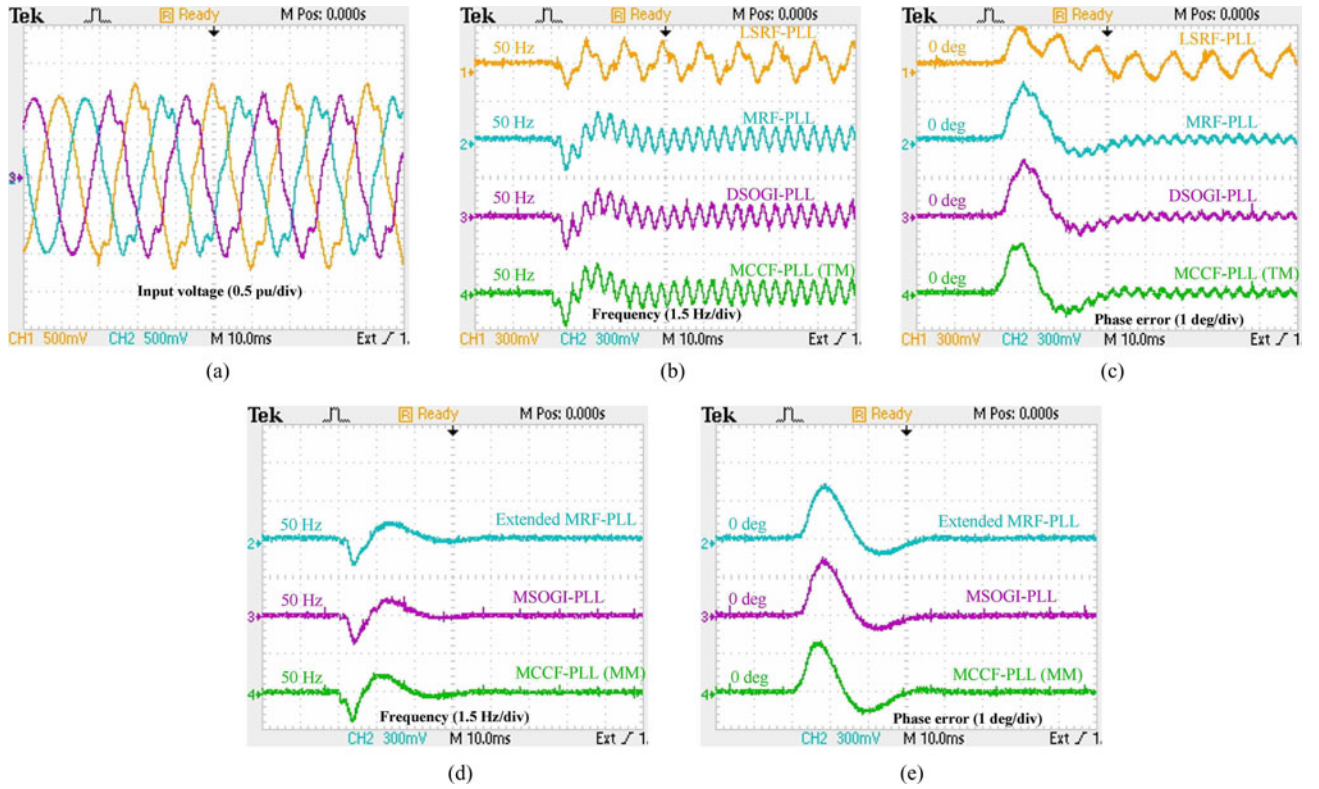


Fig. 18. Experimental results under unbalanced and distorted grid conditions. (a) Input voltages. (b) and (d) Estimated frequency. (c) and (e) Phase error.

Substituting (26) into (54), and performing some simple mathematical manipulations, yields

$$\begin{bmatrix} v_\alpha(s) - \hat{v}_{\alpha,1}^-(s) \\ v_\beta(s) - \hat{v}_{\beta,1}^-(s) \end{bmatrix} = \frac{1}{s^2 + 2\omega_p s + \hat{\omega}^2} \times \begin{bmatrix} s^2 + \omega_p s + \hat{\omega}^2 & -\omega_p \hat{\omega} \\ \omega_p \hat{\omega} & s^2 + \omega_p s + \hat{\omega}^2 \end{bmatrix} \begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix}. \quad (55)$$

Substituting  $s = j\omega$  into (55), and considering that  $v_\alpha$  and  $v_\beta$  keep the following steady-state relationship on the frequency domain [41]

$$v_\beta(j\omega) = -jv_\alpha(j\omega) \quad (56)$$

we can rewrite (55) as follows:

$$\begin{bmatrix} v_\alpha(j\omega) - \hat{v}_{\alpha,1}^-(j\omega) \\ v_\beta(j\omega) - \hat{v}_{\beta,1}^-(j\omega) \end{bmatrix} = \underbrace{\frac{\hat{\omega}^2 - \omega^2 + j\omega_p(\omega + \hat{\omega})}{\hat{\omega}^2 - \omega^2 + j2\omega_p\omega}}_{N(j\omega)} \begin{bmatrix} v_\alpha(j\omega) \\ v_\beta(j\omega) \end{bmatrix}. \quad (57)$$

Multiplying both sides of (57) by  $[T_{\alpha\beta}]^{-1}$  (Clark's inverse transformation) gives

$$\begin{bmatrix} v_a(j\omega) - \hat{v}_{a,1}^-(j\omega) \\ v_b(j\omega) - \hat{v}_{b,1}^-(j\omega) \\ v_c(j\omega) - \hat{v}_{c,1}^-(j\omega) \end{bmatrix} = N(j\omega) \begin{bmatrix} v_a(j\omega) \\ v_b(j\omega) \\ v_c(j\omega) \end{bmatrix}. \quad (58)$$

Fig. 19 illustrates the frequency response of  $N(j\omega)$  for three different values of  $\omega_p$ , and for  $\hat{\omega} = 2\pi 50$  rad/s. Notice that the

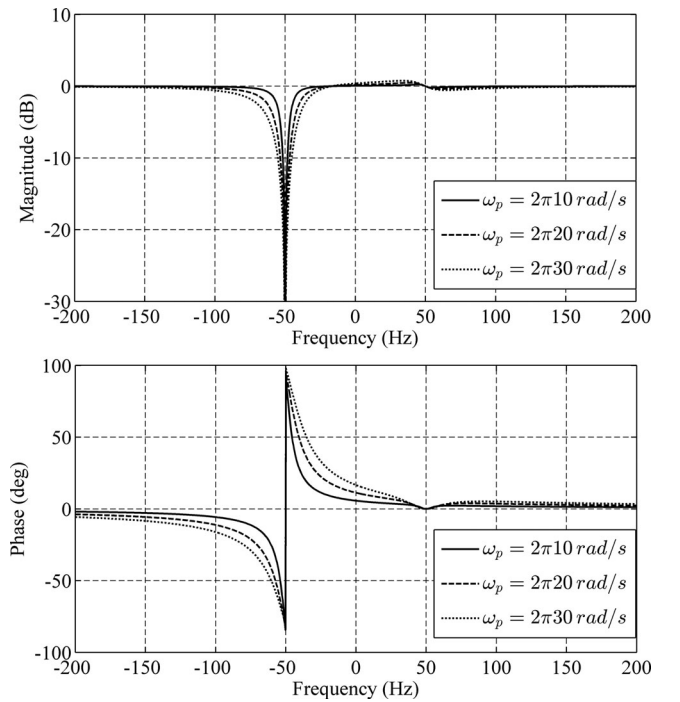


Fig. 19. Frequency response of  $N(j\omega)$ .

response to positive frequencies is the response to the positive sequence components of input voltage, and the response to negative frequencies is the response to the negative-sequence components of the input voltage [44]. As can be seen,  $N(j\omega)$



provides a notch at the fundamental frequency of the negative sequence and has no effect at the fundamental frequency of the positive sequence.

#### ACKNOWLEDGMENT

The authors would like to thank Prof. M. Karimi-Ghartemani from the Mississippi State University for discussions and critical reading of the manuscript.

#### REFERENCES

- [1] O. Vainio and S. J. Ovaska, "Noise reduction in zero crossing detection by predictive digital filtering," *IEEE Trans. Ind. Electron.*, vol. 42, no. 1, pp. 58–62, Feb. 1995.
- [2] O. Vainio, S. J. Ovaska, and M. Polla, "Adaptive filtering using multiplicative general parameters for zero-crossing detection," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1340–1342, Dec. 2003.
- [3] J. Svensson, "Synchronisation methods for grid-connected voltage source converters," *IEE Gener., Transmiss. Distrib.*, vol. 148, no. 3, pp. 229–235, May 2001.
- [4] L. L. Lai, C. T. Tse, W. L. Chan, and A. T. P. So, "Real-time frequency and harmonic evaluation using artificial neural networks," *IEEE Trans. Power Del.*, vol. 14, no. 1, pp. 52–59, Jan. 1999.
- [5] M. D. Kusljevic, J. J. Tomic, and L. D. ovanovic, "Frequency estimation of three-phase power system using weighted-least-square algorithm and adaptive FIR filtering," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 2, pp. 322–329, Feb. 2010.
- [6] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, "Power converter line synchronization using a discrete fourier transform (DFT) based on a variable sample rate," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 877–884, Jul. 2005.
- [7] B. Zeng and Z. Teng, "Parameter estimation of power system signals based on cosine self-convolution window with desirable side-lobe behaviors," *IEEE Trans. Power Syst.*, vol. 26, no. 1, pp. 250–257, Jan. 2011.
- [8] D. Yazdani, A. Bakhshai, G. Joos, and M. Mojiri, "A nonlinear adaptive synchronization technique for grid-connected distributed energy sources," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2181–2186, Jul. 2008.
- [9] M. Mojiri, M. Karimi-Ghartemani, and A. Bakhshai, "Estimation of power system frequency using an adaptive notch filter," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2470–2477, Dec. 2007.
- [10] R. Cardoso, R. F. Camargo, H. Pinheiro, and H. A. Grundling, "Kalman filter based synchronisation methods," *IET Gen., Transmiss., Distrib.*, vol. 2, no. 4, pp. 542–555, Jul. 2008.
- [11] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.
- [12] P. Rodriguez, A. Luna, R. S. Munoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu, and F. Blaabjerg, "A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 99–112, Jan. 2012.
- [13] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, Nov./Dec. 2009.
- [14] F. D. Freijedo, A. G. Yepes, O. Lopez, A. Vidal, and J. Doval-Gandoy, "Three-phase PLLs with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 85–97, Jan. 2011.
- [15] F. D. Freijedo, A. G. Yepes, O. Lopez, P. Fernandez-Comesana, and J. Doval-Gandoy, "An optimized implementation of phase locked loops for grid applications," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 9, pp. 3110–3119, Sep. 2011.
- [16] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, 2012, in press.
- [17] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012.
- [18] M. Karimi-Ghartemani, H. Karimi, and M. R. Iravani, "A magnitude/phase-locked loop system based on estimation of frequency and in-phase/quadrature-phase amplitudes," *IEEE Trans. Ind. Electron.*, vol. 51, no. 2, pp. 511–517, Apr. 2004.
- [19] M. Karimi-Ghartemani and M. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power Syst.*, vol. 19, no. 3, pp. 1263–1270, Aug. 2004.
- [20] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.
- [21] H. Awad, J. Svensson, and M. Bollen, "Tuning software phase-locked loop for series-connected converters," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 300–308, Jan. 2005.
- [22] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.
- [23] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008.
- [24] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc. IEEE 37th Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.
- [25] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.
- [26] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067–1080, Apr. 2011.
- [27] F. Liccardo, P. Marino, and G. Raimondo, "Robust and fast three-phase PLL tracking system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 221–231, Jan. 2011.
- [28] Y. F. Wang and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1987–1997, Jul. 2011.
- [29] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous reference frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2718–2731, Jun. 2012.
- [30] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [31] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter PLL for distorted three-phase systems," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 321–330, Jan. 2012.
- [32] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. A. Martinez-Velasco, C. A. Silva, J. Pontt, and J. Rodriguez, "Control strategies based on symmetrical components for grid-connected converters under voltage dips," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2162–2173, Jun. 2009.
- [33] Y. Sozer and D. A. Torrey, "Modeling and control of utility interactive inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2475–2483, Nov. 2009.
- [34] Y. Han, L. Xu, M. M. Khan, G. Yao, L. Zhou, and C. Chen, "A novel synchronization scheme for grid-connected converters by using adaptive linear optimal filter based PLL (ALOF-PLL)," *Simul. Model. Practice Theory*, vol. 17, no. 7, pp. 1299–1345, Aug. 2009.
- [35] I. Etxeberria-Otadui, A. L. D. Heredia, H. Gaztanaga, S. Bacha, and M. Reyero, "A single synchronous frame hybrid (SSFH) multifrequency controller for power active filters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1640–1648, Oct. 2006.
- [36] P. L. Chapman and S. D. Sudhoff, "A multiple reference frame synchronous estimator/regulator," *IEEE Trans. Energy Convers.*, vol. 15, no. 2, pp. 197–202, Jun. 2000.
- [37] *Voltage Characteristics of Electricity Supplied by Public Distribution Systems*. Eur. Standard EN 50160, 2008.
- [38] K. W. Martin, "Complex signal processing is not complex," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 9, pp. 1823–1836, Sep. 2004.
- [39] S. Preitl and R.-E. Precup, "On the algorithmic design of a class of control systems based on providing the symmetry of open-loop Bode plots," *Buletinul Stiintific al U.P.T., Trans. Autom. Control Comput. Sci.*, vol. 41(55), no. 1/2, pp. 47–55, Dec. 1996.

- [40] S. Preitl and R.-E. Precup, "An extension of tuning relations after symmetrical optimum method for PI and PID controller," *Automatica*, vol. 35, no. 10, pp. 1731–1736, Oct. 1999.
- [41] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. New York: IEEE-Wiley, 2011.
- [42] K. Shu and E. Sanchez-Sinencio, *CMOS PLL Synthesizers-Analysis and Design*. New York: Springer, 2005.
- [43] F. M. Gardner, *Phase-Lock Techniques*, 3rd ed. Hoboken, NJ: Wiley, 2005.
- [44] C. A. Busada, S. G. Jorge, A. E. Leon, and J. A. Solsona, "Current controller based on reduced order generalized integrators for distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2898–2909, Jul. 2012.



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