

Enhancing Power Supply Rejection of Low-Voltage Low-Dropout Voltage Regulators Using Bulk Driven PMOS

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Abstract— In this paper a low-voltage low-dropout (LDO) regulator is presented in which the power supply rejection (PSR) is increased by properly driving the bulk of the PMOS pass transistor. A signal proportional to the supply noise is injected to the bulk of the PMOS transistor so that the impact of supply noise on the output voltage coming from other paths is cancelled. Using this technique the PSR of the regulator is increased by approximately 20 dB over a wide frequency range. The supply voltage of the prototype regulator is 1.2 V and the output voltage is 1V. It is designed in 0.18 μm CMOS technology and provides a current of 50 mA to the load.

Keywords- LDO, Pass Transistor, Supply Noise.

I. INTRODUCTION

There is a growing demand for designing low voltage and low power integrated circuits. This is mainly due to the demand for portable and battery operated devices. Meanwhile a voltage regulator is one of the main building blocks of integrated circuits. Designing low-voltage low-power LDO regulators is a challenging task since the low supply voltage degrades the performance of such regulators. In designing a LDO regulator some parameters are more important such as: drop-out voltage, output current, transient response, noise and power supply rejection (PSR). The PSR is the regulator ability to eliminate the supply noise. In many applications LDOs come after a switching converter (switch mode power supplies, SMPS) and a good PSR over a wide frequency range is critical [1].

Typically four main approaches are used to increase the PSR of an LDO. These techniques are: 1- Putting an RC filter between the power supply and the regulator [2], 2- Putting two regulators in series [2], 3- Using an NMOS transistor in series with the PMOS pass transistor of the regulator and using a charge pump [3], 4- Using an NMOS transistor in series with the pass transistor of the regulator and an RC filter to bias the

NMOS [4]. All these techniques reduce the supply noise at the output of the regulator but increase the drop out voltage and consequently increase the power consumption.

In this paper we propose a new technique to increase the PSR while the voltage drop is not increased. The added circuitry is not very complex and consumes very little power.

In section II we discuss general structure of a LDO regulator and various paths that couple power supply noise to the output of the LDO. The proposed technique and simulation results are presented in section III. And the finally, the work is concluded in section IV.

II. LOW DROPOUT REGULATORS

Fig. 1 shows the general structure of a LDO regulator. The regulator is consisted of an opamp, a PMOS as a pass transistor, and a resistive divider circuit for the feedback network and an off-chip output capacitor with its equivalent series resistance (ESR).

In such a regulator the power supply noise can be injected to the output from several paths: 1-The supply noise going through the reference voltage. 2- The supply noise going through the opamp and appearing at the output of the opamp. This noise is then amplified by the pass transistor and appears at the output of the regulator 3- The noise going through the source of the pass transistor and affecting the output of the regulator. 4- The noise appearing at the output of the regulator through the drain-source impedance of the pass transistor.

Fig. 2 shows various paths that couple power supply noise to the output of the LDO.

In order to model the parameters affecting the PSR we consider the block diagram of Fig. 3 for the regulator. In this figure the pass transistor is modeled as an amplifier with a gain of A_2 .

Using Mason's gain theorem one can easily find the following equation for the supply noise appearing at the output of the regulator [5, 6].

$$\frac{V_{o2}}{V_{dd}} = \frac{1-A_{p1}}{A_1\beta} + \frac{1}{g_{mp}r_{dsp}} \cdot \frac{1}{A_1\beta} \quad (1)$$

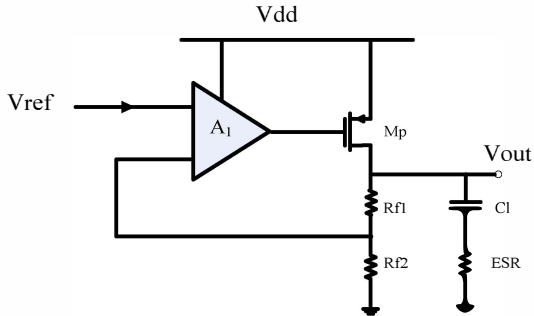


Fig. 1. General structure of an LDO regulator

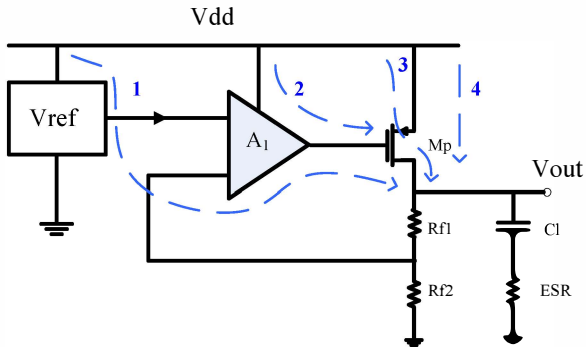


Fig. 2. Input to output noise paths

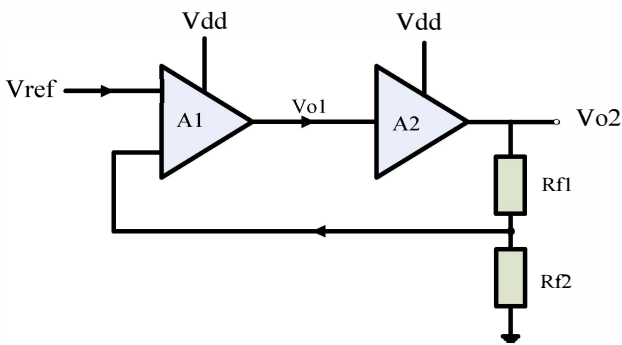


Fig. 3. Block diagram of the regulator with pass transistor modeled as an amplifier with a gain of A2

In the above equation g_{mp} and r_{dsp} are the transconductance and output resistance of the pass transistor respectively. V_{dd} represents the supply noise and V_{o2} is the output voltage of the regulator due to the supply noise. A_{p1} and β are defined as the following.

$$A_{p1} = \frac{V_{o1}}{V_{dd}} \quad (2)$$

$$\beta = \frac{R_{f2}}{R_{f1}+R_{f2}} \quad (3)$$

The above equations show how different parameters can be changed to reduce the impact of supply noise at the output of the regulator. However, there is a limit for each of these parameters and therefore, the PSR can not be increased indefinitely.

III. THE PROPOSED TECHNIQUE

If one can inject a signal to the output of the regulator in such a way to compensate the signals coming from other paths the PSR can be increased. In order to achieve this, we have used the bulk of the PMOS pass transistor to change the source-bulk voltage (V_{SB}) and consequently its drain current. As the threshold voltage of a MOSFET depends on V_{SB} changing the bulk voltage has similar effect as the gate voltage. Fig. 4 illustrates the block diagram of the proposed technique.

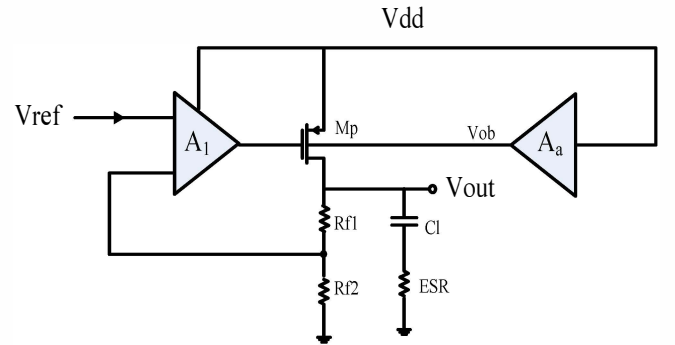


Fig. 4. Block diagram of the proposed technique

The added amplifier with a gain of A_a in the proposed circuit (Fig. 4) amplifies the supply noise and injects a signal to the bulk of the pass transistor. This causes the current of the pass transistor to change according to the supply noise. If the gain of this amplifier is chosen properly, the injected signal reduces the supply noise at the output of the regulator. It can be easily shown that in the proposed regulator, equation (1) is modified to the following equation.

$$\frac{V_{o2}}{V_{dd}} = \frac{A_{p2}+A_{p1}A_2+A_C}{1+A_1A_2\beta} = \frac{1-A_{p1}}{A_1\beta} + \frac{1}{g_{mp}r_{dsp}} \cdot \frac{1}{A_1\beta} + A_C \quad (4)$$

where:

$$A_c = A_a \cdot A_b, \quad A_b = \frac{V_{o2}}{V_{ob}} = \frac{V_{out}}{V_{ob}}, \quad A_a = \frac{V_{ob}}{V_{dd}} \quad (5)$$

According to the above equations A_a can be adjusted to minimize the impact of the supply noise at the output of the regulator. Table I shows the improvement of PSR for different values of A_a for a prototype regulator designed in the 0.18 μm CMOS technology and simulated by HSPICE. In this simulation an ideal amplifier is used for the auxiliary amplifier (A_a). According to this table there is an optimum gain for which the PSR is maximum.

Table I. . Improvement of PSR for different values of A_a at 200KHZ

A_a	4.22	5.11	5.66
PSR improvement (dB)	2.28	23.5	16.47

Fig. 6 shows the schematic of the LDO regulator with the proposed PSR enhancement techniques. The regulator is designed to deliver a maximum current of 50 mA. The supply voltage is 1.2 V and the output voltage is 1V.

As can be seen in this figure, the supply noise is amplified by transistors M_{1b} and M_{2b} and appears at the bulk of the pass transistor of the regulator. Fig. 5 compares the PSR of the regulator with and without the proposed technique at different frequencies and at different process corners. In order to examine the impact of process variations on the effectiveness of the proposed technique, the circuit of Fig. 6 is simulated at different process corners and the improvement of PSR is obtained. The results are shown in Table II.

Table II. Improvement of PSR at different process corners

corner	Fs	sf	ff	ss
PSR improvement (dB)	17	16.58	20.6	16.13

Clearly, even at extreme cases an improvement of more than 16 dB can be obtained.(The circuit is simulated at ss +90 and ff -40 corners and also improvement of PSR is obtained). Note that this technique does not increase the drop-out voltage and the added circuitry is relatively simple. The price of using this technique is the extra power consumption of the auxiliary amplifier. However, this amplifier is not power hungry and the extra power is negligible compared to the nominal as well as the standby power of the regulator.

Table III summarizes and compares the performance of the proposed LDO with the regulator provided in [5, 7, 8].

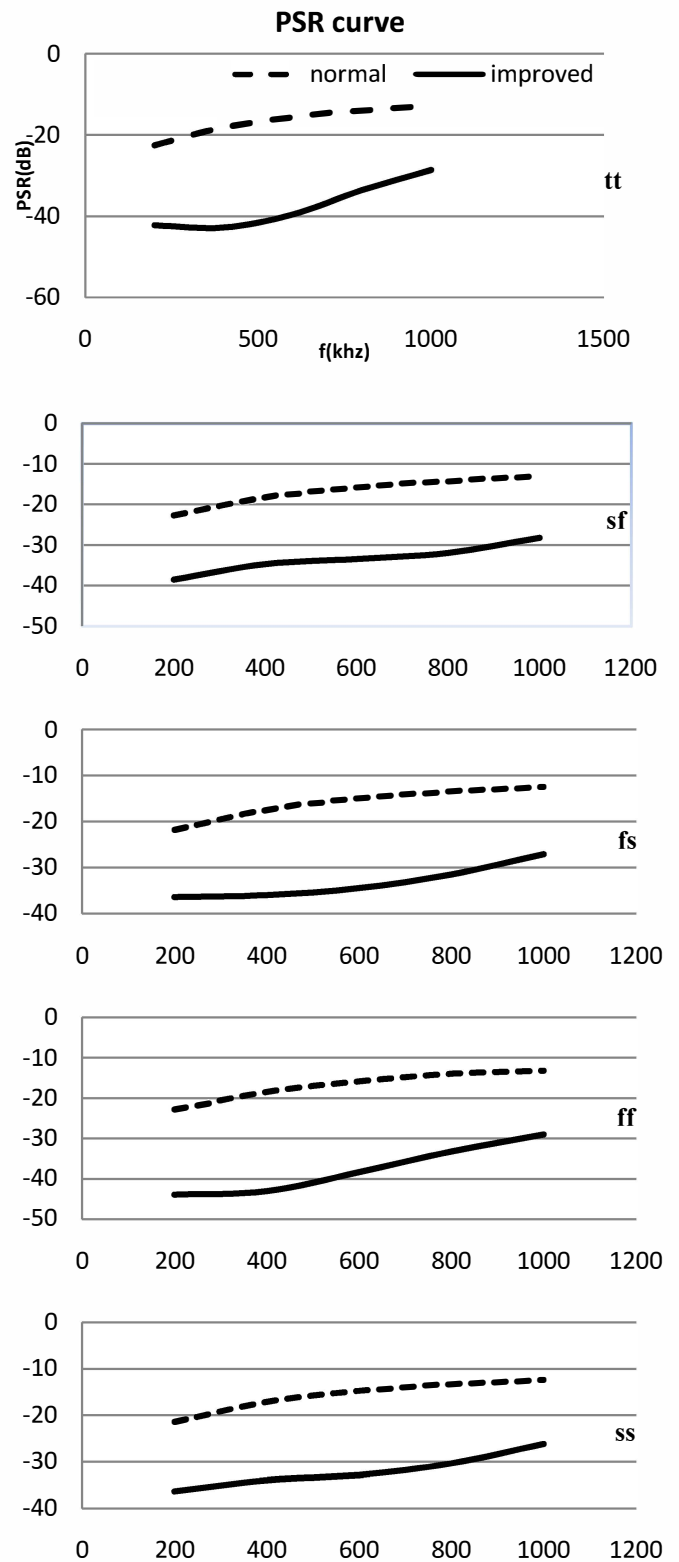


Fig. 5. PSR of the regulator versus frequency with (solid curve) and without (dashed curve) the proposed technique

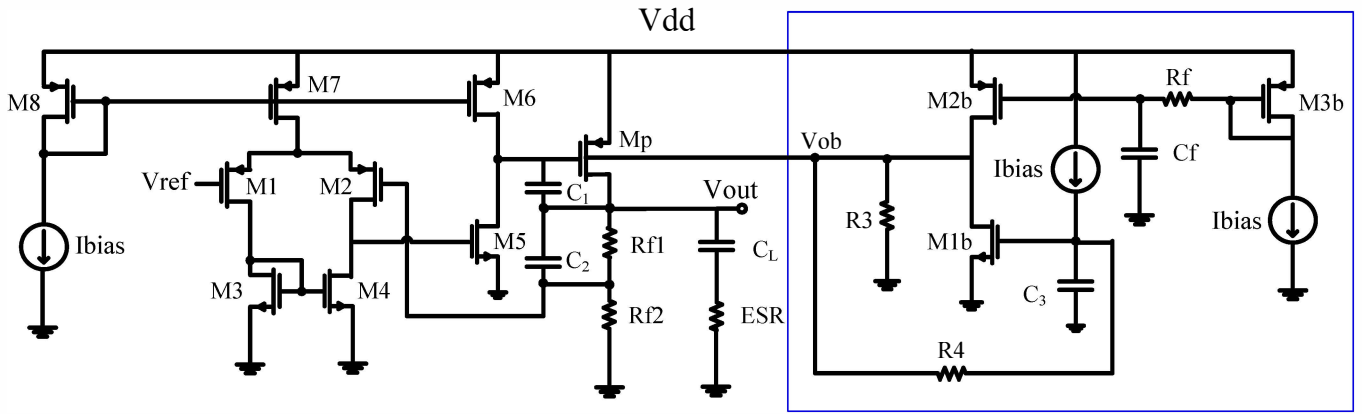


Fig. 6. Schematic of the LDO regulator with the proposed PSR enhancement techniques

Table III. performance summary and comparison

	[5]	[7]	[8]	This work
year	2005	2008	2009	
process	0.35 μ m	0.25 μ m	0.6 μ m	0.18 μ m
$V_{in}(v)$	3.1	2	2	1.2
$V_{out}(v)$	2.8	1.5	1.8	1
I_{o-max}	100mA	50mA	150mA	50mA
PSR	15dB improvement			20dB improvement
			-39.7dB @100kHz	-42.16dB @100kHz
		>25dB @200kHz		--42.27dB @200kHz

IV. CONCLUSION

A new technique for increasing the PSR of a LDO regulator is presented in this paper. The proposed technique uses the bulk of the PMOS pass transistor to inject a properly amplified version of the supply noise to the output node in order to decrease the impact of supply noise coming from other paths. This technique does not increase the drop-out voltage and the added circuitry is relatively simple. Although this technique can not fully eliminate the supply noise at the output but it is very effective in increasing the PSR even at different process corners.

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