

Comparison of RCMV-PWM Methods for Photovoltaic Systems with Deadtime Effect Consideration

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Abstract- In photovoltaic (PV) grid-connected energy conversion systems with no galvanic isolation, PV module parasitic capacitance introduces ground leakage current (common mode current (CMC)) which its amplitude depends on converter topology and pulsewidth modulation (PWM) technique. This paper analyzes and compares the performance characteristic of conventional PWM method, space vector PWM (SVPWM) and reduced common mode voltage (RCMV) PWM methods, AZSPWM, NSPWM and RSPWM. The number of switching per periods, voltage linearity, CMC, CMV, harmonic distortion factor (HDF), DC-Link ripple current of each modulation methods are thoroughly investigated by analytical methods and computer simulation. The main objective of this paper is to investigate optimal RCMV PWM methods with considering deadtime effect. This paper aids design engineer in selection of RCMV methods with respect to their applications.

Keywords- Photovoltaic; Pulsewidth modulation (PWM) technique; Common mode voltage (CMV); Common mode current (CMC).

I. INTRODUCTION

Photovoltaic (PV) energy conversion systems are used widely in the world [1-2]. Because of constant AC power on the output, three phase systems are preferable than single phase systems [1]. Most of the topologies for PV systems have a transformer which used in line or high frequency. Line frequency

transformers increase the size and weight. On the other hand, high frequency transformers decrease the efficiency and make the system more complex [1-4]. Due to the above reasons, it is better to eliminate transformer. Connecting a PV array to the grid without galvanic isolation increases the leakage current through parasitic capacitance of the PV array. This current results in oscillation of potential between the PV array and ground, distortion of grid current, losses in system, safety problems, etc [1],[2],[4]. The parasitic capacitance between PV panel and ground as shown in Fig.1 is estimated at 220nF/kw_p. This value depends on several factors, such as PV panel, frame structure, weather condition, etc [5]. This paper investigates the performance characteristics of three phase voltage source PWM converter with the photovoltaic grid-connected energy conversion system. Conventional PWM method, space vector PWM (SVPWM) and reduced common mode voltage (RCMV) methods, active zero state PWM (AZSPWM), near state PWM (NSPWM), remote state PWM (RSPWM) are considered [6-8]. These methods are compared by means of several indexes as follow: number of switching per period, maximum output voltage amplitude (voltage linearity), CMC, CMV, harmonic distortion factor (HDF), DC-Link ripple current. Finally we focus on dead time effect for each method. This paper makes the good reference for the design engineer in selection of best PWM method for their applications. In section (II), we introduce CMV and discuss about mentioned PWM methods and their switching pattern for grid-connected

converter. In section (III), comparison indexes are introduced and calculated. Then we discuss about the characteristics of each PWM method and compare them through introduced indexes. In section (IV), we speak about dead time effect and its effect on CMV and select the optimal PWM method with respect to deadtime effect.

II. GRID-CONNECTED CONVERTER

A. Common mode voltage (CMV)

In case of photovoltaic energy conversion systems, CMV is defined as the potential between the Voltage source neutral point(n) with respect to the central DC bus of grid-connected converter(Fig.1)[5],[7],[8]. It can be expressed as follow

$$V_{CM} = V_{aN} + V_{bN} + V_{cN} / 3 \quad (1)$$

B. pulsewidth modulation techniques

The space vector PWM (SVPWM) is generally used to control the output voltage of three phase converters. Transferring three phase voltage to the two phase(dq plan), there are eight possible switching states, comprised of six active vectors ($V_1, V_2, V_3, V_4, V_5, V_6$) and two zero vectors(V_0, V_7) as depicted in Fig.2. Each switching state with their corresponding CMV has been illustrated in TABLE.I. In SVPWM, in each sector two adjacent active vectors with zero vectors are used to produce reference voltage vector, in average value. Switching pattern with corresponding CMV for sector (I) are shown in Fig.3 (a). As shown in Fig.3 (a), the common mode voltage pulsation is high. For example in sector (I), where V_0, V_1, V_2, V_7 vectors are used to produce reference voltage, the CMV have four values: $0, V_{PN}/3, 2 * V_{PN}/3, V_{PN}$. Various reduced common mode voltage pulsewidth modulation (RCMV-PWM) techniques have been presented. In all of these modulation techniques, for decreasing pulsation of CMV, zero vectors are replaced by set of active vectors.

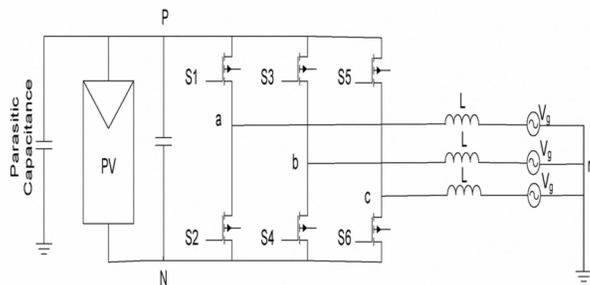


Figure 1. Transformerless grid connected PV system

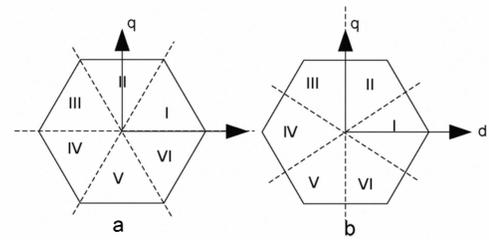


Figure 2. Space vectors in the output of a three-phase inverter:

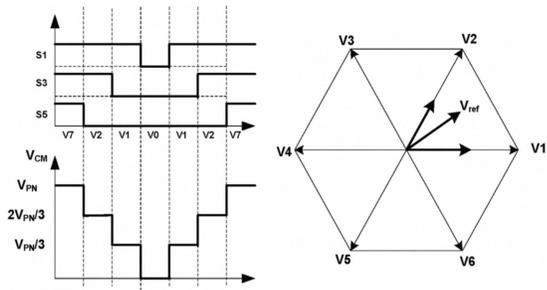
(a).SVPWM, AZSPWM, RSPWM .(b).NSPWM

Active zero state PWM (AZSPWM) uses two adjacent active vectors in each sector like SVPWM. Instead of zero vectors, this method uses two opposing vectors with equal time to effectively create a zero vector. These two opposing vectors are selected with respect to the reference voltage vector position as illustrated for section (I) in Fig.3 (b). In this method CMV pulsation is high but with less amplitude than SVPWM. AZSPWM1 always switch between adjacent vectors over 60 span on dq plan. Unlike AZSPWM1, AZSPWM2 switch between two active vectors which are 120° shifted phase on dq plan. Although CMV pulsation is less than AZSPWM but as will be illustrated in section (IV), it has a CMV spike which increases the CMC. AZSPWM1 switching pattern is illustrated in TABLE.I and the CMV is depicted in Fig.3 (b). Another RCMV-PWM method is near state PWM (NSPWM).This method uses the group of three active vectors to produce desired voltage, two classical active vectors like SVPWM and nearest neighbor active vector for the third active vector. In this method, active vectors which are used to synthesize desired voltage change every 60 on dq plan. A simplified illustration of NSPWM and its switching pattern and CMV are depicted in Fig.4 (a).

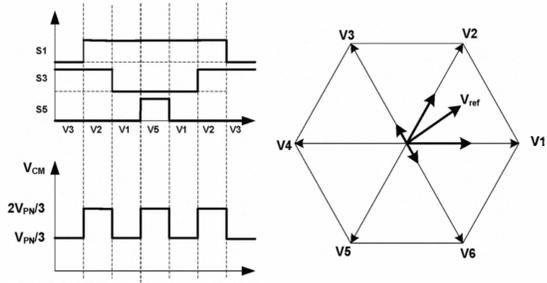
Remote state PWM (RSPWM) uses vectors with the same CMV like V_1, V_2, V_3 or V_2, V_4, V_6 . RSPWM can be grouped in two types [6]: RSPWM1 and RSPWM2. RSPWM1 utilizes only one vector group with fixed sequence to produce desired

TABLE.I

vector	S_a	S_b	S_c	V_{CM}
V_0	0	0	0	0
V_1	1	0	0	$V_{PN}/3$
V_2	1	1	0	$2 V_{PN}/3$
V_3	0	1	0	$V_{PN}/3$
V_4	0	1	1	$2 V_{PN}/3$
V_5	0	0	1	$V_{PN}/3$
V_6	1	0	1	$2 V_{PN}/3$
V_7	1	1	1	V_{PN}



(a).SVPWM



(b).AZSPWM

Figure3. Switching pattern and CMV of: (a). SVPWM

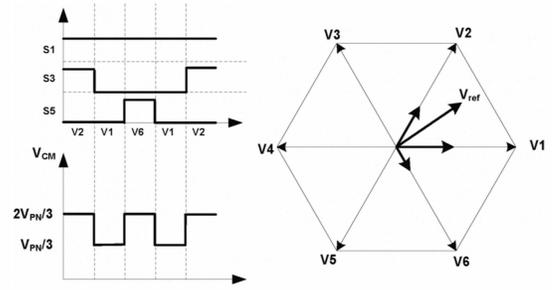
(b).AZSPWM

voltage but RSPWM2 utilizes one vector group with various sequence. The CMV and switching pattern for RSPWM are shown in Fig.4(b). This method has constant CMV which significantly decreases the CMC.

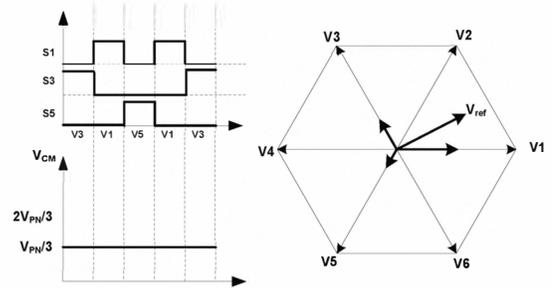
III. COMPARISON INDEXES

A. switching per period

SVPWM switches between two adjacent vectors and two zero vectors. If switching pattern is defined in such a way to reduce harmonic distortion as shown in Fig.3(a), it has one switching in each vector change, totaling six. AZSPWM1 also switches between four adjacent active vectors and has one switching in each vector change totaling six switching per period like SVPWM. NSPWM switches between three active vectors. As shown in Fig.4(a), in each sector, in one leg, its upper switch is on or off for entire period and other leg's switches are switched totaling four switching per period. In RSPWM, in each vector change, simultaneously one of the switches in one leg is turned on and in another leg upper switch is turned off. Consequently in each vector change, two switching occurred totaling ten switching per period. As mentioned above and are shown in TABLE.II, NSPWM has less switching per period.



(a).NSPWM



(b).RSPWM

Figure4. Switching pattern and CMV of(a).NSPWM (b).RSPWM

This reduces the switching losses and improves efficiency. In the other hand, RSPWM has more switching per period which reduces the efficiency.

B. voltage linearity:

In the scalar PWM implementation, where the reference signal is compared with a triangular carrier signal, there is a linear relation between the reference signal and output voltage. The operation range where this linear relation is satisfied is called voltage linearity region. However this linear relation is violated when the peak value of the reference signal is greater than triangular carrier signal peak. Hence this region is called non-

TABLE II.

REGION DEPENDENT PULSE PATTERN OF VARIOUS PWM METHODS

Technique	I	II	III	IV	V	VI
SVPWM	7210127	7230327	7430347	7450547	7650567	7610167
AZSPWM1	3216123	1234321	5432345	3456543	1654561	5612165
AZSPWM2	6213126	4231324	2435342	6453546	4651564	2615162
NSPWM	21612	32123	43234	54345	65456	16561
RSPWM1	31513	31513	31513	31513	31513	31513
RSPWM2	31513	13531	13531	15351	15351	31513

linear (over modulation or under modulation) region. Voltage linearity range is an important characteristic of the PWM methods because it is related to the maximum harmonic free output voltage that can be obtained from a VSI. Thus it is preferable to have a wide voltage linearity range. Modulation index is defined as follow:

$$M_i = V_{1m} / V_{16step} \quad (2)$$

Where $V_{16step} = 2V_{dc}/\pi$ and V_{1m} is the fundamental component magnitude of the reference voltage. The maximum amplitude of phase to neutral voltage is $V_{PN}/\sqrt{3}$ in the linear range where the fundamental component varies linearity with the voltage gain. In Fig.5 voltage linearity of various PWM methods is illustrated. SVPWM and AZSPWM1 can utilize the full inverter voltage hexagon span. They have a voltage linearity range $0 \leq M_i \leq 0.907$ which is defined by the circle tangent to the inverter voltage hexagon. For RSPWM, inverter output voltage has a triangular shape and the voltage linearity range of $0 \leq M_i \leq 0.52$. Unlike all other methods, there is also a lower boundary of the voltage linearity region for NSPWM. In this method the reference voltage vector is generated between the inverter voltage hexagon and the inner hexagon. This corresponds to the voltage linearity range of $0.61 \leq M_i \leq 0.907$.

C. CMC and CMV

To measuring the CMC and CMV, the simulation was done in Matlab/simulink using the three phase setup shown in Fig.1. The grid voltages have value of 110v (rms) and the output inductance is $L=2mH$. The PV array was simulated with the DC voltage

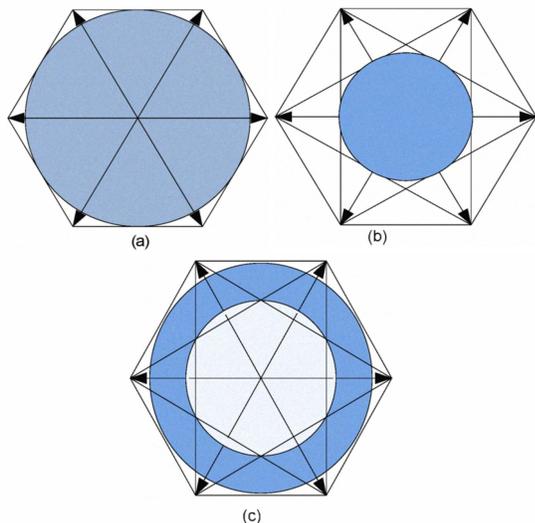


Figure 5. Voltage linearity region of: (a) SVPWM, AZSPWM1. (b) RSPWM. (c) NSPWM

source of 500v. The leakage capacitance between the cells and ground was modeled with a simple capacitance that has a value of 220nF. The ground resistance is 10.75Ω. As shown in Fig.6(a), the CMV and CMC of SVPWM is too high. This indicates that SVPWM is not suitable for transformerless PV applications. The rms value of CMC and CMV are shown in Table III. For AZSPWM, CMC and CMV are shown in Fig.6(b). Although CMC of AZSPWM is lower than SVPWM, but till is too high and it doesn't satisfy international standards. NSPWM also has a lower value of CMC and CMV than AZSPWM and SVPWM which is shown in Fig.7(a). By using the RSPWM, CMV is constant and CMC is eliminated. From point of view of CMC and CMV, RSPWM has the best performance than other modulation techniques. If only the CMC and CMV are important, the RSPWM is the best choice for transformer PV applications.

D. Harmonic distortion factor (HDF)

The inverter output voltage waveform quality can be investigated with aid of space vectors. The normalized harmonic flux vector which is proportional to the output current ripple defined over an arbitrary PWM cycle as follow [5],[9]

$$\lambda_{hn}(M_i, \theta, V_{dc}) = \frac{\pi}{V_{dc} T_s} \int_0^{N T_s} (V_k - V_{ref}) dt \quad (3)$$

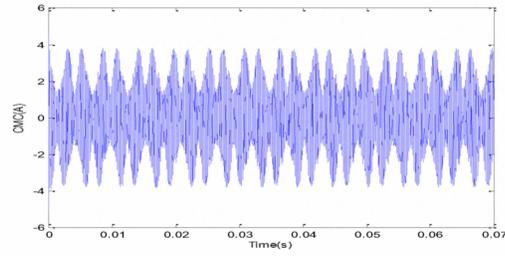
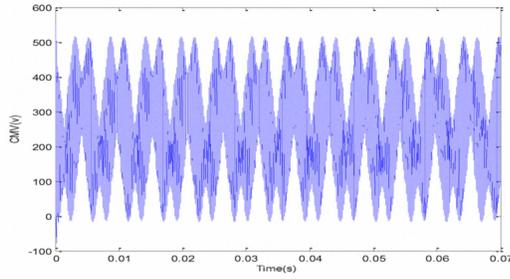
Where $M_i = \pi V_{ref} / 2V_{dc}$, T_s is the period of the modulation, and the N_{th} cycle is of the PWM is calculated. Since each PWM method differs in the utilization of the voltage vectors and their sequence, the harmonic flux vector of each PWM method is unique. The normalized harmonic flux vector rms value over a PWM cycle (duty cycle (d) 0 to 1) is calculated as follow

$$\lambda_{hn-rms}(M_i, \theta) = \sqrt{\int_0^1 \lambda_{hn}^2 dt} \quad (4)$$

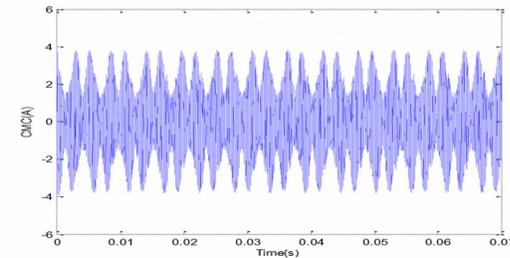
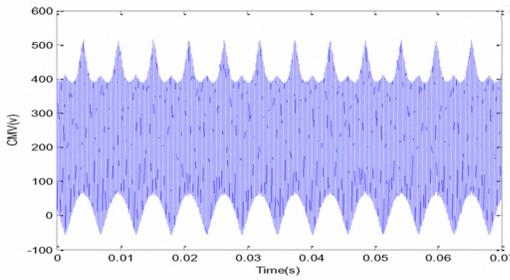
TABLE.III

Performance comparison of various PWM

PWM method	SVPWM	AZSPWM	RSPWM	NSPWM
Switching Per period	6	6	10	4
CMC (rms)	1.798	2	≈0	2.324
THD% (output Voltage)	47.8	95.4	154.3	106.4
Voltage linearity	.91	.91	.52	≥ .68 ≤ .91

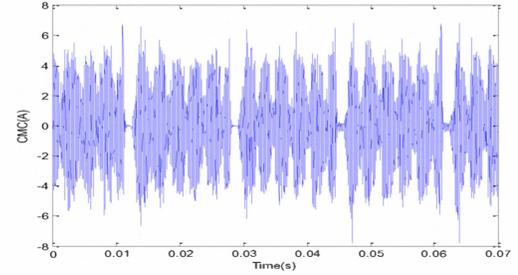
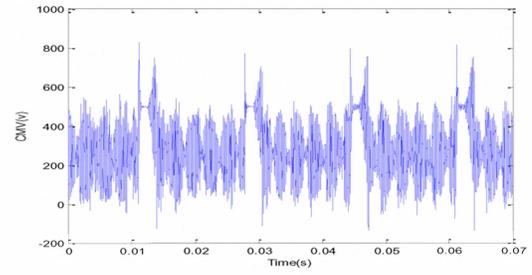


(a).SVPWM

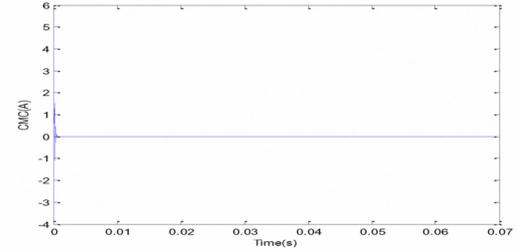
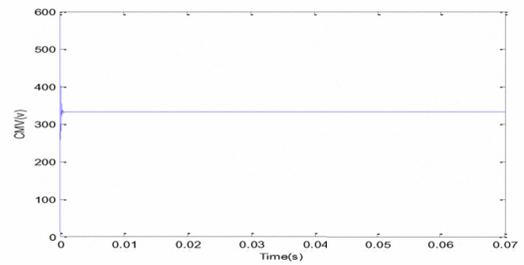


(b).AZSPWM

Figure 6.CMV and CMC of (a).SVPWM(b).AZSPWM



(a).NSPWM



(b).RSPWM

Figure 7.CMV and CMC of(a)NSPWM(b)RSPWM

All PWM methods don't have the same number of commutation per PWM cycle. In order to make a fair comparison, all methods should be operated at the same number of commutation per fundamental cycle. So the switching frequency of each PWM method is scaled with the k_f factor and the square rms harmonic flux is scaled with k_f^2 . Taking the average value of the

local rms harmonic flux function over the full fundamental cycle (spanning the whole vector space) and scaling it with $288/\pi^2$, the harmonic distortion factor (HDF) which is a true measure of AC current ripple rms value, is calculated as follow

$$HDF = f(M_i) = \frac{288}{\pi^2} \frac{1}{2\pi} \int_0^{2\pi} \lambda_{hm-rms}^2 d\theta \quad (5)$$

The HDF function is only M_i dependent. The HDF characteristic of each PWM method is shown in Fig.8. As one can see, the SVPWM has a good performance in overall variation of M_i . AZSPWM and NSPWM have a good HDF characteristic at high

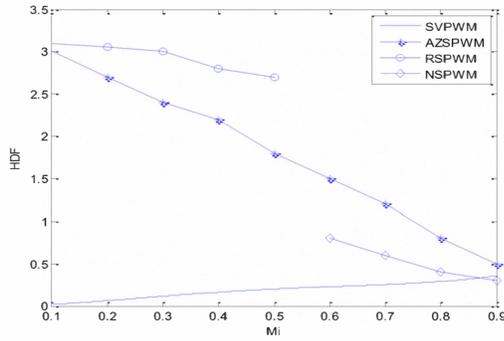


Figure 8. Harmonic Distortion Factor of various PWM

modulation index and at low modulation index have a higher value of HDF. RSPWM operates on a low value of modulation index. In this range, its HDF is very high in comparison with AZSPWM and SVPWM and has bad performance.

F. DC-Link current ripple

The DC-link current of inverter composed of an average DC value and ripple over it. It is important for DC bus capacitor sizing since the capacitor suppresses the entire PWM ripple current. The DC-link ripple current has limiting effect on the capacitor lifetime, so it should be as small as possible. In order to compare the DC link current ripple performance of PWM methods, k_{dc} is defined as follow

$$K_{dc} = \frac{I_{Dch-rms}}{I_{1rms}} \quad (6)$$

Smaller k_{dc} implies smaller capacitor requirement and longer capacitor life. For each PWM method, k_{dc} analytically is evaluated [9] and are given in the following equation

• SVPWM

$$K_{dc} = \frac{2\sqrt{3}}{\pi^2} M_i + \left(\frac{8\sqrt{3}}{\pi^2} - \frac{18}{\pi^2} M_i \right) M_i \cos^2 \phi \quad (7)$$

• AZSPWM

$$K_{dc} = 1 + \left(M_i \frac{9\sqrt{3}}{\pi^2} - \frac{3\sqrt{3}}{2\pi} \right) \cos(2\phi) - M_i^2 \frac{18}{\pi^2} \cos^2(\phi) \quad (8)$$

• RSPWM

$$K_{dc} = 1 + M_i \frac{6}{\pi^2} \cos(2\phi) - M_i^2 \frac{18}{\pi^2} \cos^2(\phi) \quad (9)$$

• NSPWM

$$K_{dc} = 1 + \left(M_i \frac{24}{\pi^2} - \frac{3\sqrt{3}}{\pi} \right) \cos(2\phi) - M_i^2 \frac{18}{\pi^2} \cos^2(\phi) \quad (10)$$

k_{dc} is a function of M_i and the power factor angle and for each PWM method are depicted in Fig.9. At low modulation index, RSPWM and AZSPWM exhibit large stress especially at low $\cos(\phi)$. At high modulation index, NSPWM and AZSPWM have a comparable value of k_{dc} to conventional method SVPWM, and have a good performance.

IV. Deadtime effect

In this section, the optimal common-mode voltage reduction pulsewidth modulation (PWM) techniques with dead-time effect consideration are investigated. Fig.10 shows the common-mode voltage for a three-phase inverter system with 500-V dc-link voltage and $2\mu s$ dead time for RSPWM. As shown in Fig.10, the common mode voltage (CMV) has “unexpected” spikes which increase with increasing inverter switching frequency. The unexpected spike occurs during the period of dead time. When the currents of phase “a” and phase “b” are both positive, the unexpected spikes of CMV occurs. As shown in Fig. 11(a), the common-mode voltage is constant without considering the dead time effect. Fig. 11(b) shows the voltage waveforms, including common-mode voltage, while taking the dead-time effect into account. As shown in Fig.11(b), the unexpected spike occurs when the current of phase “a” and phase “b” are positive. Under this condition, the output voltage for phase “a” and

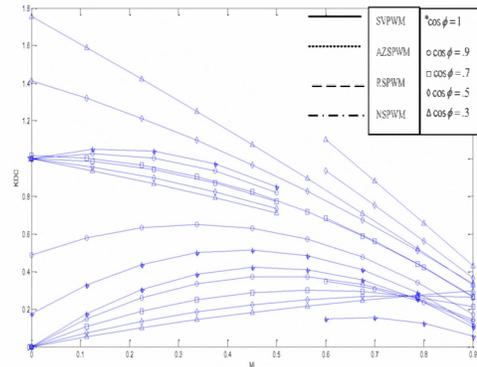


Figure 9. DC bus ripple factor (K_{dc})

III. CONCLUSIONS

This paper investigates the performance characteristics of RCMV-PWM methods and provided a comparison to the standard PWM method, SVPWM. The RCMV-PWM Methods are introduced and their pulse patterns are illustrated. Among all these methods, NSPWM has less switching per period which reduced the losses and RSPWM has much switching per period. With respect to the voltage linearity, AZSPWM and NSPWM have same maximum voltage linearity like SVPWM and RSPWM has the lowest one. For increasing the output voltage, we must increase the DC bus voltage which reduces the efficiency and reliability of the system. Analytical and computer simulation based methods utilize to obtain DC-Link current ripple (K_{DC} index), AC output current ripple (HDF index), CMC and CMV of RCMV-PWM methods. The results show that AZSPWM and NSPWM have less DC-Link and AC output current ripple especially at high modulation index same as SVPWM. In case of CMC and CMV, RSPWM eliminates the CMC and has the best result. By considering the dead time effect, AZSPWM and NSPWM have no CMV spike unlike RSPWM. Among all RCMV-PWM methods, we believe that AZSPWM and NSPWM exhibit superior overall behavior especially at high modulation index and RSPWM only eliminate the CMC. If only CMC is important subject, the RSPWM is the best choice.

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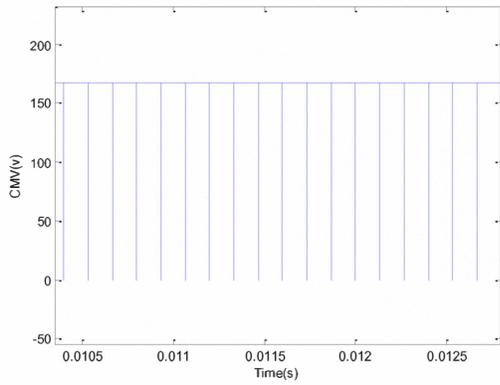


Figure 10. CMV of RSPWM

phase "b" are clamped to the negative dc-link rail, resulting in a spike of $V_{com} = 0$. With carefully considering the switching patterns and common mode voltage waveforms shown in Fig.10 and Fig. 11, we conclude that *the unexpected spikes of common mode voltage may come out only at the instants when two phases commutate simultaneously*. At these commutation instants, the outputs of three phases are clamped to either the positive or negative dc-link rail caused by the dead time, thereby increasing the common mode voltage even when using only nonzero switching states.

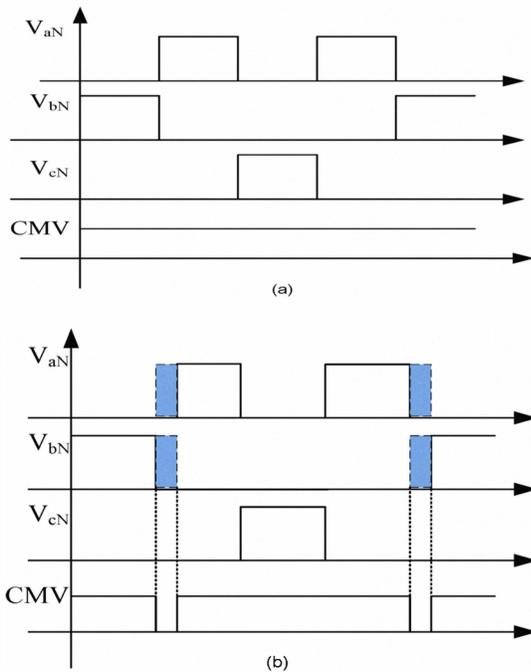


Figure 11. Illustration of voltage waveforms and CMV:(a)Without (b)With consideration dead time effect.