An Ultra-low Power Redundant Split-DAC SA-ADC using Power-optimized Programmable Comparator

Amir Arian
Electrical Engineering Department, Kavian Institute of Higher Education, Mashhad, Iran

Saied Hosseini-Khayat
Electrical Engineering Department, Ferdowsi University of Mashhad, Iran

***Abstract* — An ultra-low power successive approximation (SA) analog-to-digital converter (ADC) based on the redundant search algorithm is proposed. The power consumption of the comparator is significantly reduced through gain control of the preamplifier during conversion phase. The number of analog sampling switches is reduced to one by introducing modified clock boosting switch. A single-ended 8-bit SA-ADC is designed in a 0.18 µm CMOS process. Our simulation results show that at a supply voltage of 0.9 V and an output rate of 500 kS/s, the SA-ADC achieves a peak signal-to-noise-and-distortion (SNDR) ratio of 48 dB, and a power consumption of 1.63 µW, resulting in a figure of merit of 15.9 fJ/conversion-step.**

I. INTRODUCTION

Many energy constrained applications such as micro-sensor networks, biomedical instrumentation and portable devices demand for analog-to-digital converters (ADCs) with resolutions between 8 and 12 bits, speed of less than 1 MHz but extremely low power consumption. Successive approximation ADC (SA-ADC) exhibits the best power-efficiency over other common ADC topologies due to its minimal active analog circuit requirement [1], [2], and [3].

As shown in Fig.1, the conventional SA-ADC consists of a comparator, a successive approximation register (SAR), a capacitive-array digital-to-analog converter (DAC) and a sample and hold (S/H) circuit that can be realized with the capacitive DAC itself. In this architecture, the sampled input voltage is successively approximated and the output digital bits are determined through a number of comparison steps. In each step, the comparator decision must be as accurate as the total converter precision.

The conventional SA-ADC architecture suffers from random offset voltage of the comparator during comparison steps. In a binary SA-ADC, the comparator is typically designed to have an input referred offset lower than 1 LSB in all comparison steps. However, reducing comparator offset voltage is accompanied with more power consumption. Instead of a binary search, using a non-binary search enables one to tolerate more comparator offset errors in the first few comparison steps. This eliminates the requirement that comparator offset to be less than 1 LSB and thus can be used to reduce the comparator power consumption.

In this paper, a low-power SA-ADC is proposed based on redundant search algorithm. As a design example, an ultra-low-power 8-bit 500 kS/s SA-ADC is designed in a 0.18 µm CMOS technology. Our simulation results at supply voltage of 0.9 V show that the designed SA-ADC consumes only 1.63 µW of power.

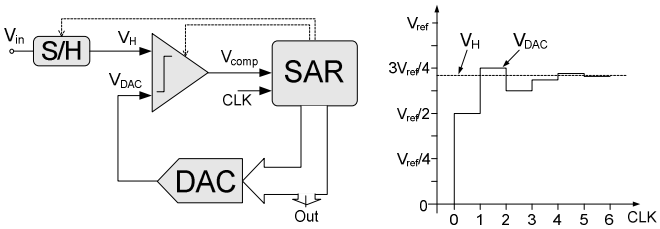

Fig.1. Principle of SA-ADC operation.

The proposed low-power solution for comparator is explained in Section II. Design considerations of the implemented ADC are addressed in Section III. Section IV presents simulation results of the ADC, followed by conclusions in Section V.

II. COMPARATOR POWER-REDUCTION SOLUTION

A. Digital Correction of Comparator Offset

A redundant search algorithm realizes N-bit resolution SA-ADC in M comparison steps ($M \geq N$). Assuming that the analog input voltage range is normalized to $[0, 2^N]$, in the k-th comparison step of a redundant search, the k-th bit, $b(k)$, is found by comparing the input voltage with $ref(k)$ given in [4], as follows:

$$ref(k) = j(1) + \sum_{i=2}^{k} s(i-1) \cdot j(i) \tag{1}$$

where $s(i)$ is equal to 1 if $b(i)=1$ or -1 if $b(i)=0$ and $j(i)$ is a positive integer value determining the voltage jump of the DAC at i-th step. The only constraints on choosing these jumps are the following ([4]):

$$j(1) = 1 + \sum_{i=2}^{M} j(i) = 2^{N-1} \tag{2}$$

$$0 \leq e(i) = 1 - j(i+1) + \sum_{k=i+2}^{M} j(k) \qquad 1 \leq i \leq M-1 \tag{3}$$

where $e(i)$, determines the maximum acceptable comparator offset error at the i-th comparison step ($e(i=M)=0$), which still can be compensated due to the redundancy. At the end of the search, an M-bit redundant code is obtained. The output binary code can be obtained from:

$$B_{out} = \sum_{i=1}^{M} b(i).w(i) \tag{4}$$

where $w(i)$, presented in [5], is the weight of i-th bit, i.e. $b(i)$, and given by:

$$w(i) = \begin{cases} 2\,j(i+1) & 1 \leq i \leq M-1 \\ 1 & i = M \end{cases} \tag{5}$$

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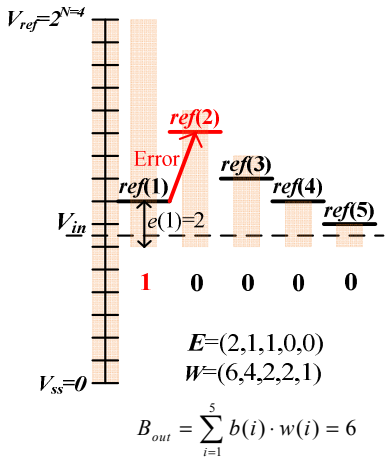

Fig. 2. An example of comparator offset error compensating procedure for a redundant search with N=4, M=5 and the jump vector J=(8,3,2,1,1).

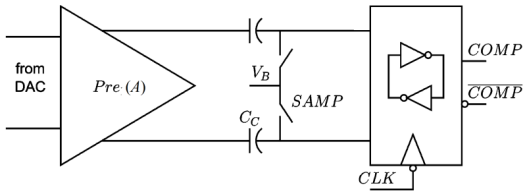

Fig. 3. Comparator with a stage of preamplifier and regenerative latch. The output offset storage technique is employed on preamplifier.

Based on (2) and (3), for an N-bit M-step redundant search, there are many solutions for vector $\boldsymbol{J}$, $\boldsymbol{J}\triangleq(j(1), j(2), \ldots, j(M))$, to be chosen. Fig. 2 shows an example of error compensating procedure for a solution of redundant search algorithm with N=4 and M=5. For the specified input (V_{in}), there is a wrong decision in the first comparison step. However this error does not exceed the first compensated range. Consequently, the search algorithm with redundancy is able to find the correct code. Therefore, 2 LSB offset error in the first comparison step can be digitally corrected and the comparator offset characteristic may be relaxed.

B. Proposed Preamplifier Gain Control Technique

The comparator in an SA-ADC is typically composed of a linear preamplifier stage followed by a regenerative latch. The preamplifier provides both sufficient gain to compensate for the relatively high input referred offset voltage of the latch and isolation from latch kickback noise. As shown in Fig. 3, the output offset storage (OOS) method is also used to reduce the preamplifier contribution to the comparator offset. Under this condition, the comparator input referred offset voltage (=V_{OC}) is

$$V_{OC} \cong \frac{V_{OL}}{A} \tag{6}$$

where V_{OL} is the latch input referred offset voltage and A is the preamplifier gain. In a conventional binary SA-ADC, the comparator offset voltage is designed to be fixed in all comparison steps. But in the i-th comparison step of a redundant SA-ADC, based on the $e(i)$, comparator offset can be larger than that of binary case. Thus the preamplifier gain can be reduced in the i-th comparison step of a redundant SA-ADC. This may be used to reduce preamplifier power consumption. Reducing preamplifier power consumption can lead to significant reduction of total power of the converter because in the SA-ADC, preamplifier is usually only circuit consuming static power. The power saved using this technique depends on preamplifier circuit structure and the selected values of $e(i)$'s through comparison steps. One can select an optimal scheme among many possible schemes.

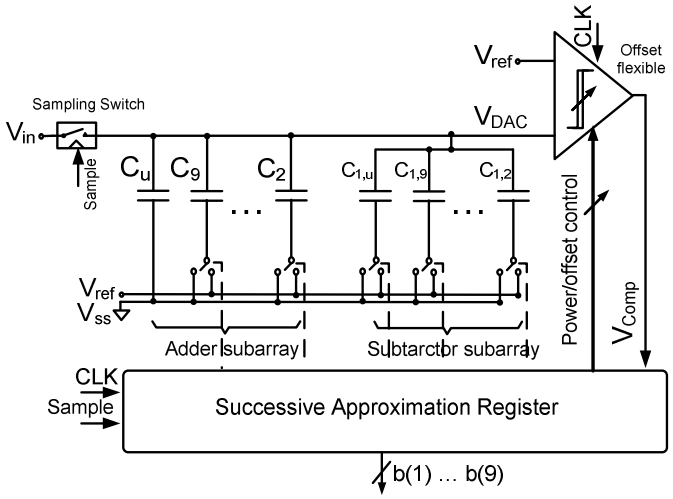

Fig. 4. Schematic of the proposed 8-bit 9-step redundant SA-ADC where $C_i=C_{1,i}=j(i)\cdot C_u$.

III. Circuit Implementation

In this paper, a non-binary search algorithm is employed in implementing low-power 8-bit 500 kS/s redundant SA-ADC in a 0.18 µm CMOS technology. In this section, circuit design considerations for this ADC are discussed.

A. Proposed Architecture

A fully-differential structure benefits from better common-mode noise rejection and less distortion, but at the cost of more power consumption. Since our design targets a moderate-resolution SA-ADC, a single-ended structure is chosen in order to reduce power.

Fig. 4 shows the schematic of the proposed 8-bit single-ended redundant SA-ADC which is based on the non-binary split capacitive-array DAC presented in [6]. This non-binary capacitive-array provides 37% lower switching energy consumption over conventional binary-weighted capacitive-array [6], [7], resulting in an energy-efficient converter. Since each extra comparison step adds one clock cycle to the conversion phase, and also increases the complexity of the control logic circuit, for this 8-bit implementation only one extra comparison step (i.e. M=9) is used.

All building blocks of the SA-ADC are supplied by a reference voltage equal to V_{DD}=0.9V. The input common-mode voltage level of the comparator is also constant value $V_{ref}=V_{DD}$, thus reducing its dynamic offset. In this structure, all bottom switches in the DAC connect to either V_{ref} or the

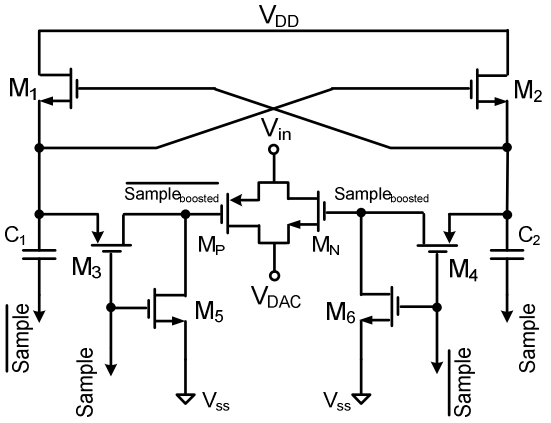

Fig. 5. Schematic of the proposed sampling switch.

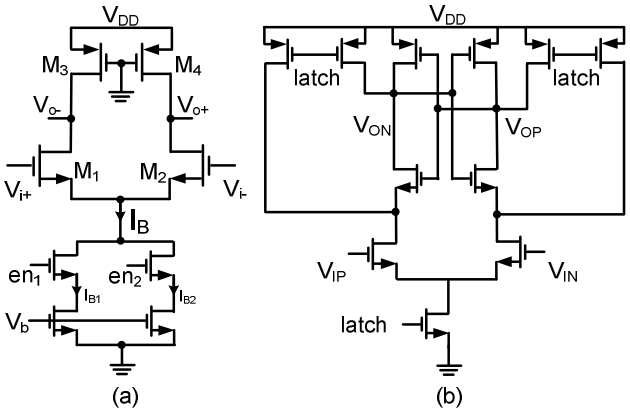

Fig. 6. Schematic of comparator circuit composed of (a) Preamplifier with two adjustable gains, (b) Conventional latch.

ground. Therefore, these switches do not suffer from poor on-resistance and were built with simple nMOS devices for the ground references and pMOS for the supply references. In order to preserve the desired low-power characteristic, the analog input is sampled on the top plates of capacitors, which decreases the number of required sampling switches from eighteen to one. But special care must be taken in designing this switch. Because with V_{DD}=0.9 V, it may not be fully turned on in the sampling phase and also it may not be fully turned off in the conversion phase resulting in V_{in}-dependent charge leakage and thus significant drop in the dynamic performance of the converter.

B. Modified Clock Boosting Sampling Switch

The clock boosting switch presented in [1], is modified in order to be able to generate two different boosted signals in both sampling and conversion phases required for proposed structure. Fig. 5 shows the designed switch composed of a transmission gate (M_P and M_N), driven by a boosted driver. The V_{DD}=0.9V is around the sum of the threshold voltages of nMOS's and pMOS's (V_{tn}+V_{tp}) in a standard 0.18 µm CMOS technology. Thus the sampling switch may show poor on resistance in the sampling phase. The boosted driver provides the boosted signal $\text{Sample}_{\text{boosted}}$ in the sampling phase for the gate of M_N to overcome this issue. The amplitude of boosted signal, $\text{Sample}_{\text{boosted}}$, is $2V_{DD}-\Delta V$, where ΔV depends on the ratio between C_2 and the parasitic capacitances at the gate nodes of M_N.

Another potential problem must be considered in the conversion phase of the proposed SA-ADC: The node V_{DAC}, may swing above V_{DD} through comparison steps. For V_{in}=V_{DD}, during the first conversion cycle, V_{DAC} reaches a worst-case maximum voltage of $1.5V_{DD}$. The transistor M_P of the sampling switch must then remain strongly off even when one side of the switch is at $1.5V_{DD}$; because its leakage current will distort the sampled input. In the conversion phase (Sample=low), the boosted signal $\overline{\text{Sample}_{\text{boosted}}}$ is produced by the boosted driver at the gate of M_P to combat this problem. Depending on the ratio between C_1 and the parasitic capacitances at the gate nodes of M_P, the amplitude of this boosted signal can reach nearly $2V_{DD}$.

C. Comparator with Adjustable-gain Preapmlifier

The design of comparator in the proposed structure needs special considerations; because the preamplifier gain must be tunable during the comparison steps. The comparator, shown in Fig. 6, has a stage of preamplifier followed by a conventional regenerative latch. The preamplifier is a linear amplifier with an input nMOS differential pair M_1-M_2 and resistive loads, formed by pMOS M_3-M_4 operating in the linear region. Using this structure, the gain of preamplifier can be adjusted through its bias current I_B, while the settling time is almost independent of I_B. The required preamplifier gain, and thus required I_B, in each comparison step i, depends on $e(i)$. On account of (2) and (3), the most energy-efficient solution can be found based on the relation between the gain and I_B in the preamplifier.

For this design the selected jump vector is $\boldsymbol{J}$= (128, 62, 31, 15, 8, 4, 4, 2, 1) resulting in the error compensating vector $\boldsymbol{E}$= (4, 4, 5, 4, 4, 0, 0, 0, 0). This solution is a near-optimal result of our design from the energy saving point of view. For this solution, the comparator can adopt at least 4 LSB offset voltage in the first five comparison steps without any drop in converter accuracy. Hence two different gains were considered for the preamplifier. Based on the latch offset voltage (i.e. V_{OL}), the larger gain is selected to be 5 and used in the last four comparison steps while the smaller gain is 1.25 and employed in the first five steps. The enable signals en_1 and en_2 are used for adjusting the gain by controlling the bias current I_B. Due to the low-speed and moderate-resolution required for this ADC, the design of I_B is not limited by thermal noise requirements.

In order to further reduce power consumption, in each comparison step the en_1 and en_2 are also used to fully turn off the preamplifier after the latch fully resolved. In our SA-ADC the preamplifier is idle between this time and the next clock edge and thus it is not required to be turned on throughout this period. The proposed ideas significantly reduce comparator power as confirmed by simulation results. The enable signals en_1 and en_2 can be easily generated by the control logic circuit.

D. SAR and Control Logic

The SAR generates the necessary control commands based on a redundant search algorithm to control the latch,

preamplifier gain/power and DAC. The SAR is built with standard CMOS logic gates. In order to save digital power, all MOSFETs of the digital gates were designed to be as small as possible to minimize charging capacitances of the internal circuit nodes.

IV. Simulation Results

The designed low-power SA-ADC was simulated at different process corners of the 0.18 µm CMOS technology. The total power dissipation of the SA-ADC is 1.63 µW with a 0.9 V supply. The power consumption of the comparator is 0.41 µW. The 8-bit 9-step redundant DAC uses MIM capacitors and consumes a switching power of 0.88 µW. The value of unit capacitor (i.e. Cu) is set to 20fF based on matching requirements over KT/C thermal noise consideration. Fig. 7 shows the power consumed by the main components of proposed redundant SA-ADC compared to those of its conventional binary counterpart working at the same specifications. As can be seen, at the expense of a small penalty in logic power, the proposed architecture saves 71% and 37% of comparator and DAC power dissipation respectively. Using the proposed low-power solutions for the preamplifier, comparator consumes 25% of total converter power while that of conventional binary case is 45%. Moreover, the non-binary split DAC of the proposed SA-ADC shows better linearity performance in terms of differential non linearity (DNL) characteristics as compared to conventional binary weighted capacitive array [6], [7].

Fig. 8 shows the FFT spectrum of the ADC output, for a full-scale sinusoidal input signal at a near-DC frequency, sampling rate of 500 kS/s, and over 1000 data samples. The ADC achieves a SNDR and a SFDR of 48 dB, and 60.5 dB respectively. It corresponds to an effective number of bit (ENOB) of 7.68 bits. Fig. 9 plots the simulated SNDR and SFDR of the SA-ADC versus input frequency at different process corners. The results verify the proper operation of the designed ADC in corner process.

Table I gives a performance summery of the ADC at TT process model comparing it with other low-power SA-ADC designs. By defining the Figure-Of-Merit as $FOM=Power/2^{ENOB}{\cdot}f_s$, the design shows an FOM comparable to the state-of-the-art providing measurement results. Our simulation results show that this ADC has also a satisfactory performance when operating at a supply voltage as low as 0.8V and an output rate of 300 kS/s. Table I also lists the performance summary of the SA-ADC at this supply voltage.

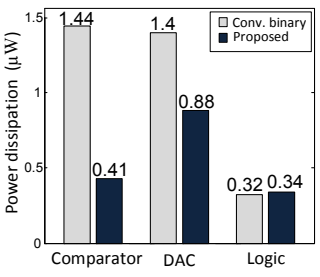

Fig. 7. Power consumption of the proposed SA-ADC versus conventional binary structure.

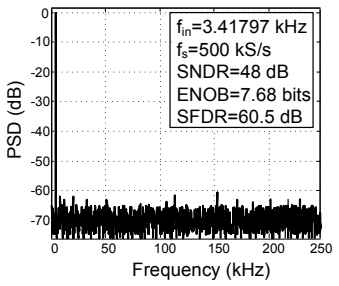

Fig. 8. Output spectrum of the SA-ADC with the 3.41797 kHz sinusoidal input.

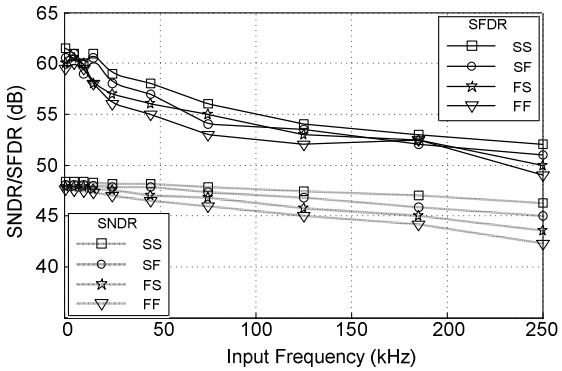

Fig. 9. Simulated SNDR and SFDR versus input frequency at process corners.

TABLE I. Performance summary of pproposed SA-ADC in comparison with other low-power SA-ADCs

	[1]	[2]	[3]	This work	
Technology	0.18 µm	0.18 µm	65 nm	0.18 µm	
Resolution	8 bit	10 bit	10 bit	8 bit	
Supply (V)	0.9	1.2/0.5	1	0.9	0.8
Sampling rate (S/sec)	200 K	150 K	1 M	500 K	300 K
SNDR @ DC (dB)	47.4	55.3	54.4	48	47
SFDR @ DC (dB)	58.9	65	N/A	60.5	57.2
ENOB @ DC (bits)	7.58	8.9	8.75	7.68	7.51
Power diss. (µW)	2.47	2.49	1.9	1.63	0.93
FOM (fJ/c-s)	65	34.7	4.4	15.9	17
Simulation /Measure	M	M	M	S (TT)	

V. Conclusion

A low-power SA-ADC architecture was proposed based on the redundant search algorithm. A 0.9 V, 8-bit 9-step 500kS/s SA-ADC was designed in a 0.18 µm CMOS process base on proposed low-power techniques. Our simulation results confirm that its effective number of bits is more than 7.6 bits while consuming only 1.63 µW, and achieving an FOM as low as 15.9 fJ/conversion-step.

REFRENCES

[1] H-C. Hong, G-M. Lee, "A 65-fJ/Conversion-Step 0.9-V 200-kS/s Rail-to-Rail 8-bit Successive Approximation ADC," *IEEE J. of Solid-State Circuits*, vol. 42, No. 10, pp. 2161-2168, Oct. 2007.

[2] K. L. Chan, *et a*l: "A 8.9-ENOB 2.5-µW 150-KS/s Non-Binary Redundant Successive Approximation ADC in 0.18-µm CMOS for Bio-Implanted Devices," 32nd International Conference of the IEEE EMBS, Buenos Aires, Argentina, August 2010.

[3] M. van Elzakker, *et al*: "A 1.9µW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," *ISSCC Dig. Tech. Papers*, pp. 244-245 Feb. 2008.

[4] T. Ogawa, *et al*: "SAR ADC Algorithm with Redundancy and Digital Error Correction," *IEICE TRANS. Fundamentals*, vol. E93-A, no. 2, 2010.

[5] A. Arian, *et al*: "A 10-bit 50-MS/s redundant SAR ADC with split capacitive-array DAC," *International J. of Analog Integrated Circuits and Signal Processing*, vol. 71, issue 3 (2012), pp. 583-589.

[6] A. Arian, *et al*: "SAR ADC With Redundancy Using Split Capacitive-array DAC," *Proceedings of the 19th Iranian Conference on Electrical Engineering* (ICEE2011), pp. 464-467, Tehran, May 2011.

[7] B.P. Ginsburg, A.P. Chandrakasan, "500-Ms/s 5-bit ADC in 65-nm CMOS with Split Capacitor Array DAC," *IEEE J. of Solid-State Circuit*, vol. 42, no. 4, April 2007.