New Charge Balancing Method Based on Imbalanced Biphasic Current Pulses for Functional Electrical Stimulation

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Abstract: *A new active charge balancing technique for functional electrical stimulation is presented. This method is adopted in a micro-stimulator to be used in deep brain stimulation application. Simulations in a high-voltage 0.18-µm CMOS technology validates the feasibility of the approach and its low power consumption. The power consumption of the charge-balancing circuits contributes 3.4 % of the overall power consumption of the system.*

Keywords: Active charge balancing, neural stimulator, deep brain stimulation.

I. Introduction

The development of biomedical implantable devices has had a great role in treatment of diseases and disabilities in the recent years [1]. Cochlear implant, cardiac pacemaker, and retinal implant are some biomedical implantable devices that have progressed recently. Functional electrical or neural stimulation (FES/FNS) is the common purpose of these devices to restore lost functions of damaged tissues. Electrical stimulation is based on charge injection into the tissue, initiation action potentials and excitation neural reactions [2].

Three methods more commonly used for electrical stimulation are switched-capacitor stimulation (SCS) [3], voltage-controlled stimulation (VCS) [4] and constant current stimulation (CCS) [5]. Among these, the CCS is the most commonly used method, due to its advantages compared to other stimulation methods: high controllability of injected charge and low area occupation [6]. The CCS usually uses biphasic current pulse, in which the stimulation pulse consists of a cathodic phase followed by an anodic phase (Fig. 1). At the cathodic phase, the action potentials are initiated by applied current pulse and neural reaction is elicited. The subsequent anodic phase cancels the charges accumulated on the electrodes. The anodic phases are usually delayed shortly to prevent blocking of action potential propagation [7]. Unfortunately, due to irreversible reactions and mismatch of microelectronic devices, there

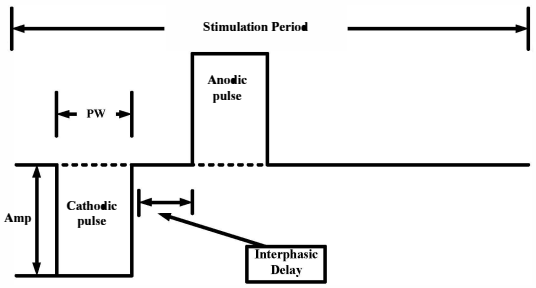

Fig. 1: Biphasic current stimulation pulse

is a difference between the amounts of delivered charges to the electrodes at the anodic and the cathodic phases. Unbalanced charges lead to unwanted extra voltage across the electrodes. If the electrode voltage exceeds its safe range, i.e. water oxidation potential (±50 mV), electrode corrosion and tissue damage can occur. Therefore, charge balance stimulation is necessary to achieve safe electrical stimulation. A few approaches have been introduced to achieve charge balancing in literature. First solution is to insert a large off-chip capacitor in series with the stimulation electrode to prevent dc current flow to electrode over the time [8]. Due to large area occupation of the capacitors, this method cannot be used in multichannel application. Discharging the electrodes after the stimulation phase is another approach applied for charge balancing [9]. Nevertheless, it has been proved that for small electrode sizes, the electrode potential may exceed the safe range [10]. Active charge balancing method is introduced to solve the mentioned disadvantages of the blocking capacitor and the passive discharging approaches. In this approach, the electrode voltage is fed-back to the stimulation circuit and undesirable electrode voltage will be compensated using various techniques.

In this paper, an active charge balancing technique is presented. Power consumption and simplicity of the circuits are improved compared to the other active charge balancing techniques.

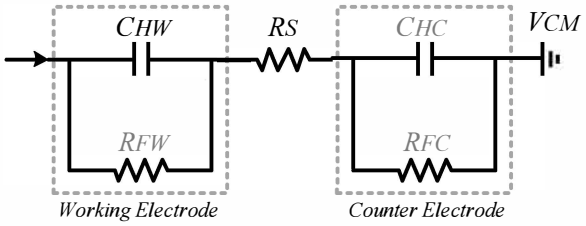

Fig. 2: Electrode-electrolyte model

The paper is organized as follows: The equivalent model of the electrode-electrolyte interface as well as a brief review on previously published active charge-balancing methods is described in section 2. Section 3 explains the proposed method. Simulation results are presented in section 4 and finally, the concluding remarks are addressed in section 5.

II. Literature Review

2.1 Electrode-Electrolyte Interface Model

Fig.2 shows a simplified model for electrode-tissue interface consisting of a solution resistance in series with a capacitive path and a charge transfer path [11]. In this model, C_{HC} and C_{HW} represent Helmholtz capacitors (double layer capacitor) and R_{FC} and R_{FW} represent Faradic resistance of counter and working electrodes, respectively. Note that the double layer capacitance models the non-Faradic charge redistribution while the Faradaic resistance models the Faradic charge transfer. R_S is the solution resistance (also referred to as the access resistance R_A or the ohmic resistance R_Ω) that exists between two electrodes in solution. The value of this resistance depends on the electrode properties such as material and geometry. When stimulation is monopole, counter electrode is usually much larger than the working electrode; hence C_{HC} can be neglected compared to C_{HW}. Additionally, since the Faradic current must be avoided by long-term charge balancing, usually the Faradic resistance R_F is neglected. So in safe stimulation, only R_S and C_{HW} are considered.

2.2. Active Charge Balancing Methods

Active technique is one of the best approaches for charge balancing in neural or functional stimulation. In this technique, the electrode voltage is measured before the stimulation pulse is as applied and this voltage is compared with the electrode voltage that is measured after the stimulation. If the voltage difference exceeds a given range, the feed-back loop consisting of a window comparator and charge balancer block delivers a given amount of charge to neutralize the accumulated charge on the electrode to bring the electrode voltage in the safe range.

In this section we will briefly review the previous works on functional electrical stimulation with active charge balancing approach. Two techniques of charge balancing are proposed in [12]: pulse insertion and offset regulation.

In the first method, after the stimulation phase, the electrode voltage is monitored. If this voltage exceeds the safe range, a short-duration current pulse will be applied to the electrode. This operation will be repeated if the electrode voltage remains out of the safe range. It is proved that this technique is reliable [12] but the main disadvantage is the neural excitation caused by short-duration pulses. In addition, the number of pulses required for charge balancing, hence the total time needed for charge balancing depend on the mismatched charge [11]. The offset regulation is the other active solution for charge balancing [11]. Similar to the pulse-insertion technique, after each stimulation phase, the electrode voltage is compared with a predefined safe range (-50mv, +50mv). An offset DC current is used to neutralize remaining charges on the electrodes instead of small bursts of charges. The amplitude of the DC offset current is increased or decreased if the electrode voltage is lower or higher than the safe range, respectively. After the settling-process time, the background offset current cancels the residual charge completely. It has been proved that this technique guarantees charge balancing [11]. This technique utilizes an extra current source that increases the power consumption of the system.

III. Proposed Technique

Here, a novel technique is proposed to achieve charge balancing based on charge imbalanced biphasic current pulses. The charge-imbalanced biphasic current pulse is the most efficacious and least damaging to tissues or the electrodes [13]. The concept of this method is shown in Fig. 3. Similar to the previous methods, after applying anodic pulse, the electrode voltage is compared with the predefined levels. If the voltage is out of the safe range,

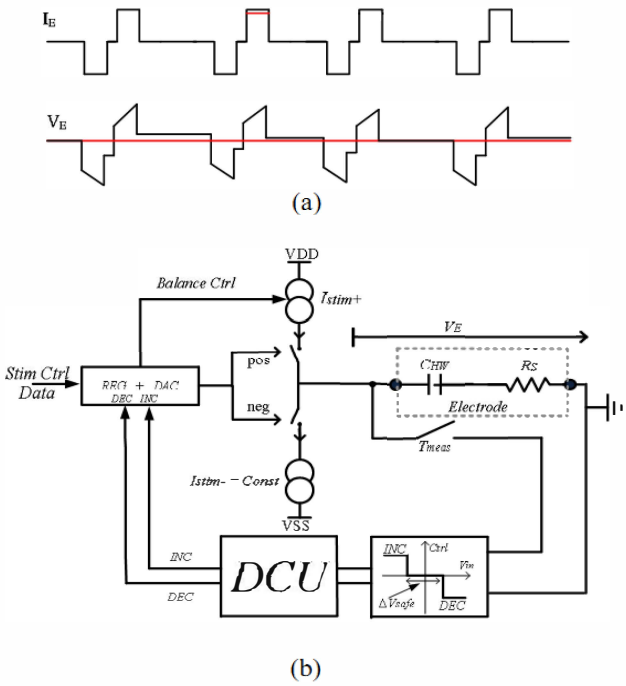

Fig. 3: Proposed technique (a) concept and (b) block diagram

the parameters of subsequent anodic pulse such as amplitude and duration can be adjusted in the digital domain to take the electrode voltage back into the safe range. This adjustment can be done by decreasing or increasing the amplitude or duration of the anodic phase of subsequent stimulation pulse or a combination of these.

In this work, the first adjustment approach i.e. amplitude adjustment is applied. At the measurement phase, the window comparator outputs are given to the digital control unit (DCU) and the DCU generates two digital outputs (Fig. 3). If the voltage of the stimulation electrode (V_E) is greater than the predefined safe range, the decrement signal (DEC) will be set to logical "one". Activation of this signal decreases the amplitude of subsequent anodic pulse and accordingly V_E decreases. For the case in which V_E falls below the safe range, the increment signal INC will be set and a greater amount of charge will be delivered by anodic phase of the following stimulation pulse, so V_E increases. If this procedure repeats, V_E always remains in the safe range. The main critical parameter which must be adjusted carefully is the increment or decrement of anodic pulse; i.e. anodic level variation (ALV). If the value of ALV is not set large enough, charge balancing may not be achieved. Also, since the large value of ALV can take the electrode voltage out of the safe range, it forces another limitation on the maximum value of ALV. Since the mismatch at each period is compensated at the subsequent period, the threshold levels of the window comparator should be set to a smaller value to guarantee safe stimulation. The new threshold for window comparator is:

$$V_{th(new)} = V_{th(old)} - \Delta V_{th} \tag{1}$$

$$\Delta V_{th} = \beta \times \frac{I_c \times W}{C_{HW}} \tag{2}$$

where I_c is cathodic current, β is the percentage of mismatch between cathodic and anodic current and W is the stimulation pulse-width.

Defining the electrode voltage value before the i^{th} stimulation as α, the electrode voltage after the stimulation is:

$$V_{e,i} = \alpha + (I_{a,i} - I_{c,i}) \times \frac{W_i}{C_{HW}} = \alpha + [\beta \times I_{c,i} \times \frac{W_i}{C_{HW}}] \tag{3}$$

where I_a is the anodic current amplitude. Assuming the electrode voltage exceeds the safe range after the i^{th} stimulation process, so the anodic current amplitude at the $(i+1)^{th}$ stimulation must vary in a way to bring the electrode voltage in the safe range:

$$V_{e,i+1} = V_{e,i} + \{[I'_{a,i+1} - I_{c,i+1}] \times \frac{W_{i+1}}{C_{HW}}\} = \{\alpha + [\beta \times I_{c,i} \times \frac{W_i}{C_{HW}}]\} + \{[I'_{a,i+1} - I_{c,i+1}] \times \frac{W_{i+1}}{C_{HW}}\} \tag{4}$$

in which:

$$I'_{a,i+1} = I_{a,i+1} - \Delta I \,. \tag{5}$$

Therefore, we can define the electrode voltage after the $(i+1)^{th}$ stimulation as:

$$V_{e,i+1} = \alpha + [\beta \times I_{c,i} \times \frac{W_i}{C_{HW}}] + \{[(\beta \times I_{c,i+1}) - \Delta I] \times \frac{W_{i+1}}{C_{HW}}\} \tag{6}$$

For a safe stimulation, $V_{e,i+1}$ must be in the safe range, i.e.:

$$-|V_{th(new)}| < V_{e,i+1} < |V_{th(new)}| \tag{7}$$

In order to investigate the feasibility of this technique, it is employed in a conventional current-mode stimulator which is used in deep brain stimulation (DBS) application. Block diagram of the stimulator and charge balancing system are shown in Fig. 4. The part represented by dashed-line is the charge balancing system. The operation of the system is as follows: similar to the conventional stimulator, the anodic and cathodic currents are generated using p-type and n-type current-mode digital to analog converter (DAC) (Fig. 5), respectively . Whereas in this system, the anodic current amplitude is not only determined by the amplitude register, but also it is dependent on the electrodes voltage. The voltage of electrodes are compared to the new threshold levels ($\pm V_{th,new}$). The logic circuits determine the anodic current amplitude according to comparison results. In the case which the electrode voltage is lower than $-|V_{th,new}|$, the adder sums the ALV to the amplitude register's output and causes the electrode voltage increases to its safe range. If the electrode voltage is higher than $|V_{th,new}|$, the subtractor reduces a constant value (ALV) from the amplitude register's output. So the next anodic current amplitude is reduced and the electrode voltage reduces to its safe range. Note that even

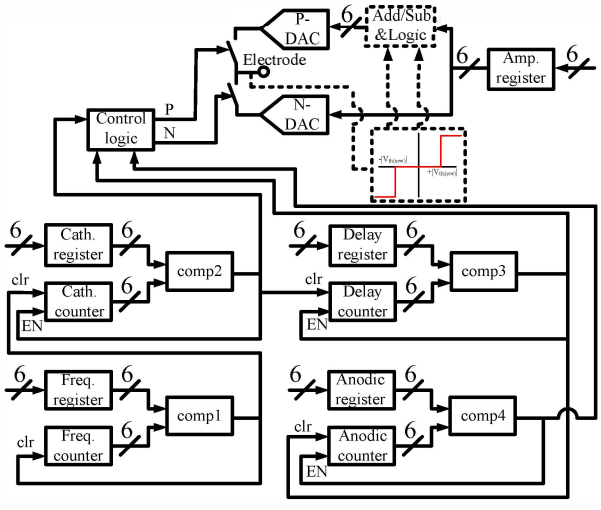

Fig. 4: The block diagram of proposed system

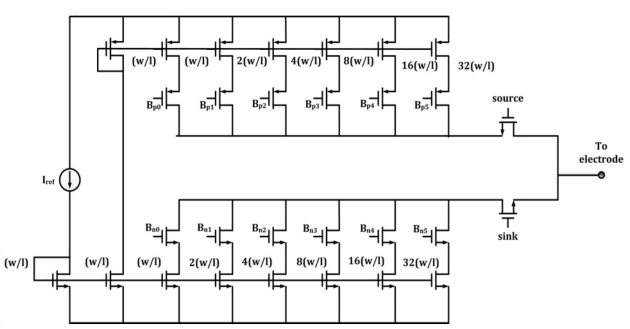

Fig. 5: Current-mode DAC

if the anodic and cathodic pulses are perfectly balanced, the electrode voltages become positive after stimulation [13]. Therefore, since usually lower amplitude for anodic current is needed, the power consumption of the system reduces.

Also, to minimize the power consumption of the system, dynamic comparators are utilized which are only turned on after the stimulation period for a short time (Fig. 6).

IV. Simulation Results

As mentioned in the previous section, a current-mode stimulator is designed and the proposed technique is employed for charge balancing. The specifications of the stimulator are as follow:

stimulator frequency range=50-3000 Hz,
stimulator amplitude range=0-126 µA,
stimulator pulse-width range=5-315 µs
and interphasic delay rage=0-315 µs.

According to these specifications and (7), the ALV can be chosen between 8.5 µA and 26 µA, and $V_{th,new}$ is 46 mV.

The system is designed and simulated in a high-voltage 0.18 µm CMOS technology. Biphasic current pulses have been applied to an R-C load with 10 kΩ

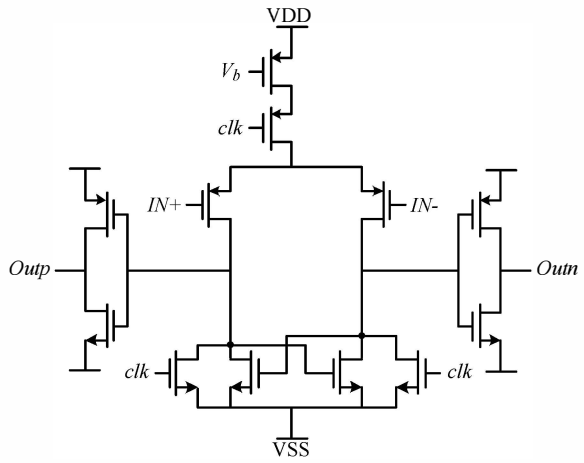

Fig. 6: Dynamic comparator

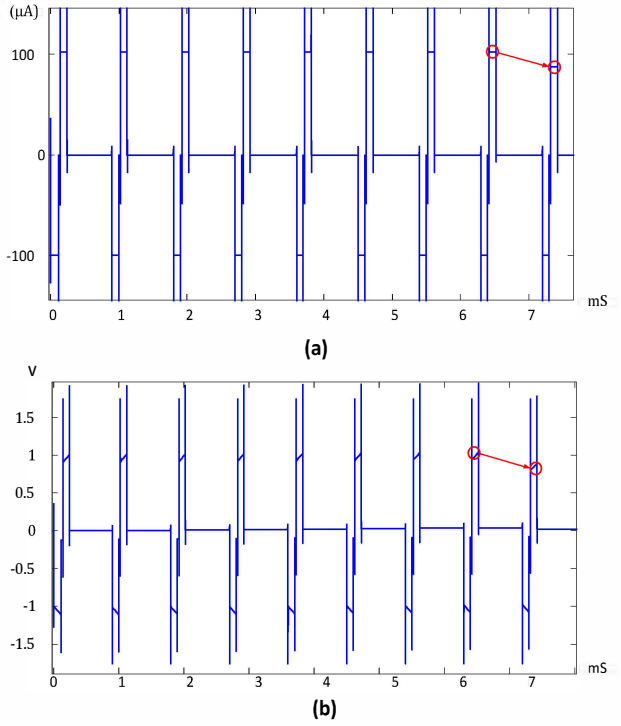

Fig. 7: Simulation results (a) Stimulation pulses (b) Electrode voltage

resistance and 100 nF capacitance. The amplitudes of anodic and cathodic pulses are set to 98 µA and 102 µA to define 4% mismatches. Other stimulation parameters are as follow: The width of the current pulse (PW), stimulation period, interphasic delay and ALV are set to 100 µs, 900 µs, 25 µs and 16 µA, respectively. The stimulation pulses and electrode voltage are depicted in Fig. 7. It is seen that the electrode voltage never exceeds the safe range. Simulations show that the power consumption of this method is lower than other active charge balancing methods, if the amplitude of the anodic pulse is higher than the amplitude of cathodic pulse. Table I presents the power consumption of different parts of the stimulation system. The power consumption of charge balancing circuits is 2.517 µW which contributes 3.4 % of the overall power consumption of the system. The specifications of the proposed technique are compared with recently published charge balancing systems in Table II.

TABLE I: Power consumption of different parts of the stimulator

	Power consumption (µW)
N-DAC	30.687
P-DAC	31.711
Stimulus generator	9.588
Comparators	2.176
Adder/Subtractor	1.86e-3
Comparator clock generator	0.339

TABLE II: Performance Comparison

	CMOS process (µm)	Power Diss. (µW)	Sim/Meas.	Charge balancing method
[14]	0.35 HV	10	Sim.	Charge metering
[15]	0.18	50	Sim.	Charge metering
[16]	0.7 HV	47	Meas.	Charge metering
[7]	1 SOI	200	Meas.	Blocking capacitor
This work	**0.18 HV**	**2.5**	**Sim.**	**Active**

5. Conclusion

This paper describes a low power active charge balancing technique for neural stimulation. Since even for perfectly balanced anodic and cathodic pulses, the electrode voltages become positive after stimulation, the unbalanced pulsed adopted in this technique reduces the power consumption of the system. To minimize the power consumption, the comparators, which contribute the majority portion of the power consumption of the charge balancing circuits, operate dynamically. Also, in comparison with other active charge balancing techniques with complex circuitry (e.g. what proposed in [17]), this technique adopts simple digital circuit that leads to lower power consumption and overall area.

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