Power Reduction Techniques in a 6 bit 1 GSPS Flash ADC

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Abstract—**Flash Analog-to-Digital Converters (ADCs) are usually used in high-speed yet low-resolution applications such as wide-band radio transceivers. Since the power consumption of such ADCs exponentially rises with the number of bits, low-power design techniques are of increasing interest. In this work, the power consumption of the comparators, the most important building blocks in such ADCs, have been reduced. First, a modified circuit configuration is proposed where the value of the kick-back noise is remarkably reduced. Then in order to save power, a power reduction technique is presented based on the principle of turning off the preamplifier of the comparators after the time when output voltages have been decided using an XOR gate. Since the difference of the input voltage with the reference level is not very small for most of the comparators in a Flash ADC, most of the comparators' outputs are ready before the end of the clock period and thus the proposed idea can save up to 40% of the power consumption of the entire ADC. In order to illustrate the effectiveness of the suggested idea, a 6-bit 1GS/s ADC is designed and simulated in a 0.18µm CMOS technology. The circuit consumes 20.2 mW from a 1.8-V supply voltage, and the THD is -32 dB at the input frequency of 200 MHz.**

Keywords- Flash ADC, Low power design technique, low Kick back noise, dynamic comparator.

I. INTRODUCTION

Reliable ultra wideband radio requires 4 bits of resolution and in the order of few a Giga samples/sec (GSPS) [1]. State-of-the-art disk-drive read channels and high speed Ethernet signals use partial-response signaling, which requires 6 bits at conversion rates of 1 GHz and beyond [2]. The converters used in these applications have to combine the stringent speed specifications with the demand for low power consumption. Flash architectures are often chosen because they offer the highest speed. However, this architecture is very power-hungry as the power depends exponentially on the resolution since the comparators are often the largest contributors to the overall power consumption. There are several ways to reduce the power at the same speed and accuracy. Although technology scaling can lower the power, device mismatch will be increased thus posing greater design challenges for obtaining the required resolution. For a given CMOS technology, alternative circuit techniques, such as time-interleaving, requires multiple accurately-speed clocks, and furthermore mismatches in interleaved comparators can cause distortion and spurious tones [3]. Also in a folding architecture, high folding factor results in reduced power consumption, but on the contrary, it lowers the maximum input signal frequency of the A/D converter [4]. In [5], [6] and [7] comparators with built-in reference levels have been used to estimate the comparator thresholds in order to omit the static power of the conventional reference ladder. However, the ADC performance is degraded due to the device mismatches. This paper presents a new technique to lower the power dissipation in Flash ADCs.

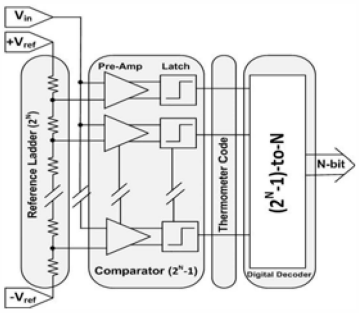

Figure 1. Block diagram of the N-b flash ADC

The organization of the paper is as follows; Section II describes the ADC architecture. The proposed comparator circuit in which the kickback noise is reduced is presented in part A. Besides, the proposed power reduction technique is introduced in part B. The digital decoder that is used in this design is briefly presented in part C. Finally, analyzing the simulation results is presented in the concluding section of the paper.

II. ADC ARCHITECTURE

Fig. 1 shows the block diagram of the N-bit Flash ADC architecture. There are 2^N-1 comparators where N is the number of the bits of the ADC. One of the inputs of each

comparator is connected to the input signal and the other is connected to the reference voltage that is commonly generated by a resistor ladder. Finally, a digital decoder is employed to translate the thermometric output code into an N-bit digital output. Fig.2 illustrates the percentage of the power consumption of the different part of a Flash ADC for a typical design. In Flash ADCs, area and power depend exponentially on the resolution since the comparators are often the largest contributors to the overall power consumption.

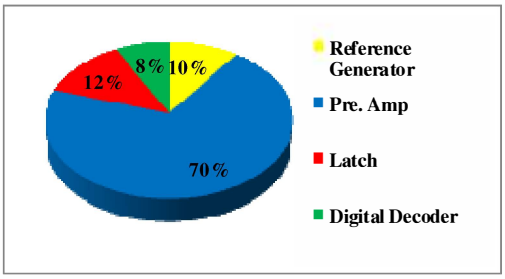

Figure 2. Distribution of power dissipation in the flash ADC

A. *Proposed dynamic comparator and power reduction technique*

The proposed dynamic comparator is shown in Fig. 3. It consists of two stages; preamplifier and latch. The operation of the comparator is as follows. During the reset phase, (*Clock* $=V_{DD}$), the outputs of the latch are reset to ground (by transistors M_{r1} –M_{r2}), while transistors M_{s1}-M_{s2}, disconnect the latch from the preamplifier. Besides, the preamplifier tail transistor (M_c) is cut-off to prevent any static power from supply to the ground. During the decision making phase (when clock goes low), latch reset transistors (M_{r1}-M_{r2}) turn off, while M_{s1}-M_{s2} connect intermediate stage transistors (M_5-M_6) to the latch. Preamplifier tail transistor, M_c, turns on and input transistors force currents into diode-connected loads (M_3-M_4) by a gain of three, which has been set to reduce the latch offset much below one V_{LSB}, (which is 10mV in our design). The intermediate stage transistors transfer the current imbalance proportional to the input voltage to the latch, resulting in latch regeneration and charging the corresponding latch output (outp or outn) to V_{DD}, while other output remains at ground.

In order to reduce the dependence of the input-referred offset of the preamplifier to the common-mode voltage (V_{cm}), transistor M_b has been added. As we know, any mismatch between input transistors contribute the most in preamplifier total offset as far as they control the currents to loads. The following equations indicate how M_1 and M_2 affect the offset of the preamplifier

$$\Delta V_{os-eq-M_1,M_2} = \Delta V_{th1,2} + \frac{\Delta s_{1,2}}{2\times s_{1,2}}\left(V_{gs1,2} - V_{th1,2}\right) \quad (1)$$

where $\Delta V_{th1,2}$ is the threshold voltage offset of the differential pair M_1-M_2, $\Delta s_{1,2}$ is the physical dimension mismatch and ($V_{gs1,2} - V_{th1,2}$) is the effective voltage of the input pair. The first term in (1) is a static offset but the second term is a

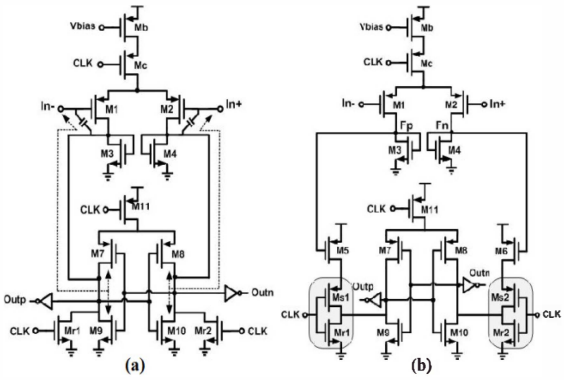

Figure 3. Comparator architecture (a) conventional (b) proposed

signal-dependent dynamic offset. By writing $V_{gs1,2}$ in terms of input common-mode voltage, V_{cm} , the equation can be rewritten as follows,

$$\Delta V_{os-eq-\Delta\beta_{1,2}} = \frac{\Delta w_{1,2}}{2\times w_{1,2}}\left[\frac{w_{ctail}(V_{dd}-V_{th})}{2\times w_{1,2}}\left(\sqrt{1+\frac{4w_{1,2}(V_{cm}-V_{th})}{w_{clk}(V_{dd}-V_{th})}}-1\right)\right] \quad (2)$$

Thus, V_{cm}-V_{th} affects ΔV_{os-eq} in approximately square-root dependence. In order to reduce this dependency, a simple and effective way is to use a cascode-saturated biased MOS transistor (M_b in Fig. 3) in series with the switch MOS (M_c). Since M_b is biased in saturation, its current has little variations with the variation of its drain-source voltage; therefore, it keeps the effective voltage of the inputs nearly constant when V_{cm} is changed.

This architecture also takes advantage of isolating the inputs from latch, which results in much less kickback noise compared to other comparator architectures such as conventional double-tail and conventional comparator. Fig. 4 compares the kickback noise voltage at the input of the conventional and proposed comparator that is shown in Fig. 3. Simulations are done under the same conditions with the same transistor size. Fig. 4 depicts that the kickback noise voltage in the modified structure has reduced from 20 mV to 6 mV.

Fig. 5 illustrates the proposed idea which turns off the preamplifier of those comparators for which the output voltages have been decided using an XOR gate. Noting that one input terminal of all comparators is connected to the input signal and the other to different equally-spaced reference levels, the difference of the input voltage with the reference level is not very small for most of the comparators; thus most of the comparators' outputs are ready before the end of the clock period. The operation of the circuit in Fig. 5 is as follows. During decision making phase, Outn and Outp are decided and either the M8-M9 pair or the M10-M11 pair will

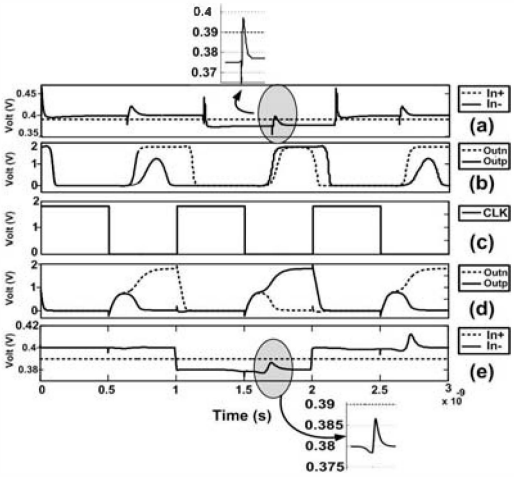

Figure 4. Comparison of kickback noise in a conventional and proposed comparator. (a) Input voltages of a conventional comparator and (e) input voltages of the proposed comparator

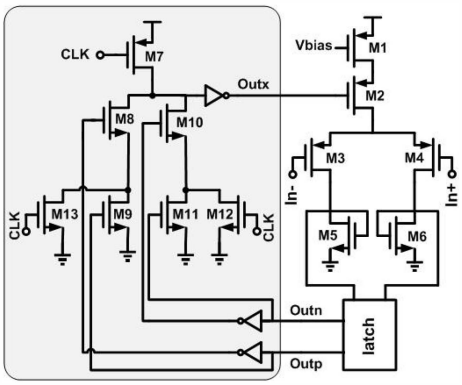

Figure 5. Modified architecture of the preamp

turn on. This will connect Outx to VDD thus the transistor M2 and therefore the entire preamplifier will be turned. Outx voltage is shown in Fig. 6. When the difference of the input voltage with the reference level is very small (e.g. 10 mV), it will take all the clock period for the circuit to decide [Fig. 6 (a)] but where the difference of the input voltage and the reference level is not very small, Outx is ready before the end of the clock period [Fig. 6 (b)].

B. Digital Decoder

Speed and error handling capability are the two main design issues of any Flash ADC encoder. Voltage offsets in the comparators result in bubble errors in the thermometer code. These errors can cause serious degradation in the linearity and the signal-to-noise-and-distortion ratio (SNDR) of the ADC. An effective and popular method to minimize the effect of bubble errors is to insert a *Gray* or *qausi-Gray* encoding stage as an intermediate step before generating binary codes. Because only one bit changes between adjacent *Gray* codes,

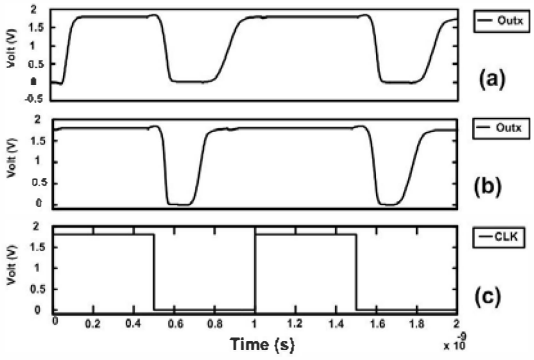

Figure 6. The value of Outx voltage for two cases where the input differential voltage is (a) small (b) large

the degradation in the accuracy of the *Gray* code is gradual as more bubbles appear in the thermometer code [8]. But to further improve the performance of the encoder, the OR gates are replaced with NAND and NOR gates using *DeMorgan's* theorem for the reason that the inverting logic gates have lower propagation delay compared to non-inverting logic gates [8].

III. SIMULATION RESULTS AND CONCLUSIONS

In this paper, a 6-bit 1GS/s flash ADC is presented. A technique is used to turn off the preamplifier of those comparators for which the output voltages have been decided. Fig. 7 shows the comparison between a Flash ADC employing a conventional comparator and one employing the proposed comparator (i.e. the comparator in which the preamplifier is turned off when the comparators' outputs are decided). The power consumption of the entire ADC is saved up to 40%. Fig. 8 shows the simulated value of THD of the ADC as a function of input frequency with a fixed clocked frequency, which shows a THD of -32 dB at the input frequency of 200 MHz.

The technique becomes more beneficial in this resolution or even higher, whereas the difference of the input voltage with the reference level is not very small for most of the comparators. The performance of the entire ADC is summarized in Table I. Also, Table II shows the comparison of this work with other Flash ADCs. It can be concluded that the idea in turning off the preamplifier has shown to be effective in reducing the power consumption of the ADC.

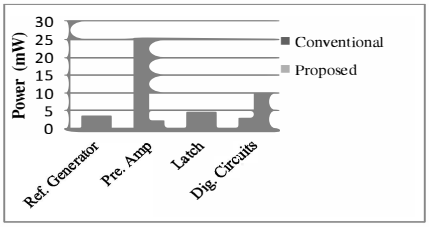

Figure 7. Comparison of power dissipation Distribution

TABLE I. ADC performance summary

Parameter	*Value*
Technology	180nm CMOS TSMC
Resolution	6-bit
Supply Voltage	1.8 V
Sampling Frequency	1 GS/s
Input Voltage Range	640 mV_{pp}
THD	-32 dB @ f_{in}=200MHz
Power dissipation	20.2 mW

TABLE II. Performance comparison

	[9]	*[10]*	*[11]*	*[12]*	*[13]*	*This work*
Technology (CMOS)	65 nm	90 nm	180 nm	90 nm	90 nm	180 nm
Supply Voltage	1.2^v	1.2^v	1.8^v	0.9^v	1.2^v	1.8^v
Resolution	6-bit	6-bit	6-bit	6-bit	4-bit	6-bit
Sampling Frequency	0.8 ***(GS/s)***	1 ***(GS/s)***	1.6 ***(GS/s)***	3.5 ***(GS/s)***	5.5 ***(GS/s)***	1 ***(GS/s)***
THD (@ f_{in}=200 MHz)	-	-	-32	-31.18	-21	-32
Power (mW) ***Simulation or Measurement***	12 Meas.	72 Meas.	240 Sim.	98 Meas.	86 Meas.	20.2 Sim.

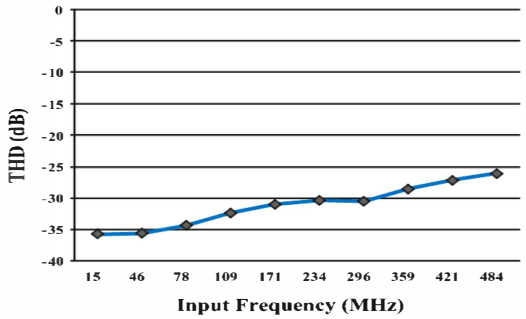

Figure 8. THD vs. input frequency

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