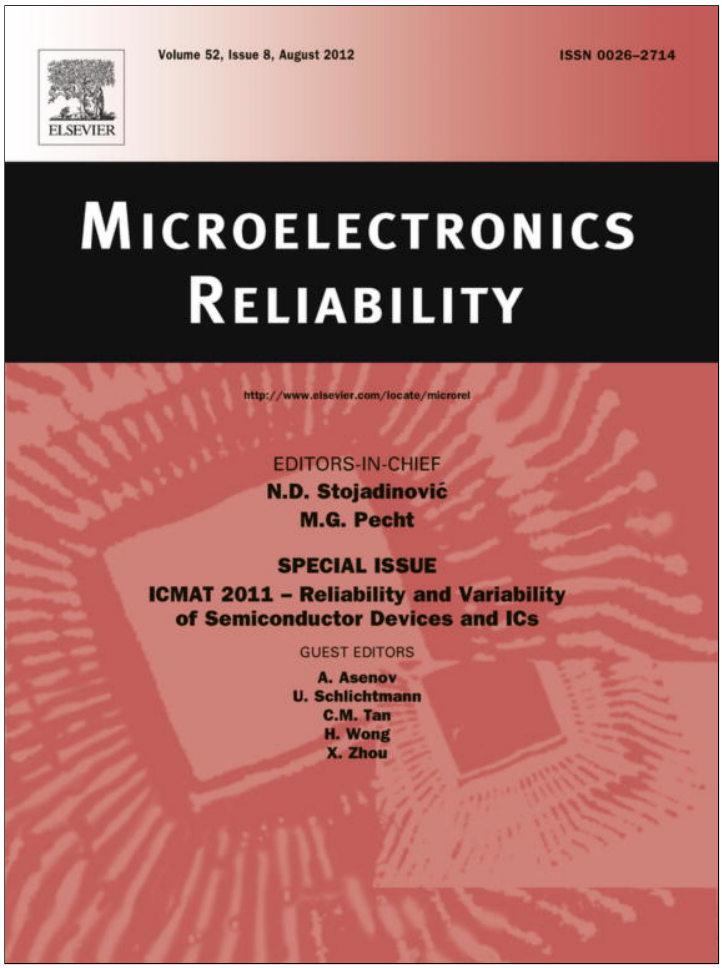

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Impacts of NBTI/PBTI on performance of domino logic circuits with high-*k* metal-gate devices in nanoscale CMOS

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ABSTRACT

Negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) weaken PFETs and high-*k* metal-gate NFETs, respectively. This paper provides comprehensive analyses on the impacts of NBTI and PBTI on wide fan-in domino gates with high-*k* metal-gate devices. The delay degradation and power dissipation of domino logic, as well as the Unity Noise Gain (UNG) are analyzed in the presence of NBTI/PBTI degradation. It has been shown that the main concern is the degradation impact on delay which can increase up to 16.2% in a lifetime of 3 years. We have also proposed a degradation tolerant technique to compensate for the NBTI/PBTI-induced delay degradation in domino gates with a negligible impact on UNG and power.

1. Introduction

Wide fan-in domino gates provide higher performance and compactness compared to their counterpart static gates and are commonly used in the read path of register files, L1 caches, match line of ternary content-addressable memories (TCAMs), flash memories and programmable logic arrays (PLAs) [1]. Fig. 1 shows a wide-OR domino gate with the standard keeper. Dynamic gates need keepers to maintain a high state during evaluation phase (when clock is high). Otherwise, the input noise or the leakage current can discharge the dynamic node. However, the use of the keeper transistor degrades the circuit delay and increases the power consumption through providing contention current [2]. At the same time, Negative-bias temperature instability (NBTI) has long been a major concern for scaled pMOS transistors. NBTI affects the circuit performance through inducing the long-term threshold voltage (V_{th}) drift. Recently, with the introduction of high-*k* metal-gate technology to restrict the gate leakage current especially beyond 45-nm node, PBTI has emerged to be a major reliability concern for *n*MOS transistors due to instability caused by charge trapping at the interface [3].

In this paper, we present a comprehensive analysis on the impacts of NBTI and PBTI degradation on the performance of wide-OR domino gates in a high-*k* metal-gate 32-nm technology. Main performance metrics for domino gates including delay, power and Unity Noise Gain (UNG) are investigated in the presence of NBTI and PBTI during the circuit lifetime. UNG is a metric of robustness and is defined as the DC input noise voltage generating the equal level of noise in the final output of the domino gate. The main observations and contribution of this paper are as follows:

- The degradation of the precharge PFET and the inverter NFET has almost no impact on the circuit's critical delay (i.e. the evaluation delay).
- The degradation of the keeper decreases the circuit's evaluation delay.
- The NBTI degradation of the output inverter PFET and the PBTI degradation of the pull-down path have considerable impacts on the circuit's evaluation delay.
- The BTI degradation decreases the leakage current and the on-state current of all the devices which in turn decreases the power. However, the increase of $|V_{th}|$ in the inverter PFET makes the output transition slower which leads to a slower transition of the keeper and consequently increases the contention power to some extent. On the other hand, the $|V_{th}|$ increase in the keeper decreases the contention power
- Unity Noise Gain (UNG) is decreased by the degradation of the keeper and is increased by the degradation of pull-down network; however, the impact of the pull-down network degradation is much more dominant in the overall impact of transistors. The overall impact of the NBTI/PBTI degradation in the circuit is a considerable increase of UNG up to 39.6% during the circuit lifetime.
- We also propose an NBTI/PBTI-tolerant design technique for dynamic logic gates based on inverter PFET upsizing.

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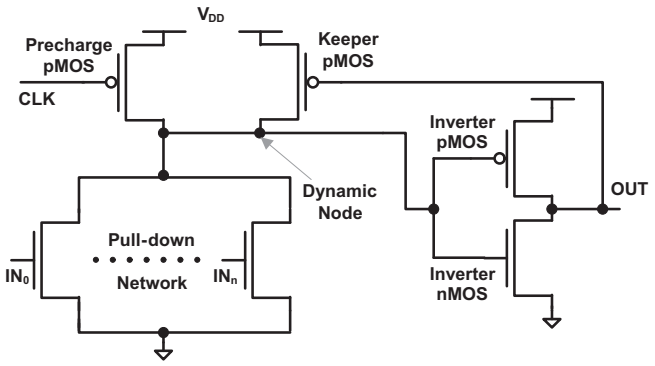

Fig. 1. Footless wide-OR domino gate.

The remainder of the paper is organized as follows. In Section 2, the details of our NBTI/PBTI simulation model used in conjunction with 32-nm high-*k* metal-gate Predictive Technology Model (PTM) [4] are described. The effects of NBTI and PBTI degradation on domino logic gates are explained in Section 3. In Section 4, the impact of upsizing just the output inverter PFET, as a technique to mitigate the NBTI/PBTI degradation, has been investigated. Finally, the conclusion is presented in Section 5.

2. NBTI and PBTI model

NBTI occurs when pMOS transistor is negatively biased ($V_{GS} = -V_{DD}$) at elevated temperatures and causes the absolute value of the threshold voltage (V_{th}) to increase with time. This leads to gradual degradation of current drive and increases the circuit delay. NBTI has been mainly attributed to the H dissociation from the Si–H bonds at the oxide/silicon interface. The H-species diffuse into the oxide, leaving traps at interface and giving a rise in $|V_{th}|$. When stress conditions are removed ($V_{GS} = 0$), H species can diffuse back to interface and passivate dangling Si-bonds recovering NBTI degradation to some extent. Thus, the device lifetime under alternating periods of stress and recovery (ac stress) is longer than that predicted by DC stress measurements [5,6]. The corresponding effect for *n*MOS transistors is PBTI which is commonly small and negligible for oxide/poly-gate devices. However, NFETs with high-*k* gate, exhibit significant charge trapping [7] and thus PBTI-induced drift in V_{th} must be considered for correct analysis and design margining.

The V_{th} drift of PFET (NFET) due to NBTI (PBTI) can be described by DC Reaction-Diffusion (RD) framework when the device is under static stress. Under dynamic operation conditions, the DC RD model is modified by a prefactor to account for the recovery mechanism (AC RD model). This prefactor is a function of the signal (stress) probability and is relatively independent of the signal frequency [8]. We have modeled the V_{th} drift due to NBTI/PBTI based on an exponential behavior as proposed in [7] which is expressed by

$$\Delta V_{th} = \Delta V_{max} \cdot (1 - \exp(-(t/\tau)^{\beta}) \quad (1)$$

where ΔV_{max}, τ and β are fitting parameters. We have accurately fit the above formulation with the V_{th} drift values reported in [8] for PTM High-*k* 32-nm device model with a supply voltage of 0.9 V and a temperature of 125 °C. The resulted values are shown in Fig. 2. The prefactors of ac RD framework in our analyses are from [9].

3. Impacts on wide fan-in domino gates

To analyze the NBTI/PBTI impact on dynamic logic circuits, we have designed a wide-OR dynamic gate with eight inputs as shown in Fig. 1. In order to have a low-contention circuit and

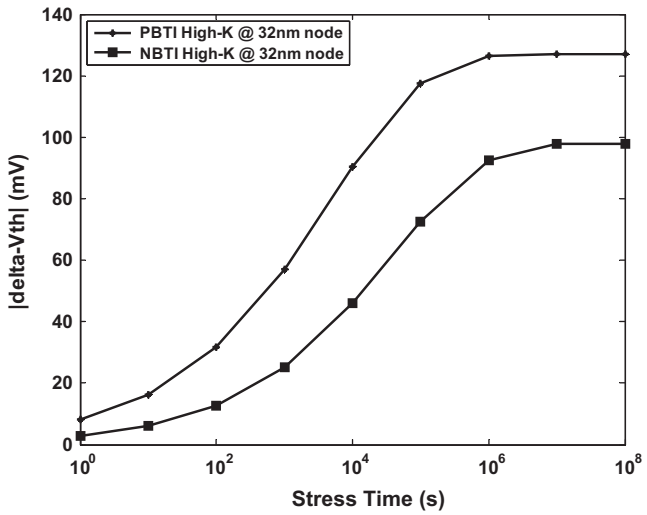

Fig. 2. V_{th} drifts induced by NBTI and PBTI for a 32 nm high-*k* technology.

at the same time have reasonable noise immunity, the keeper transistor is sized so that its saturation current is equal to about 25% of the current provided by the pull-down transistors. The measured UNG is about 0.23 normalized to VDD. In designing a domino logic circuit, the keeper ratio (*K*) criteria indicates the relative current capabilities of the keeper and the pull-down network and is defined as [10]

$$K = \frac{\mu_{eff,p} \cdot (W/L)_{keeper}}{\mu_{eff,n} \cdot (W/L)_{Pull\text{-}Down}} \quad (2)$$

The keeper ratio provides a way to trade off robustness and performance in standard domino gates. As the size of the keeper transistor increases, the noise immunity increases; however, the circuit speed degrades and the power consumption increases. In low contention designs, the keeper ratio is usually much smaller than unity.

The output static inverter is skewed for fast low-to-high transition so the PFET size is wider than the NFET size by a factor of four. The capacitive load has been set equal to the input capacitance of a 16_x minimum size inverter. The circuit has been simulated using the BSIM 32-nm Predictive High-*k* Metal-Gate Model at a temperature of 125 °C and a supply voltage (V_{DD}) of 0.9 V. The clock frequency is 1 GHz. At first, we considered the degradation of each transistor in the circuit individually to understand the impact of that transistor on the circuit performance metrics including delay, power and UNG. Then, the circuit was simulated considering the NBTI/PBTI degradation for all transistors. In a wide-OR domino gate with uncorrelated inputs, the probability of the input to be in state "0" is equal to the probability of the input to be in state "1". Moreover, if there is a high state in at least one of the inputs, the dynamic node discharges and the final output will be in the high state. Therefore, for a dynamic OR with n inputs the probability of having a high state in the output node ($P_{out}(1)$) is

$$P_{out}(1) = 1 - (1/2)^n \approx 1 \quad \text{if} \quad n \gg 1 \quad (3)$$

The assumption of $P_{out}(1) \approx 1$ is reasonable due to the fact that domino logic is usually used for high fan-in structures ($n > 4$) because of its compactness and high speed. So if a duty cycle of 0.5 is considered for the clock signal, the dynamic node and the output node will be low in about 50% of each clock period leading to a BTI stress probability of 50% for keeper and the inverter transistors.

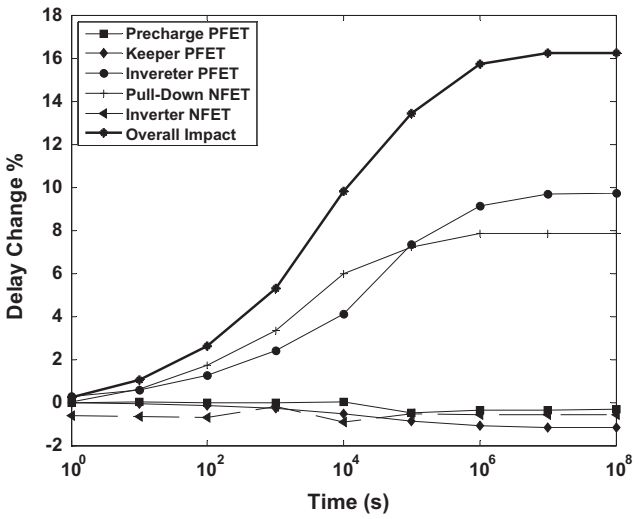

Fig. 3. Percentage of delay change during the circuit lifetime.

3.1. Impacts on delay

Fig. 3 shows the percentage of delay change due to NBTI/PBTI degradation during a circuit lifetime of 3 years ($\approx 10^8$ s). The circuit delay is measured from input IN_0 to OUT (referring to Fig. 1) in the worst case which occurs when only one of the inputs has a 0-to-1 transition during the evaluation phase (CLK = high). As it can be seen in Fig. 3, the degradation of the precharge PFET and the inverter NFET has almost no impact on the circuit delay. This is due to the fact that these transistors are off in the evaluation phase.

When the degradation is considered for the keeper, the circuit delay is decreased. This is due to the fact that the NBTI degradation of the keeper leads to less contention between the keeper and the pull-down network. Therefore, the voltage change in the dynamic node occurs faster leading to a faster transition of the final output. The NBTI degradation of the output inverter PFET has relatively a considerable impact on the circuit delay. Firstly, the delay increases because the output transition speed decreases. Secondly, a slower transition in the output causes the keeper turn off later which in turn leads to more contention and a slower transition of the dynamic node and consequently a slower transition of the output (a positive feedback mechanism). The PBTI degradation of the pull-down path has also a considerable impact on the circuit delay. It makes the transition of the dynamic node and consequently the transition of the output node slower leading to an increase of delay. As it can be seen in Fig. 3, the overall NBTI/PBTI degradation of all transistors available in the circuit causes an increase of more than 16.2% in the circuit delay during a lifetime of 3 years.

The degradation impact on delay can be also described considering the fact that in the evaluation phase, the delay from input to output for a signal transition can be divided into two stages; the first phase is the delay from input up to the dynamic node (t_{PHL}) and the second phase is the delay from the dynamic node to the output t_{PLH} which can be approximated as follows

$$T_{delay} = t_{PHL} + t_{PLH} = \frac{C_{dyn}(V_{DD}/2)}{i_{av,P\cdot D} - i_{av,Kpr}} + \frac{C_{out}(V_{DD}/2)}{i_{av,inv-PFET}} \quad (4)$$

where C_{dyn} is the capacitance at the dynamic node and C_{out} is the capacitance at the output node. $i_{av,P.D}$, $i_{av,Kpr}$ and $i_{av,inv\text{-}PFET}$ are average current values of pull-down network, keeper and the inverter PFET respectively. Eq. (5) shows that the keeper, the pull-down and the inverter pMOS transistors are the main transistors determining the circuit delay. Based on alpha-power law for deep submicron devices, the MOS current is proportional to $\mu_{eff} \cdot (W_{eff}/L_{eff}) \cdot (|V_{GS}| - |V_{th}|)^{\alpha}$ and α is velocity saturation index which is a technology-dependent constant between 1 and 2 [11]. The relative impact of each transistor is dependent on its $\mu_{eff} \cdot W_{eff}$ product and the corresponding $|\Delta V_{th}|$. The increase of $|V_{th}|$ leads to a decrease in the MOS current. Therefore, a BTI-induced increase in $|V_{th}|$ of the keeper tends to decrease the t_{PHL} opposing to the impact of the pull-down network degradation. An NBTI-induced increase in $|V_{th}|$ of the output PFET leads to an increase in the t_{PLH}.

3.2. Impacts on power

Fig. 4 shows the impact of NBTI/PBTI degradation on average power. The power has been measured in one period of clock when one input goes high, discharging the precharge node and producing a low-to-high transition in the output in evaluation phase. The total power of a domino gate can be expressed as

$$\begin{aligned} P_{tot} &= P_{switching} + P_{short\text{-}circuit} + P_{leakage} + P_{clk} \\ &= AF \cdot (C_{dyn} + C_{out}) \cdot V_{dd}^2 \cdot f_{clk} + AF \cdot I_{SC} \cdot V_{dd} \cdot f_{clk} \\ &\quad + V_{dd} \cdot I_{leakage} + P_{clk} \end{aligned} \quad (5)$$

where AF is the activity factor which is equal to the probability that a power consuming transition occurs. In other words, it equals the probability of the gate output goes high in the evaluation phase or $P_{out}(1)$ which is close to unity for a wide-OR domino gate as expressed by Eq. (4). In contrast to static gates, the 0.5 factor is not present in the switching power component since a dynamic gate switches twice in each cycle [12]. I_{SC} for a dynamic gate is the short-circuit contention current between the evaluation network and pMOS keeper during evaluation transition. P_{clk} is the power overhead due to clocking, which depends on the load that the gate puts on the clock.

The BTI-induced increase of $|V_{th}|$ decreases the subthreshold leakage power (I_{SUB}) since I_{SUB} is proportional to $\exp(-V_{th}/mkT)$ leading to a decrease in $P_{leakage}$. It also decreases the on-state current of all the circuit devices which in turn decreases the power. However, the increase of $|V_{th}|$ in the inverter PFET has another opposing effect as well. The degradation of this transistor makes the output transition slower which leads to a slower transition of the keeper and consequently increases the contention power to some extent. On the other hand, the V_{th} shift in the keeper decreases the contention power. The overall impact is a considerable

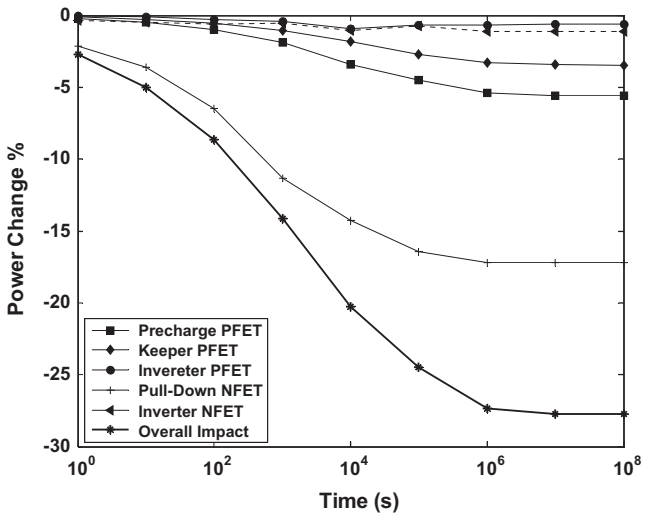

Fig. 4. Percentage of power change during the circuit lifetime.

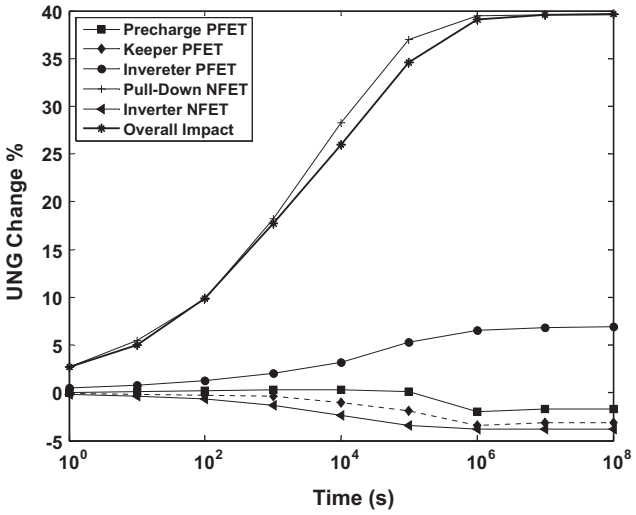

Fig. 5. Percentage of UNG change during the circuit lifetime.

decrease in power up to more than 27.7% during the circuit lifetime.

3.3. Impacts on UNG

In order to investigate the impact of NBTI/PBTI degradation on the circuit robustness we have used UNG criteria. UNG is measured under worst-case conditions when all the inputs are subjected to DC noise (simulated using a slow ramp signal). The voltage that the output and the applied ramp intersect is identified as UNG [13].

The percentage of change in UNG due to the degradation in each transistor of the circuit during its lifetime is shown in Fig. 5. UNG is decreased by the degradation of keeper and is increased by the degradation of pull-down network. Since the keeper ratio (K) is much smaller than unity to have a low-contention circuit and also all transistors of the pull-down network are active while measuring the UNG, the impact of pull-down network degradation is much more dominant in the overall impact of transistors. The PFET and the NFET of the output inverter have opposing impacts on UNG. The PFET degradation makes the 0-to-1 transition of the output slower leading to a slower transition of the keeper and a higher UNG. However, due to the positive shift in the NFET threshold voltage, this transistor turns off faster at the beginning of the evaluation phase, leading to somewhat faster transition of the output and the keeper which decreases the UNG. The overall impact of the NBTI/PBTI degradation in the circuit is a considerable increase of UNG up to 39.6% during the circuit lifetime.

From the above analysis it is obvious that NBTI/PBT degradation in a wide domino gate increases the circuit delay. However, it decreases the power consumption and increases the UNG (or equivalently the circuit robustness) which are desirable. In the following section a BTI-aware design technique is introduced to compensate for delay degradation with a negligible impact on UNG and power consumption.

4. Proposed NBTI/PBTI tolerance technique

According to the analysis presented in Section 3, it is obvious that the main undesirable impact of NBTI/PBTI degradation in wide-OR domino logic is the increase of the circuit delay. This increase is mainly due to the degradation of the inverter PFET as well as the degradation of pull-down network which leads to more contention between the pull-down transistors and keeper. In order to mitigate this impact we propose upsizing just the inverter PFET. Upsizing this transistor increases its initial speed and after the degradation it can have a better performance in comparison with a normally-sized transistor. Moreover, due to the feedback mechanism described in section 3, upsizing this transistor makes the output transition during the evaluation phase faster which leads to a faster on-to-off transition of keeper. This can compensate for the degradation of pull-down network in contention between the keeper and the pull-down network. In other words, the dynamic node will have a faster transition and consequently the output will have a faster transition as well.

To apply this technique, one must find a suitable amount of increase in the inverter PFET width so that the delay in the upsized circuit at the end of its lifetime becomes equal or less than the initial delay of the normal circuit without any degradation, that is

$$\text{delay}(t = \text{life-time})|_{\text{upsized}} \leq \text{delay}(t = 0)|_{\text{normal}} \quad (6)$$

Based on simulations, we upsized the inverter pMOS transistor about 32.5% to completely compensate for the delay degradation in a circuit lifetime of 3 years. Fig. 6 shows the percentage of delay change in the compensated circuit in comparison with the initial delay of the normal circuit which was investigated in the previous circuit. As it can be seen in this figure, the initial delay of the compensated circuit is less than the normal circuit and during the circuit lifetime its delay increases. However, at the end of the circuit lifetime, the degraded delay does not still exceed the initial delay of the normal circuit.

Table 1 shows the percentage of change in the circuit performance metrics in comparison with the corresponding parameters in the initial circuit with normal inverter PFET at the beginning and at the end of circuit lifetime. As it can be seen in this table, BTI-induced degradation of delay is completely compensated. However, there is an increase of just 0.18% in power at the beginning of the circuit operation ($t = 0$). It is noticeable that although increasing the inverter PFET width tends to increase the switching power, the contention power decreases due to a faster transition of the keeper because of the positive feedback described in the previous section and the net power impact becomes negligible. Moreover, the simulations show that this change very rapidly decreases to 0% and less than that due to the circuit degradation (Fig. 7). Similarly, there is a decrease of about −3.48% in UNG at the beginning of the circuit operation, the percentage of change reaches to 0% just in a few seconds (Fig. 8).

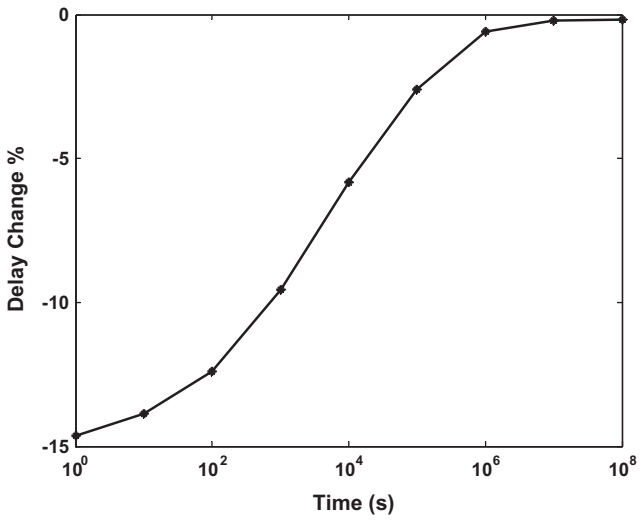

Fig. 6. Delay change in the compensated circuit during its lifetime in reference to the initial delay of the uncompensated circuit.

Table 1
Impacts of upsizing the inverter PFET on the performance metrics.

Performance metric	Percentage of change @ $t = 0$ s (%)	Percentage of change @ $t = 10^8$ s (%)
Delay	−15.35	−0.176
Power	0.18	−27.54
UNG	−3.48	37.23

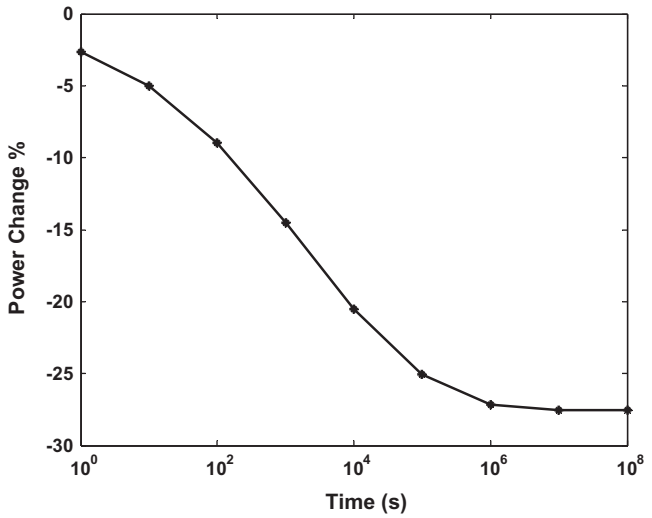

Fig. 7. Power change in the compensated circuit during its lifetime in reference to the initial power of the uncompensated circuit.

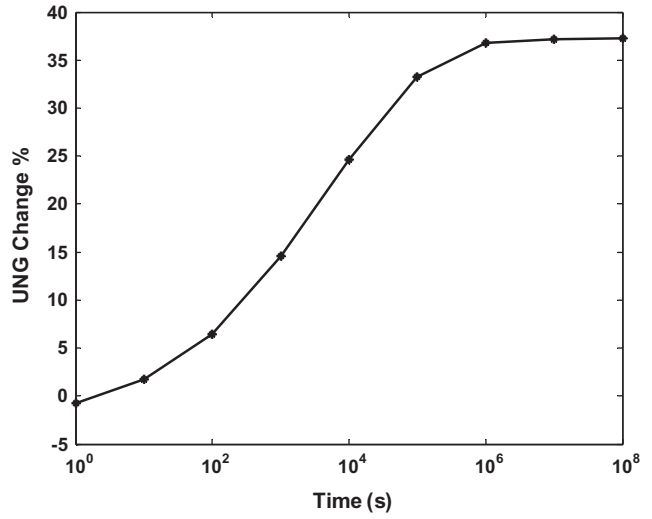

Fig. 8. UNG change in the compensated circuit during its lifetime in reference to the initial UNG of the uncompensated circuit.

Based on our analysis and simulation results, upsizing the output inverter PFET can be a successful NBTI/BPTI mitigating technique in domino logic with least area penalty. In a nominal domino circuit design, there will still be room for delay improvement, which may have not been exploited due to the associated metrics and constraints in the optimization process because the metric of optimization in high speed applications is not delay only and rather it is energy and delay product. It is noticeable that the same compensation can be used for longer circuit lifetimes due to the fact that the V_{th} degradation is almost saturated before 3 years as Fig. 1 shows. However, the overhead in area and the self-loading effect (which can occur when the intrinsic capacitance of the upsized transistor dominates the extrinsic load) can limit the effectiveness of this technique. In our circuit, the output node capacitance increases just about 1.423% by upsizing the inverter PFET and it has also a negligible impact on the dynamic node capacitance.

It is noticeable that speeding up the circuit may cause early mode timing failures (i.e. hold time failures). However, this can happen only on high-speed paths where the aging is not an issue. Hence only the logic gates on the critical path need to be overdesigned for a safe guard against the aging. If the high-speed paths experience early mode failure as a result of speed up of the critical path, it can be easily fixed by buffer insertion on high-speed paths to slow them down.

5. Conclusion

This paper presents comprehensive analyses on impacts of NBTI and PBTI on the main performance metrics of high-fan in domino gates based on PTM 32 nm high-*k* metal-gate technology models. It has been shown that due to the BTI-induced degradations, the circuit speed is decreased while the power and the UNG metrics are improved. Although the keeper transistor tends to decrease the delay, the pull-down network and the inverter PFET tend to increase the delay and have a dominant impact on the circuit delay. An NBTI/PBTI compensation technique is proposed based on upsizing just the inverter PFET. Upsizing this transistor makes the output transition faster and also helps reduce the contention between the keeper and the degraded pull-down network. We have shown that the long-term delay degradation can be mitigated with a negligible impact on other performance metrics at the expense of area.

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