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Recessed p-buffer layer SiC MESFET: A novel device for improving DC and RF characteristics

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ABSTRACT

This is the first report of novel structures designated as recessed p-buffer (RPB) silicon carbide (SiC) metal semiconductor field effect transistors (MESFETs). Important parameters such as gate–source capacitance, short channel effect, DC trans-conductance, cut-off frequency, DC output conductance, drain current and breakdown voltage of the two structures, the source side-recessed p-buffer (SS-RPB) and drain side-recessed p-buffer (DS-RPB), are simulated and compared with the conventional recessed gate SiC MESFET. Our simulation results describe that reducing the channel thickness under the gate at the source side of the SS-RPB structure, improves the gate–source capacitance, DC trans-conductance, and cut-off frequency compared with DS-RPB and conventional structures. Short channel effects for the SS-RPB structure are improved compared with that of the DS-RPB structure. Also, the SS-RPB structure has smaller DC output conductance in comparison with the conventional and DS-RPB structures. However, saturated drain current and breakdown voltage in the DS-RPB structure is larger than those in the conventional and SS-RPB structures.

1. Introduction

MESFETs are important for high speed and low noise communication systems. Current MESFET technologies are based on gallium arsenide (GaAs) and other compound semiconductors and their integration levels are modest when compared to ultra-large scale integration (ULSI) complementary metal oxide semiconductor (CMOS) and BiCMOS technologies. MESFET-based circuits would have a much wider application in the space and aeronautics fields if they could be manufactured using widely available CMOS technologies [1].

The absence of gate oxide makes the MESFET device naturally immune to oxide-related problems such as radiation plasma damages and hot-carrier effects. Besides, the channel of a metal oxide semiconductor field effect transistor (MOSFET) device is formed by the inversion layer at the gate oxide–silicon interface, thus carriers suffer from high normal fields and serious roughness scattering, leading to drastic reduction of effective mobility and trans-conductance. However, the channel of MESFET device is formed in the undepleted bulk region which is usually near the bottom of the active layer, thus carrier mobility is less degraded. This is one of the advantages for the MESFET devices against the MOSFETs. On the other hand, since the gate of MESFET is a metal–semiconductor Schottky contact, the voltage swing is limited within a relatively small range, depending on the barrier height. Hence, the MESFET is a good candidate for low-power applications [2].

The SiC MESFETs technology is a candidate for high power microwave applications. Its wide bandgap and high thermal conductivity offer several advantages compared to Si- and GaAs-based technologies. SiC MESFETs are very

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well-suited for high voltage, high power and high temperature applications due to its superior material properties especially high critical electrical field, high electron saturation velocity, and high thermal conductivity. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of 300–500 $cm^2/V\,s$, at doping levels of interest for MESFETs in the range of $1–5\times10^{17}\,cm^{-3}$. This drawback results in a larger source resistance and lower trans-conductance compared to GaAs based MESFETs [3–8].

For first time in this paper, recessed p-buffer SiC MESFETs in the source/drain sides are proposed to be aimed at improving device performance. Two device structures are proposed and investigated, namely source side recessed p-buffer (SS-RPB) and drain side recessed p-buffer (DS-RPB) SiC MESFET. SS-RPB has two regions under the gate that have different channel thicknesses. The region with narrower channel thickness is at the source side and will lead to a larger aspect ratio of the gate length to the channel thickness (L_g/a). It will be shown that this reduces short-channel effects such as drain-induced barrier lowering (DIBL). Also, this region improves the gate–source capacitance, maximum DC trans-conductance, cut-off frequency and DC output conductance compared to the conventional recessed gate structure. Similarly, in DS-RPB SiC MESFET the region with narrower channel thickness is at the drain side which improves the breakdown voltage and the region with wider channel thickness in the source side increases the drain current compared to the conventional recessed gate structure.

The unique features of the SS-RPB and DS-RPB SiC MESFET devices are explored and compared with those of a conventional recessed gate structure in terms of gate–source capacitance, short channel effects, DC trans-conductance, cut-off frequency, DC output conductance, breakdown voltage and saturated drain current. We demonstrate that the SS-RPB structure improves the gate–source capacitance, short channel effect, DC trans-conductance, cut-off frequency, and DC output conductance in comparison with the conventional and DS-RPB structures. But the DS-RPB structure has larger breakdown voltage and drain current than those in the conventional and SS-RPB structures.

2. Devices structures

Fig. 1(a), (b) and (c) shows the schematic cross-section of the SS-RPB, DS-RPB, and conventional [9,10] structures, respectively. The dimensions of the proposed structures are as follows: gate length $L_g=0.7\,\mu m$, recessed p-buffer layer depth to channel and recessed channel depth to the p-buffer layer are 0.05 μm, gate–drain spacing $L_{gd}=1\,\mu m$, gate–source spacing $L_{gs}=0.5\,\mu m$, channel thickness is 0.25 μm, and channel doping is $N_d=3\times10^{17}\,cm^{-3}$. The doping and thickness of the p-buffer layer are $1.4\times10^{15}\,cm^{-3}$ and 0.5 μm, respectively. The substrate is semi-insulating. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV. All the device parameters of SS-RPB structure are equivalent to those of the DS-RPB, except that the recessed p-buffer layer into the channel for the SS-RPB structure is at the source side while for the DS-RPB structure is at the drain side. The devices are simulated using two dimensional device simulator ATLAS software [11] with SiC material parameters [12–14].

3. Results and discussion

3.1. Gate–source capacitance

The dependence of the gate–source capacitance on the frequency for different recessed p-buffer lengths (L_{rpb}) in the DS-RPB and SS-RPB structures at $V_{GS}=0\,V$ and $V_{DS}=30\,V$ conditions is shown in Fig. 2. As is evident from this figure, the SS-RPB structure for different L_{rpb} has significantly smaller gate–source capacitance in comparison with conventional and DS-RPB structures, therefore, SS-RPB structure has better behavior in high frequency application. It is also clear in this figure that increasing L_{rpb} at the source side decreases the channel thickness near the source hence, the total channel charge decreases. Therefore, the gate–source capacitance reduces and consequently improves high frequency. The gate–source capacitance reduction with varying L_{rpb} from 0.2 μm to 0.35 μm in the SS-RPB structure is more than varying L_{rpb} from 0.35 μm to 0.5 μm. Because increasing L_{rpb} from 0.2 μm to 0.35 μm reduces the channel thickness under the gate at the source side while increasing L_{rpb} from 0.35 μm to 0.5 μm reduces the channel thickness under the gate at the drain side. Hence, it can be concluded that the channel thickness under the gate in the source side is an important factor in the gate–source capacitance. The minimum gate–source capacitance is obtained in the SS-RPB structure with $L_{rpb}=0.5\,\mu m$.

3.2. DC trans-conductance

The trans-conductance (g_m) of devices can be calculated by differentiating the drain–source current with respect to gate–source voltage at a constant drain–source voltage [15]:

$$g_m=\left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=const} \quad (1)$$

Fig. 3 shows the maximum DC trans-conductance as a function of L_{rpb} in the DS-RPB and SS-RPB structures at $V_{GS}=0\,V$ and $V_{DS}=10\,V$. In this figure, L_{rpb} is varied from 0.2 μm to 0.5 μm. The maximum DC trans-conductance with $L_{rpb}=0$ corresponds to the conventional structure. Simulation results in this figure demonstrate that the maximum DC trans-conductance for the SS-RPB structure is larger in comparison with the conventional and DS-RPB structure. Also, the maximum DC trans-conductance for the conventional structure is larger than that of the DS-RPB structure. The DC trans-conductance for the SS-RPB structure increases with increment of L_{rpb} from 0.2 μm to 0.35 μm at the source side. This is because of the dependence of drain current on the gate–source voltage increases due to the reduction of the channel thickness under the gate and therefore the g_m increases. Although, increasing L_{rpb} from 0.35 μm to 0.5 μm at the source side

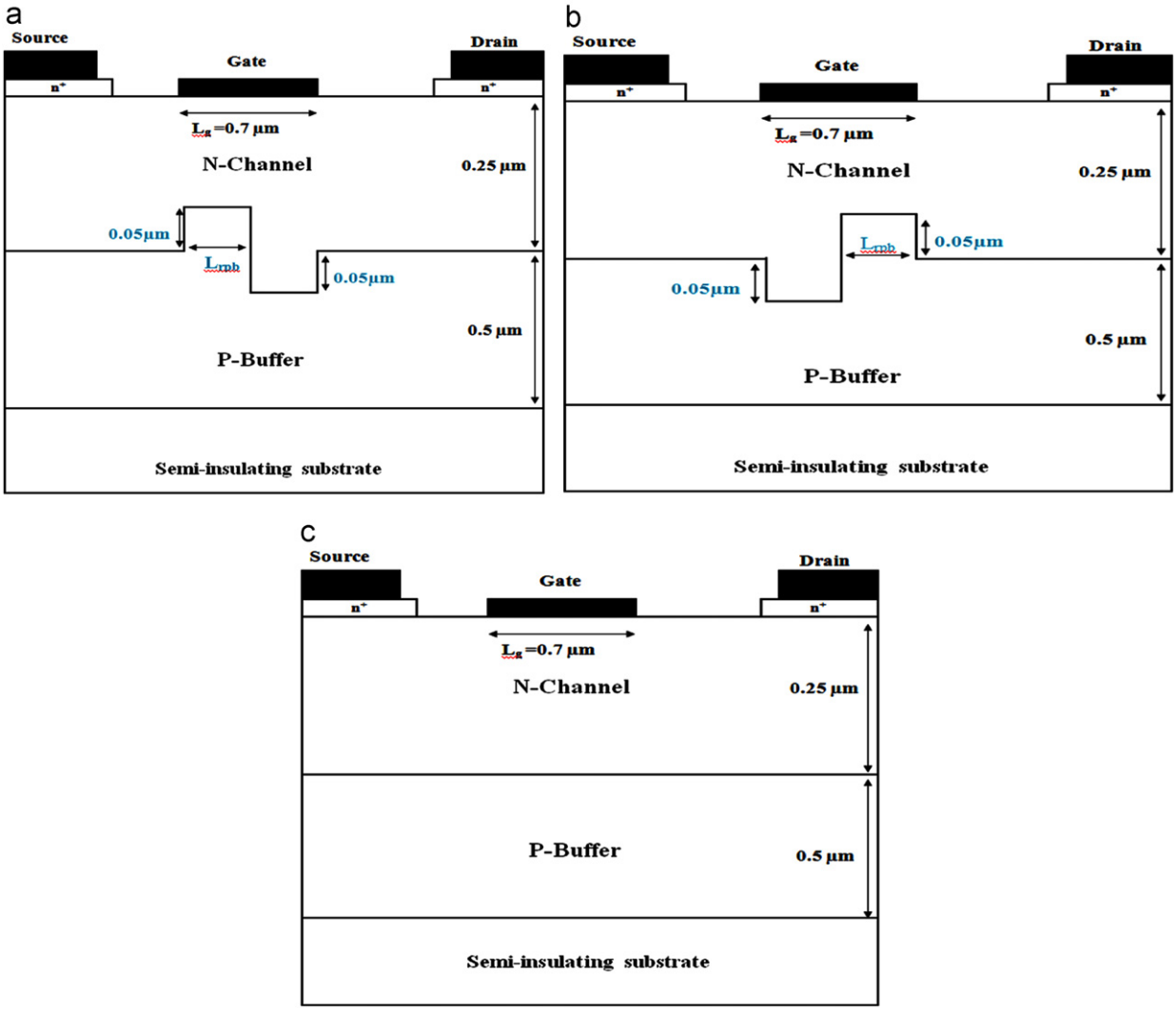

Fig. 1. Cross section of the (a) SS-RPB, (b) DS-RPB, and (c) conventional structures.

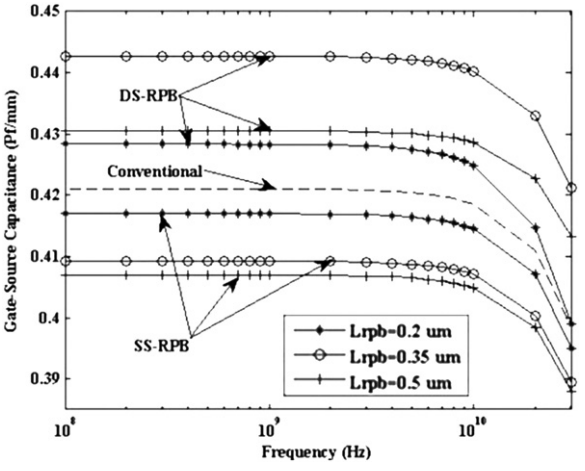

Fig. 2. Gate–source capacitance as a function of the L_{rpb} in the SS-RPB and DS-RPB structures at $V_{GS}=0$ V and $V_{DS}=30$ V.

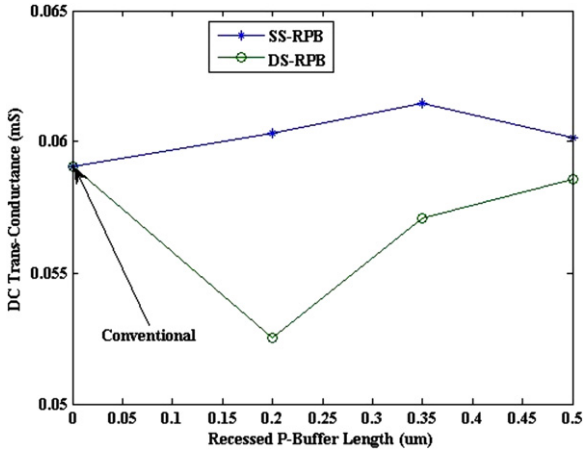

Fig. 3. Maximum DC trans-conductance as a function of the L_{rpb} in the SS-RPB and DS-RPB structures at $V_{GS}=0$ V and $V_{DS}=10$ V.

reduces the maximum DC trans-conductance slightly. This reduction is mainly due to the reduction of the drain current. The DC trans-conductance of the DS-RPB structure increases with increasing L_{rpb} from 0.2 μm to 0.5 μm.

3.3. Cut-off frequency

The cut-off frequency (f_T) can be calculated from Eq. (2) where g_m is the maximum DC trans-conductance and c_{gs} is the gate–source capacitance [16].

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2}$$

Eq. (2) shows that a larger g_m/C_{gs} ratio improves the f_T. It can be seen from Figs. 2 and 3 that the SS-RPB structure has larger g_m and smaller C_{gs} than the DS-RPB and the conventional structures. Therefore, the SS-RPB structure has larger g_m/C_{gs} ratio and consequently larger f_T compared to the DS-RPB and the conventional structures. Also, it is evident that a smaller channel thickness under the gate at the source side improves the high frequency performance of the devices.

3.4. DC output conductance

The output conductance (g_o) can be calculated by differentiating the drain–source current with respect to drain–source voltage with a constant gate–source voltage:

$$g_o = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{gs}\,=\,const} \tag{3}$$

Fig. 4 shows the DC output conductance as a function of L_{rpb} for the DS-RPB and SS-RPB structures at $V_{GS}=-1$ V and $V_{DS}=15$ V. According to this figure, the DC output conductance for the DS-RPB reduces with increasing L_{rpb}. This is because with increasing L_{rpb}, the channel thickness under the gate reduces which increases the vertical electric field by the gate–source voltage in the channel and this in turn reduces the drain current dependence to the drain voltage. The DC output conductance in the SS-RPB structure is smaller than that of the conventional structure. For the DS-RPB, the g_o is larger than that of the conventional structure. Therefore, the DC output conductance improves with increasing L_{rpb} in the SS-RPB structure.

3.5. Short channel effect

The device performance can be greatly improved by reducing the gate length to enhance the trans-conductance and reduce the gate capacitance. On the other hand as the technology is pushing the gate length to the sub-quarter micrometer range, short channel effects are becoming increasingly significant. One of the most pervasive short channel effects is the drain-induced barrier lowering (DIBL). The DIBL is an electrostatic effect causing the barrier between the source and drain of a field effect transistor (FET) in or near the sub-threshold region to be lowered when the drain voltage is increased. This effect causes the channel to return from a pinch-off state to conduct and shifts the threshold voltage. Consequently, the DIBL places a hard limit on the minimum gate size and degrades the trans-conductance and output conductance, which are critical to the gain and power output for a power FET and the noise margin for a digital FET [17,18].

Fig. 5 reveals that the negative shift in the threshold voltage with increasing drain voltage at a fixed L_{rpb} for the SS-RPB structure is less than that in the DS-RPB structure. For example, according to this figure the negative shift in the threshold voltage with increasing the drain voltage at a fixed L_{rpb} (0.35 μm) for the SS-RPB and DS-RPB structures are -5 V and -8 V respectively. In the SS-RPB structure, the channel thickness under the gate at the source side is reduced which will lead to a larger aspect ratio of the gate length to the channel thickness (L_g/a). This in turn increases gate control on the channel and therefore reduces short-channel effects such as drain-induced barrier lowering (DIBL). This is also the case for the DS-RPB structure, but reducing short channel effects for the SS-RPB structure is more evident. This implies that the impact of the channel thickness at the source side on

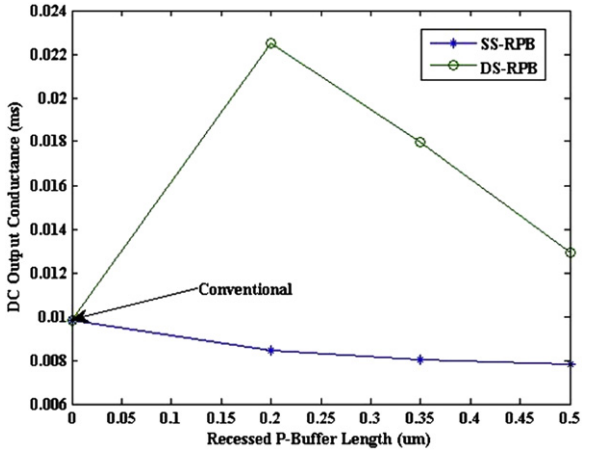

Fig. 4. DC output conductance as a function of the L_{rpb} in the SS-RPB and DS-RPB structures at $V_{DS}=15$ V and $V_{GS}=-1$ V.

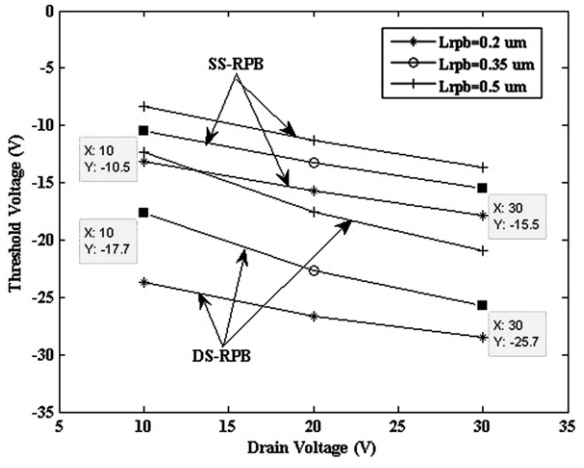

Fig. 5. Threshold voltage as a function of the drain voltage for different L_{rpb} in the SS-RPB and DS-RPB structures.

the short channel effects is larger than that of the channel thickness at the drain side. As can be seen from the figure, for both structures, a larger L_{rpb} at a fixed drain voltage increases the narrower channel region which decreases Shottcky barrier thickness, and therefore the threshold voltage increases.

3.6. Breakdown voltage

Fig. 6 shows the breakdown voltages of the SS-RPB and DS-RPB structures as a function of the L_{rpb} at $V_{GS}=-1$ V. The breakdown voltage of the DS-RPB structure for different L_{rpb} is larger than that of the SS-RPB and conventional structures due to the narrower channel at the drain side. Simulation results in Fig. 6 show that the breakdown voltage of the SS-RPB structure reduces with increasing L_{rpb} from 0.2 μm to 0.35 μm, while with increasing L_{rpb} from 0.35 μm to 0.5 μm, the breakdown voltage improves. This is because for large L_{rpb}, the channel at the drain side is also narrow [9]. Increasing L_{rpb} from 0.2 μm to 0.5 μm in the DS-RPB structure reduces the channel thickness at the drain side and therefore increases the breakdown voltage. Hence, the channel thickness at the drain side is an important factor in the breakdown voltage for the DS-RPB and SS-RPB structures.

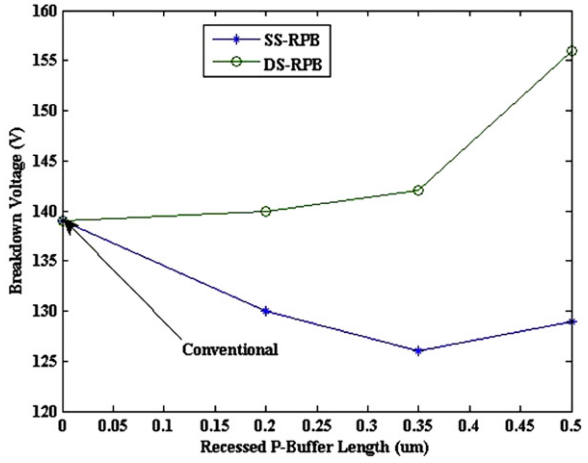

Fig. 6. Drain current as a function of the drain voltage for different L_{rpb} in the SS-RPB and DS-RPB structures at $V_{GS}=0$ V.

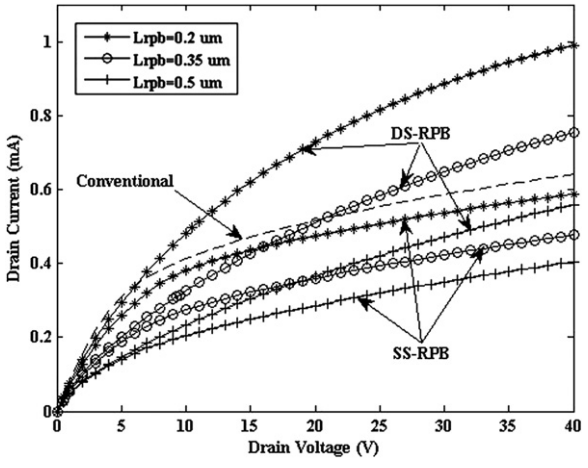

Fig. 7. Breakdown voltage as a function of the L_{rpb} in the SS-RPB and DS-RPB structures at $V_{GS}=-1$ V.

3.7. Drain current

Fig. 7 shows the simulated drain currents of the DS-RPB and SS-RPB structures at different values of L_{rpb} at $V_{GS}=0$ V conditions. As this figure shows, the drain current reduces with increasing L_{drg} from 0.2 μm to 0.5 μm for both structures. This is because a high drain current requires a large product of the channel doping and thickness ($N\times a$). When the recessed p-buffer length increases from 0.2 μm to 0.5 μm the region with narrow channel will increase and therefore the drain current will decrease. According to Fig. 5, at a fixed drain voltage, increasing the recessed p-buffer length causes a positive shift in the threshold voltage, which causes more overdrive voltage (Fig. 7 is depicted at $V_{GS}=0$). Therefore the drain current is increased.

It can be seen from Fig. 7 that drain currents for different L_{rpb} in the DS-RPB structure are larger compared to the SS-RPB structure. Therefore, the DS-RPB structure has higher saturated drain current in comparison with the SS-RPB and conventional structures.

4. Conclusions

DC and RF characteristics of the recessed p-buffer layer SiC MESFETs are simulated. The DC trans-conductance, gate–source capacitance, cut-off frequency, short channel effect, DC output conductance, breakdown voltage and drain current for both the SS-RPB and DS-RPB structures are studied in details. Our simulation results describe that the SS-RPB structure improves DC trans-conductance, DC output conductance, gate–source capacitance, cut-off frequency and short channel effect compared with conventional and the DS-RPB structures. However, the DS-RPB structure has larger breakdown voltage and saturated drain current than those in the SS-RPB and conventional structures. Therefore, the SS-RPB structure can be used in high frequency applications while the DS-RPB structure has higher output power density in comparison with the DS-RPB structure.

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