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A novel 4H–SiC MESFET with recessed gate and channel

S.M. Razavi [a,*], S.H. Zahiri [a], S.E. Hosseini [b]

[a] Department of Electrical Engineering, University of Birjand, Birjand, Iran
[b] Faculty of Engineering, Ferdowsi University of Mashhad, Mashhad, Iran

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ABSTRACT

New structures named as recessed gate and channel (RGC) silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are reported in this paper, in which the gate is recessed into the channel, and the channel is recessed into the p-buffer layer at the source and/or the drain side. Important parameters such as short channel effect, maximum DC trans-conductance (g_m), drain current, breakdown voltage and output resistance of the proposed structures are simulated and compared with the conventional 4H–SiC MESFET. Simulation results disclose that, compared to the conventional structure, the structure with recessed full gate and channel (FGC):

1. Improves the DC trans-conductance (g_m).
2. Increases the output resistance.
3. Enhances the breakdown voltage.
4. Reduces the short channel effect.

Moreover, source side recessed gate and drain side recessed channel (SG–DC) structure has higher g_m and output resistance in comparison with the conventional structure. Drain side recessed gate and source side recessed channel (DG–SC) structure has larger breakdown voltage and drain current than those of the conventional structure.

* Corresponding author. Tel./fax: +98 571 4411160.
E-mail address: m.136287@gmail.com (S.M. Razavi).

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1. Introduction

Silicon carbide metal semiconductor field-effect transistors (SiC MESFETs) are well suited for high power radio frequency (RF) applications, especially in extremely challenging environments, owing to their superior material properties. With the recent progress in SiC epitaxial material and the device process, excellent power and RF performances of SiC MESFETs have been reported [1]. The absence of gate oxide makes the MESFET device naturally immune to oxide-related problems such as radiation plasma damages and hot-carrier effects. Besides, the channel of a MOSFET device is formed by the inversion layer at the gate oxide–silicon interface, thus carriers suffer from high normal fields and serious roughness scattering, leading to drastic reduction of effective mobility and trans-conductance. However, the channel of MESFET device is formed in the undepleted bulk region which is usually near the bottom of the active layer, thus carrier mobility is less degraded. This is one of the advantages for the MESFET devices against the MOSFETs. On the other hand, since the gate of MESFET is a metal–semiconductor Schottky contact, the voltage swing is limited within a relatively small range, depending on the barrier height. Hence, the MESFET is a good candidate for low-power applications [2]. SiC MESFETs are very well-suited for high voltage, high power and high temperature applications due to its superior material properties especially high critical electrical field, high electron saturation velocity, and high thermal conductivity. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of 300–500 $cm^2/V\,s$, at doping levels of interest for MESFETs in the range of 1×10^{17}–$5 \times 10^{17}\ cm^{-3}$. This drawback results in a larger source resistance and lower trans-conductance compared to GaAs based MESFETs [3–9].

In order to improve the device performance of SiC MESFETs, various structures are proposed in the literature. Floating metal strips [7], recessed p-buffer layer [9], double recessed gate [10], multiple recessed gate [11], and un doped space barrier [12] are techniques to improve the device performance. In this article, with the purpose of improving the short channel effects, saturated drain current, breakdown voltage, DC trans-conductance and output resistance, new 4H–SiC MESFETs with recessed gate and channel (RGC) are proposed. In the following section, the proposed structures and the physical models used in the 2-D simulation are described in details. Also, in this section, fabrication feasibility of the proposed structures is investigated. In the third section, we first explain how the presence of the recessed gate and channel will reduce the short channel effects such as DIBL. Also, in this section the effect of recessed gate and channel on the drain current, electric field and breakdown voltage is studied in details. After that, the maximum DC trans-conductance and output resistance of the proposed structures are simulated and compared to that of conventional structure.

2. Device structure and fabrication feasibility

2.1. Device structure

Fig. 1a–d shows the schematic cross-section of the source side recessed gate–drain side recessed channel (SG–DC), drain side recessed gate–source side recessed channel (DG–SC), recessed full gate and channel (FGC) and conventional [9] structures respectively. The dimensions of the four structures are as follows: gate length $L_g = 0.7\ \mu m$, gate–drain spacing $L_{gd} = 1\ \mu m$, gate–source spacing $L_{gs} = 0.5\ \mu m$, channel thickness $T_C = 0.25\ \mu m$, and the channel doping $N_D = 3 \times 10^{17}\ cm^{-3}$. The doping and thickness of the p-buffer layer are $N_A = 1.4 \times 10^{15}\ cm^{-3}$ and $T_P = 0.5\ \mu m$, respectively. A compensation-doped (vanadium) semiconductor is used for semi-insulating substrate. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV and aluminum is used for the source/drain contacts. For all of the structures, recessed gate depth into channel and recessed channel depth into p-buffer layer are 0.05 μm. Recessed gate and channel length for SG–DC and DG–SC structures are 0.35 μm, but, recessed gate and channel length for FGC structure is 0.7 μm. The devices are simulated using two dimensional device simulator ATLAS software [13] with SiC material parameters [14–16]. In order to achieve more realistic results, several models are activated in simulation, including the 'SRH' model for Shockley–Read–Hall recombination, the 'Conmob' model for standard concentration dependent mobility, the 'Fldmob' model for parallel electric field-dependent mobility, the 'Fermi Dirac' model for statistics and the 'Impact Selb' model for impact ionization [17].

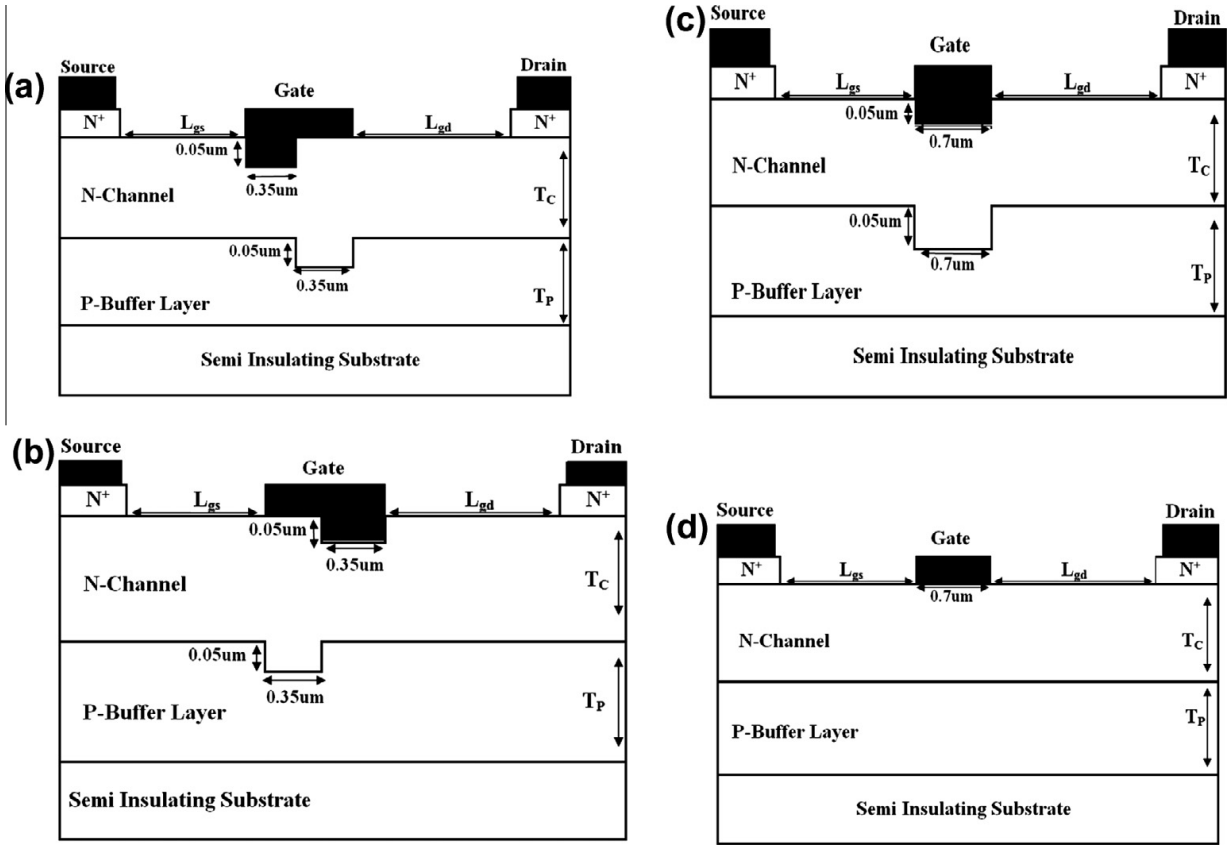

Fig. 1. Cross section of the (a) SG–DC, (b) DG–SC and (c) FGC and (d) conventional structures.

2.2. Fabrication feasibility

It is worth noting that the conventional structure can be fabricated using based on the procedure of [18]. Also, the FGC, SG–DC and DG–SC structures can be fabricated using the same procedures as reported in [18,19]. The recession of the channel into the p-buffer layer n-type region with the doping concentration of 3×10^{17} cm^{-3} can be produced with the same procedure used to form highly doped n-type source and drain regions in [18] with ion implantation and activation process as follows: high-temperature and multiple-energy ion-implantation with phosphorous can be performed. A thick SiO_2 layer can be used as a mask for implantation, and a thin SiO_2 layer can be used to protect the surface of the implanted region. Activation of the implanted ions can be achieved by inductively heating at a desired time and temperature in an Ar atmosphere. A sacrificial oxide layer, which is formed with consuming thin contaminated surface and is removed during etching process, plays an important role both to passivate the substrate surface and to achieve a controlled interface between the substrate and the contact metal. A thin thermal SiO_2 layer as sacrificial layer, and then a thick SiO_2 layer can be deposited by plasma enhanced chemical vapor deposition (PECVD).

To create the recessed gate in the channel, the recessed gate area of the transistors can be fabricated as reported in [19] as follows: First, a thermal oxide is grown on top of the channel area. An opening where the recessed gate should be placed is etched through this oxide and continued down into the 4H–SiC channel. This step defines the gate length, and the drain current of the device could be determined by the etch depth into the SiC channel. Second, the Nickel gate is deposited on top of the opening.

3. Results and discussion

The device performance can be greatly improved by reducing the gate length to enhance the transconductance and reduce the gate capacitance. On the other hand as the technology is pushing the gate length to the sub-quarter micrometer range, short channel effects becomes increasingly significant.

One of the most pervasive short channel effects is the drain-induced barrier lowering (DIBL). DIBL is an electrostatic effect causing the barrier between the source and drain of a field effect transistor (FET) in or near the sub-threshold region to be lowered when the drain voltage is increased. This effect causes the channel to return from a pinch-off state to the conduction state and shifts the threshold voltage. Consequently, the DIBL places a hard limit on the minimum gate size and degrades the trans-conductance and output conductance, which are critical to the gain and power output for a power FET and the noise margin for a digital FET [20,21]. As is depicted in the Fig. 2, negative shift in the threshold voltage with increasing the drain voltage of the FGC structure is less than those in the SG–DC, DG–SC and conventional structures. This is due to larger recessed gate length of the FGC compared to other structures that increases the vertical electric field by the gate–source voltage in the channel. With increasing vertical electric field of the gate in the channel, carrier transport in the channel is significantly affected by the gate–source voltage. This in turn reduces the carrier transport dependence to the lateral electric field by the drain–source voltage in the channel and then reduces the short channel effects such as DIBL. As can be seen in this figure, the negative shift in the threshold voltage with increasing the drain voltage for FGC and conventional structures are -4 V and -5.4 V respectively. It is clear from this figure that the recessed gate in the source side of the SG–DC structure has more effect than the recessed gate in the drain side of the DG–SC structure to reduce the short channel effects. This is because the SG–DC structure increases the aspect ratio of the gate length to the channel thickness (L_g/a) in the source side while the DG–SC structure reduces the (L_g/a) in the drain side. Negative shift in the threshold voltage in the DG–SC structure is more than those in the other structures. It is worth noting that we determine the threshold voltage of a MESFET from a conventional definition involving an abrupt transition between turn-on and turn-off operations [21].

To allow for high drain current in a MESFET, a large product of the channel doping and thickness ($N \times a$) is required [9]. Fig. 3 shows the drain current with respect to the drain voltage for SG–DC, DG–SC, FGC and conventional structures at $V_{GS} = -1$ V. As is evident from this figure, the DG–SC structure has larger saturated drain current compared to other structures. This is because in the DG–SC structure, the recessed gate is located in the drain side and recessed channel is placed in the source side. Therefore, in this structure channel thickness in the source side is larger than that at drain side. The SG–DC structure has smaller channel thickness at source side in comparison with the other structures and therefore has smaller saturated drain current. It can be concluded that the channel depth under the gate in the source side has a significant effect on the drain current.

It is important to understand the breakdown mechanism in SiC MESFETs since the breakdown is a major factor limiting the output power. Though many mechanisms have been identified in the past

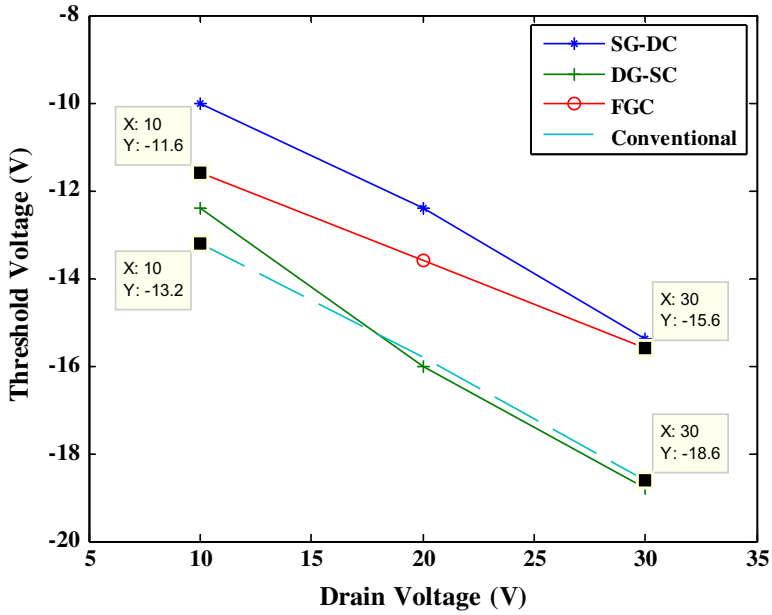

Fig. 2. Threshold voltage as a function of the drain–source voltage for four structures.

two decades, it is generally accepted that the gate/drain avalanche mechanism is the physical cause of high field breakdown [22]. A further investigation shows that the breakdown happens at the gate corner near the drain due to the electric field crowding [9,10,23]. It is well known that there is a critical electrical field in the semiconductor material of the channel. The maximum electric field in the channel is increased by enlarging the drain–source voltage at the gate corner of nearing the drain. When the electric field is reached to the critical electric field at the gate corner near the drain, the applied drain–source voltage is considered as the breakdown voltage. In our simulations, to find the breakdown voltage, we have activated the Impact Selb model for impact ionization and then we can reveal the breakdown voltage from the drain current with respect to the drain–source voltage curve. The breakdown voltage of the four structures are shown in the Fig. 3 at $V_{GS} = -1$ V. As can be seen in this figure, the DG–SC structure has a larger breakdown voltage compared with the other structures. This is because, this structure has a recessed gate at the drain side that reduces the channel thickness under the gate near the drain and consequently reduces the maximum lateral electric field at that place compared to the other structures. Therefore, this structure can reach to the critical electric field at a larger drain–source voltage and consequently has a larger breakdown voltage. The breakdown voltages of the SG–DC, DG–SC, FGC and conventional structures are 121 V, 172 V, 168 V and 142 V respectively. Simulation results in Fig. 4 show the maximum lateral electrical field of the four structures at the gate corner near the drain at $V_{DS} = 120$ V and $V_{GS} = -1$ V. Comparing Figs. 3 and 4 reveals that the breakdown voltage improves with decreasing the maximum lateral electrical field at gate corner in the drain side. The maximum lateral electric field of the DG–SC and FGC is less than those in the SG–DC and conventional structures. Therefore, the DG–SC and FGC structures have bigger breakdown voltage compared to the SG–DC and conventional structures. The DR-MESFET investigated in [11,12] has the same structure as SG–DC in this paper. Comparing electric field and breakdown voltage results of this paper with those reported in [11,12] shows that the breakdown voltage improvement in this paper is more than that in the [11,12]. This is because in this paper the breakdown voltage is improved from 121 V in the SG–DC structure to 172 V of DG–SC structure. In [11], the breakdown voltage is improved from 105 V to 116 V. Also, as can be seen in [12], the breakdown voltage is increased from 109 V to 144.5 V.

The DC trans-conductance (g_m) of a transistor can be calculated by differentiating the drain current with respect to the gate–source voltage at a constant drain–source voltage [24]:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=const} \tag{1}$$

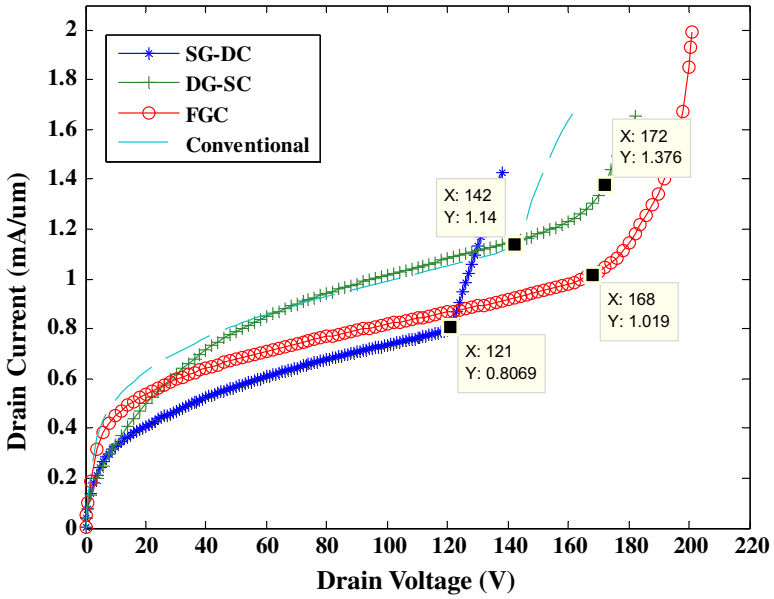

Fig. 3. Drain current as a function of the drain–source voltage for four structures at $V_{GS} = -1$ V.

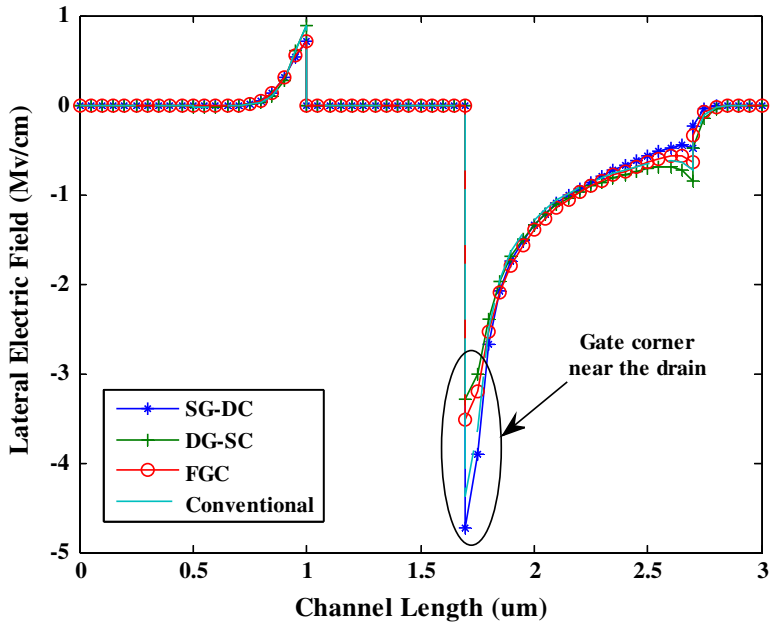

Fig. 4. Electric field distribution in the channel at $V_{GS} = -1$ V and $V_{DS} = 120$ V for different structures.

The DC trans-conductance shows the drain current dependence on the gate–source voltage at a constant drain–source voltage. Fig. 5 provides a comparison between maximum DC g_m for different structures. In this figure, it is illustrated that the SG–DC structure has superior g_m than those in the other structures for different drain voltages. The DG–SC structure has less g_m compared to other structures for different drain voltages. It can be concluded that reducing the channel depth at the source side under the gate, improves the maximum g_m. This is because reducing the channel thickness under the gate at the source side increases the vertical electric field imposed by the gate–source voltage in the channel and therefore increases the drain current dependence on the gate–source voltage [9]. The least g_m in Fig. 10 of [11] obtain for MR-MESFET with $N = 1$ (DR-MESFET). Increasing N improves the g_m in this figure. The g_m of SG–DC in this paper is bigger than that in other structures. Since the DR-MESFET in [11] is the same as SG–DC structure, it can be concluded that the MR-MESFETs ($N = 2, 3, 4$) in [11] have larger g_m than that of reported in this paper.

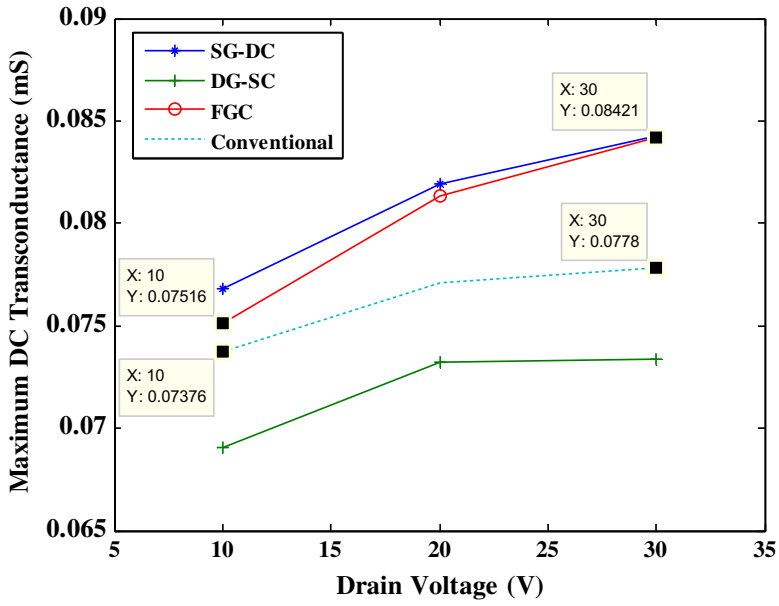

Fig. 5. Dependence of the maximum DC trans-conductance on the drain–source voltage for SG–DC, DG–SC, FGC and conventional structures at $V_{GS} = 0$ V.

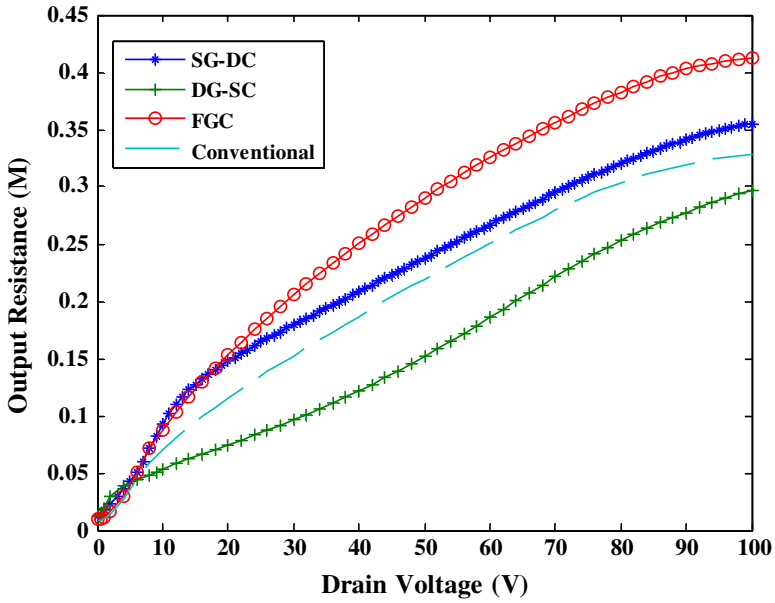

Fig. 6. Output resistance with respect to the drain–source voltage in the four structures at $V_{GS} = -1$ V.

The output conductance (g_o) can be calculated by differentiating the drain–source current with respect to the drain–source voltage at a constant gate–source voltage:

$$g_o = \frac{\partial I_D}{\partial V_{DS}}\bigg|_{Vgs=const} = \frac{1}{r_o} \tag{2}$$

Fig. 6 shows the output resistance with respect to the drain–source voltage at $V_{GS} = -1$ V for different structures. As is obvious from this figure, the output resistance in the FGC structure is larger than those of the other structures, and DG–SC structure has the lowest r_o. It can be concluded from Fig. 6 that reducing channel thickness under the gate in the source side, increases the output resistance.

4. Conclusions

Recessed gate and channel 4H–SiC MESFETs with recession in the source/drain sides are proposed in this work. Breakdown voltage, short channel effect, drain current, output resistance and the maximum DC trans-conductance for SG–DC, DG–SC, FGC and conventional structures are simulated and compared. Simulations describe that FGC structure has better performance in terms of reducing short channel effect such as DIBL than the other structures. Also, the FGC structure enhances g_m, output resistance and breakdown voltage compared to the conventional structure. The SG–DC structure has the best g_m among the simulated structures. The breakdown voltage and saturated drain current in the DG–SC structure is better than those of the other structures.

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