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A New Design Technique for Low Power Subthreshold Logic Circuits with Enhanced Robustness Against Process Variations

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***Abstract*— Designing logic circuits in the subthreshold regime is one of the most effective ways to reduce the power consumption of digital circuits. In the subthreshold region, the current is an exponential function of the threshold voltage and the behavior of transistors is more susceptible to process variations. In this paper, we present a new design technique that helps reduce the impact of process variations on the circuit. The proposed technique is implemented on the staticC2MOS flip-flop and the flip flop is used in a shift register. The circuit is simulated in the 90nm CMOS technology using a 0.2V supply voltage. Simulation results show that the robustness of the circuit is improved while the power consumption and the area are kept at minimum.**

I. INTRODUCTION

In the past decade the demand for low power electronic circuits has increased dramatically. This is mainly due to the growth of portable equipments, laptops, and biomedical implantable devices. In most of these devices digital circuits form the main part of the IC and consume a considerable amount of power. Hence, reducing the power consumption of digital circuits is very important. Several techniques, e.g. voltage scaling and clock gating; for low power design of digital circuits have been proposed so far [1-4]. However, in some applications, the power consumption should be extremely low while the speed is not the primary concern. In these applications more aggressive methods for power reduction are required. Reducing the supply voltage is the most effective technique. Subthresholddigital circuits in which the supply voltage is lowered below the threshold voltage of transistors are becoming more attractive in extremely low power applications.

While the power consumption of subthreshold circuits is very low, the circuits are very susceptible to process variations. This is due to the fact that the drain current is an exponential function of the threshold voltage[4,5]. Hence, the process variations cause the circuit to cease working correctly.

In order to tackle this problem, techniques at the device level as well as circuit level have been proposed. In [5] techniques at the device level are proposed to reduce the impact of process variations. It is concluded that new devices like double gate silicon-on-insulator transistor are better candidates for subthreshold static CMOS and pseudo NMOS circuit design in terms of insensitivity against process variations. However, using this technique would be expensive.

In [4] and [6] techniques at the circuit level are proposed to increase the stability of the circuit against process variations. In [4] two techniques, i.e. CMOS with variable threshold voltage (VT-sub-CMOS) and CMOS with dynamic threshold voltage (sub-DTMOS), are proposed. The VT-sub-CMOS requires an auxiliary circuit to stabilize the circuit against process variations. This auxiliary circuit should be designed very precisely. The sub-DTMOS does not need any auxiliary circuit but it should be implemented in a triple-well technology.

In [6] a new topology, called Subthreshold Source Couples Logic (STSCL) is introduced. It is shown that this topology is suitable, in terms of PDP, for supply voltages between 0.3V and 0.6V.This technique does not use the maximum achievable speed of the circuit.

In this paper we present a new circuit design technique which leads to more robust circuits against process variations. In the proposed technique, the circuit is designed with the lowest possible power consumption which meets the desired specifications using the typical device models. Then the circuit is examined in other process corners to see in which corner the circuit fails to operate and to find the root cause of the failure. Some auxiliary transistors are added to the circuit to make it work in the problematic corners. These extra transistors become active only when the circuit goes into those corners. Using this technique the overall power consumption and the area is kept at minimum while it is guaranteed to operate in all process corners.

The paper is organized as follows. In section II the impact of process variations on the subthreshold current and sizing of transistors in subthreshold digital circuits are discussed. In section III the impact of process variations on the performance of digital circuits are discussed and it will be shown how the power consumption and area of the circuit are

increased if the circuit is to be able to operate in all process corners. In section IV the proposed method to tackle the problem of process variations is introduced and simulation results are provided. Conclusions are drawn in section V.

II. SUBTHRESHOLD CURRENT VARIATIONS

The drain current of an NMOS in the subthreshold region is given by the following equation [7].

$$I_{sub-th} = I_0 \times I_1 \quad (1)$$

$$\begin{cases} I_0 = \mu_0 C_{ox} \dfrac{W}{L}(n-1)V_t^2 \\ I_1 = e^{\left[\frac{V_{GS}-V_{TH}}{nV_t}\right]} \end{cases}$$

Where Vt=KT/q is the voltage equivalent of temperature (approximately 26mV at room temperature), VTH is the threshold voltage of the transistor, n is the subthreshold slope factor $\left(1+\frac{C_d}{C_{ox}}\right)$.

As can be seen in the above equation, the subthreshold current has an exponential dependence on the threshold voltage. Many factors affect the VTH and they typically change during fabrication of the IC. Hence, process variations have a strong impact on the overall performance of subthreshold circuits. This impact is less for transistors operating in the strong inversion region since the current has a quadratic dependence on VTH. In circuit simulators like HSPICE the impact of process variations can be examined by simulating the circuit in different process corners, i.e. TT, SS, FF, SF, FS corners. Simulations in the 90nm CMOS technology shows that the threshold voltage of PMOS and NMOS transistors changes by more than 48% in different process corners. This amount of VTH variations leads to a much larger change of subthreshold current due to the exponential relationship between VTH and current.

of the important parameters that affect the subthreshold current is the length of the transistor (L). According to equation (1) I0 is inversely proportional to L. Hence, by increasing L the current decreases. However, in modern technologies L changes the threshold voltage as well and by increasing L, VTH decreases. A lower VTH leads to a higher current according to equation (1). Therefore, the subthreshold current can be either decreased or increased by L. Fig. 1 shows the variation of VTH with respect to L in the 90nm CMOS technology. As can be seen in this figure, as L increases VTH decreases quite rapidly for small values of L but the change of VTH becomes smaller for larger values of L. For L more than 700nm the variation of VTH becomes negligible. Hence, in order to increase the maximum subthreshold current of the transistor it is better to increase L and W (note that W should be increased to keep the W/L ratio constant). However, larger values of L and W make the circuit to take a large area.Therefore, the impact of L should be carefully taken into account in designing subthreshold digital circuits and choosing the minimum value for L is not the best choice. For many practical cases L can be chosen around 300nm.

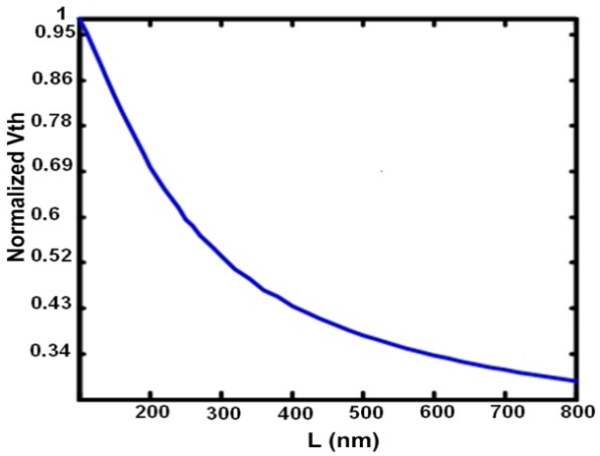

Figure 1.The normalized VTH vs L.

III. SUBTHRESHOLD C2MOS D FLIP-FLOP

In order to see the effect of process variations on the performance of subthreshold digital circuit we consider the static C2MOS D Flip-Flop (DFF). The circuit of the flip flop is shown in Fig. 2. This flip flop is not sensitive to the overlap of clkand clkb [8]. The schematic of the clocked inverters in this flip flop is also shown in Fig. 2. In order to check the operation of the flip flop of Fig. 2, we have used it in an 8-bit shift register as shown in Fig. 3. Since each DFF is connected to another DFF with exactly the same circuit, each of the clocked inverters I1 and I2 of the DFF in Fig. 2 is connected to another clocked inverter.

In the shift register of Fig. 3, if a 1 enters the register, after 8 clock cycles it should appear at the final output. The shift register is simulated by HSPICE in 90nm CMOS technology. The simulations are done at all process corners. In these simulations the supply voltage is 0.2V. In order to keep the area at minimum, the size of all transistors are chosen to be (W/L)n,p=120nm/100nm. This sizing is close to the minimum sizes that can be chosen in the 90nm technology. Fig. 4 illustrates the clock, the input of the shift register and the output of the final DFF for two process corners, i.e. TT and SS. As can be seen in Fig. 4, for the TT model the shift resister works properly at the clock frequency of 20MHz and after 8 clock cycles the 1 appears at the output. However, for the SS corner the shift register fails to work. This is because the threshold voltage of transistors increases in the SS corner and the current decreases. Hence, the delay of the DFFs increases and the shift register cannot follow the input. The power consumption of the shift register at all process corners is shown in Table 1. This table also shows an approximation of the area taken by the shift register. For calculating the area only the W and L of individual transistors are taken into account.

It is possible to modify the DFFs to make them work in all process corners, including the SS corner. In order to do this we should change the sizesof transistors of I1 and I2 inverters to increase the current they can provide so that nodesX and OUT in Fig. 2can be charged or discharged fast enough. The

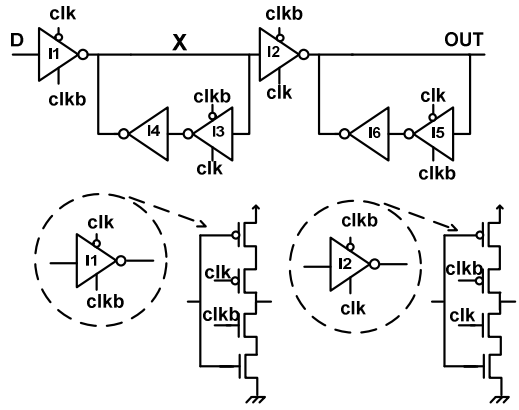

Figure 2. The C2MOS D Flip Flop.

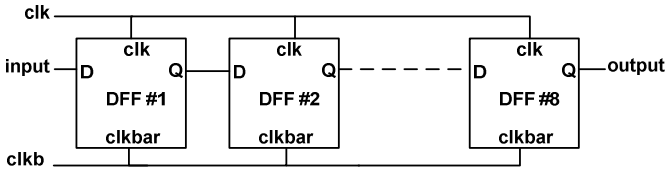

Figure 3.An 8-bit shift register as a test bench for the flip flop.

modified I1 and I2 inverters have transistor sizes of W/L=500nm/500nm. Note that the ratio of W and L of the transistors is almost one and it seems that the current capability of transistors should not be increased. However, we should note that increasing L reduces the threshold voltage and the current of transistors increases exponentially.The shift register of Fig. 3 with these new transistor sizes is simulated in the 90nm CMOS technology. The shift register operates correctly in all process corners. However, the power consumption and the area increase. Table 2 shows the power consumption of the shift register. Comparing the values of this table to that of Table 1 makes it clear that in all process corners the power consumption has increased by at least a factor of 2.Similar to Table 1, the area of the shift register is also shown in Table 2. As can be seen the area of the shift register has also increased considerably.

The above discussion makes it clear how the power consumption and area increases if the circuit is to be designed in such a way that it works in all process corners. This increase of power consumption is not desirable especially in extremely low power subthreshold circuits. In the next section we propose a new subthreshold circuit design technique that leads to a circuit that operates in all process corners but the power and area penalty is lower than the traditional design technique.

TABLE 1: POWER CONSUMPTION OF THE 8-BITS SHIFT REGISTER WITH D FLIP-FLOP OF FIG. 2@ F=20MHZ,VDD=0.2V & A=1.

corner	TT	FF	FS	SF	SS
Power(nW)	22	73	23	25	Doesn't work
Approximate area	1.92μm^2				

TABLE 2: POWER CONSUMPTION OF THE 8-BITS SHIFT REGISTER WITH MODIFIED D FLIP-FLOPS @ F=20MHZ,VDD=0.2V & A=1.

Corner	TT	FF	FS	SF	SS
Power(nW)	58	145	61	62	37
ApproximateArea	17.792um^2				

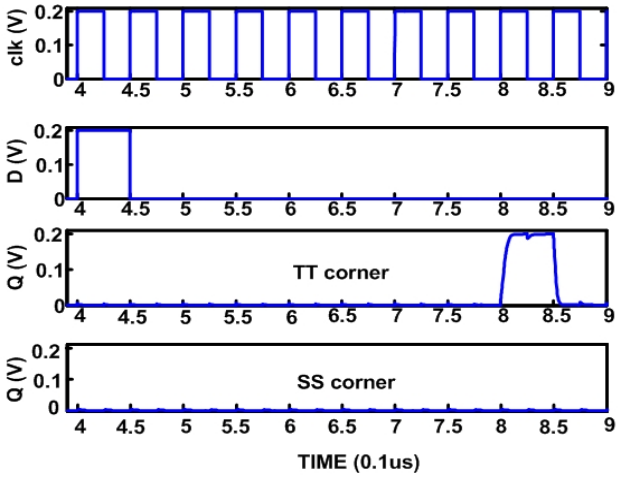

Figure 4.Input and output of the shift register at TT and SS process corners.

IV. THE PROPOSED DESIGN TECHNIQUE

As we saw in the previous section, we can design the digital subthreshold circuit with minimum power and area. However, in order to make sure it will work in all process corners we have to increase the power consumption and area. In this section we propose a new design technique that can ensure the correct operation in all process corners while the extra power and area we have to pay for the reliability of the circuit is lower.

The proposed technique will be explained on thestatic C^{2}MOS DFF in Fig. 2. As explained in the previous section, in order to make the DFF work in all process corners one can increase the size of *I1* and *I2* inverters. Instead of this, we add two extra inverters in parallel to *I1* and *I2* as shown in Fig. 5. These two added inverters (*Ie1* and *Ie2*) turn on only when the circuit goes into the SS corner. The control signals, cc and cb, are set or reset when the IC is being tested. If the circuit goes into the SS corners cc=1 and cb=0. In other corners cc=0 and cb=1. In this wayif the circuit is fabricated in the TT, SF, FS, and FF corners only *I1* and *I2* inverters drive the *X* and *OUT* nodes. In this case the auxiliary inverters (*Ie1* and *Ie2*) are not working and the outputs of *Ie1* and *Ie2* are float and It is worth mentioning that although the auxiliary inverters are not active in TT, SF, FS, and FF corners, but they increase the capacitive load on *X* and *OUT* nodes. This leads to an increase in power consumption and delay compared to the DFF where the auxiliary inverters are not added.

The control signals, cc and cb,can be hard wired after testing the IC and finding the process variations. It is also possible to design a suitable circuit to automatically generate

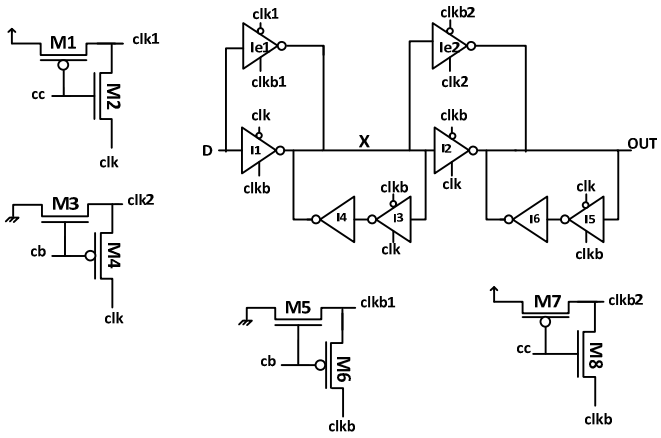

Figure 5.The proposed static C2MOS DFF.

these control signals. The extra circuit for generating these signals do not increase the overall power consumption considerably since it constitutes a small block in the whole IC.

The 8-bit shift register of Fig. 3 with the proposed static C^2MOS DFFs of Fig. 5 is simulated in the 90nm CMOS technology using HSPICE. The supply voltage is chosen to be 0.2V so that the circuit operates in the subthreshold region. The clock frequency is 20MHz. Table 3 shows of transistor sizes for the proposed DFF. The simulations are done in all process corners. The shift register works in all process corners. The power consumption and the area of the shift register are shown in Table 4.

Comparing Table 4 with Table 2 shows that the proposed technique can reduce the power consumption in all process corners except FF corner. In the FF corner the power consumption is almost the same as that of Table 2. Also, note that the area of the shift register is much lower than the previous circuit. This means that although two auxiliary inverters are added to the DFF the overall area is still lower than the previous circuit and the circuit consumes less power.

TABLE3: TRANSISTOR SIZES OF THE D FLIP-FLOP IN FIG. 5.

Size / inverter & transistors	$(W/L)_{n,p}$
I1,I2	(0.12um/0.25um)
Ie1,Ie2	(0.12um/0.25um)
I3,I4,I5,I6	(0.12um/0.1u)
M1,M2,M3,M4	(0.12um/0.1u)
M5,M6,M7,M8	(0.12um/0.14u)

TABLE4: POWER CONSUMPTION AND AREA OF THE 8-BIT SHIFT REGISTER WITH D FLIP-FLOP OF FIG. 5@ F=20MHZ&VDD=0.2V.

corner	TT	FF	FS	SF	SS
Power(nW)	34	146	40	45	21
ApproximateArea	5.9136um^2				

V. CONCLUSION

Process variations have a greater impact on the performance of digital subthreshold circuits compare to circuits operating in the strong inversion region. In order to make the subthreshold circuit to operate in all process corners typically the *W* and *L* of transistors are increased. This causes the circuit to consume more power and take more area. In this paper we proposed a new design technique for making the digital circuit to operate in all process corner which leads to lower power consumption and smaller area compared to the traditional method. The proposed technique was implemented on a C^2MOS DFF and is based on adding auxiliary inverters. The auxiliary inverters become active only when the circuit is fabricated in the problematic corner(s). The control signals should be provided during testing of the IC.

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