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This paper presents a new successive approximation analog to digital converter (SA-ADC) with wireless transmission which samples sparse signals in a non-uniform adaptive way and transmits the samples power-efficiently. The proposed SA-ADC changes the rate of sampling in accordance with the rate of changes of the signal and modified FSK and an OOK transmitter is used to eliminate sending extra time flags which are typically needed for synchronization during signal restoration in the receiver. In this way, the data volume is reduced considerably without losing the important information in the signal. Simulation results in the 0.18um CMOS technology shows a power saving of up to 90.5% and a compression ratio of 10.5 compared to the conventional sampling technique of ECG signals. View full abstract»

A New Power Efficient Wireless Non-Uniform Adaptive-Sampling ECG Recording System

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Abstract*—This paper presents a new successive approximation analog to digital converter (SA-ADC) with wireless transmission which samples sparse signals in a non-uniform adaptive way and transmits the samples power-efficiently. The proposed SA-ADC changes the rate of sampling in accordance with the rate of changes of the signal and modified FSK and an OOK transmitter is used to eliminate sending extra time flags which are typically needed for synchronization during signal restoration in the receiver. In this way, the data volume is reduced considerably without losing the important information in the signal. Simulation results in the 0.18um CMOS technology shows a power saving of up to 90.5% and a compression ratio of 10.5 compared to the conventional sampling technique of ECG signals.

I. INTRODUCTION

Bio-potential signals convey valuable information for diagnostic purposes. In many cases it is desirable to have a record of such signals for a relatively long period of time. This requires the electronic recording device to consume very little power and to have a relatively large memory to sample and save the signal for several days (or even weeks). Reducing the number of samples in the recording device is critical in the reduction of the memory size as well as the power consumption.

Fig. 1 illustrates a sample of an electrocardiography (ECG) signal. The main features of the ECG signal are shown by the P, Q, R, S, and T letters. As can be seen in this figure the waveform can be divided into regions of slow and fast transitions (corresponding to 'low activity' and 'high activity' regions in Fig. 1). The region around the QRS complex has the fastest transitions. In other regions the signal variations are moderate or slow. The required sampling rate depends on the harmonics of the QRS complex and the application. For example, the analysis of heart rate variations (HRV) requires high resolution of time for the detection of the R points. This demands a high sampling rate (250 Samples/s) [1]. Sampling the whole signal with this high rate increases the volume of data. In this case, many consecutive samples in the slow transition regions are almost the same and do not convey much information. If we can change the rate of sampling in accordance with the rate of signal variations, the data volume

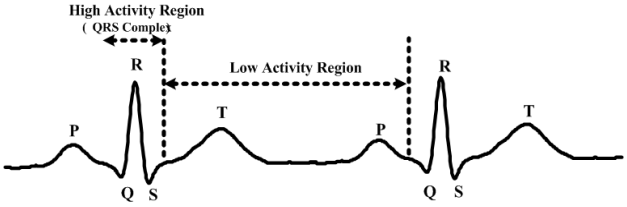

Figure 1. ECG waveform with inherent time-domain sparsity

can be reduced considerably without losing the important information in the ECG signal.

In order to reduce the volume of sampled data in a monitoring device, the bio-signal is typically sampled and converted to digital by an analog to digital converter (ADC) at the Nyquist rate or more. The sampled data is then compressed using compression technique to reduce the size of the memory needed to save the data [2-6]. In this method, although the size of data is reduced, the power consumption of the circuit prior to digitization is not decreased. If the reduction of the sampling rate happens during digitization, it can lead to lower power consumption in the analog part of the circuit. Hence, the technique that is used to reduce the number of samples should be compatible with the architecture of the ADC. In bio-implantable devices in which the sampled signal is to be transmitted out of the body, reducing the sampling rate is also desirable since it leads to lower transmitter power.

The successive approximation analog to digital converter (SA-ADC) is a good candidate for low to moderate sampling rates and can be designed to be very low power [2-7]. In this paper we propose a new SA-ADC which implements a non-uniform adaptive sampling technique. Using this non-uniform adaptive sampling SA-ADC and modified wireless transmission the data volume can be reduced for sparse bio-signals like ECG while the power consumption is also decreased. In section 2 of this paper the system architecture and the proposed non-uniform adaptive sampling algorithm are presented. In section 3, the proposed SA-ADC is discussed. The proposed data transmission is presented in section 4 and simulation results are provided in section 5. We finally conclude the paper in section 6.

II. SYSTEM ARCHITECTURE

Fig. 2 presents the biomedical signal recording architecture proposed in this paper. The weak bio-signals are first pre-amplified and band-pass filtered. The preconditioned signals are then delivered to non-uniform adaptive-sampling successive approximation ADC (SA-ADC) in order to be digitized. These bits, prepared by SA-ADC, are packaged into data packets to be sent to the outside world serially. A modified radio-frequency frequency-shift-keyed (FSK) transmitter mixed with on-off-keying (OOK) transmitter is used for transmitting the data. The main advantage of this architecture over conventional uniform recording systems is the saved power and data volume resulted from non-uniform adaptive sampling technique which this would lead to transmitting lower data and ability to turn off the transmitter for a long period of transmit time. The signal processing of the external side was implemented in software.

A. The Non-Uniform Adaptive Sampling Technique

In this section we present the proposed non-uniform adaptive sampling technique. In this method, sampling is done based on the activity of the signal. The system has two clock signals CLK_H and CLK_L with frequencies f_H (the high sampling frequency) and f_L (the low sampling frequency), respectively. For the sake of illustration, Fig. 3 shows a typical ECG signal sampled with this technique. As can be seen the ECG signal is composed of regions with slow and fast variations. This figure shows the two clocks used in the sampling system. The signal is monitored at a rate determined by CLK_H to detect the rate of change of the signal. During the fast transition regions the signal is sampled by f_H and during the slow transition regions the signal is sampled by f_L. The CLK_{sample} in Fig. 3 is the overall clock which represents the sampling instants. Clearly, the sampling rate is changing based on the rate of variation of the ECG.

An important issue in the proposed technique is how to detect the fast and slow transition regions. For which the procedure of the proposed sampling technique is explained as follow. Let T_H and T_L be the period of CLK_H and CLK_L, respectively. We also define m as the ratio of T_L to T_H ($m=T_L/T_H$) and $V_{DAC(PS)}$ as the value of the last sampled signal (i.e. the last digital code converted to analog by a digital to analog converter).The sampling algorithm starts by initializing the value of $V_{DAC(PS)}$. The input signal at time nT_H ($V_i(n\times T_H)$) is compared with $V_{DAC(PS)}$. If the absolute value of the difference is not larger than a threshold value (V_{th}), then the signal variation has not been fast enough and the signal is not sampled. However, if the time interval between $n\times T_H$ and the last sampling instant is equal to T_L the signal should be sampled. If the absolute value of the above difference is larger than V_{th} then the signal variations has been fast enough and the signal is sampled. The value of the $V_{DAC(PS)}$ is also updated for the next sampling. Note that the signal is being monitored by f_H, however, it is not necessarily sampled with this frequency. In fact the sampling is done at a rate whose average is more than f_L and less than f_H. To obtain the best results in terms of the lowest distortion in the recovered signal and not losing important information of the signal, the three parameters f_L, f_H, and V_{th} should be chosen carefully. f_H is typically chosen large enough so that the highest frequency harmonic present in the signal can be sampled properly (at least the Nyquist rate of the signal). This can be obtained from the Short Time Fourier Transform (STFT) [8]. f_L is chosen based on the frequency contents of the P and T waves of the ECG [1]. Therefore, we have chosen a low (f_L) and a high (f_H) sampling rate, 62.5 Hz and 1 KHz for this design respectively. We have obtained the best value for V_{th} based on system level simulations using MATLAB, as explained in [9].

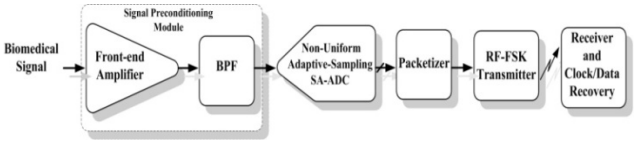

Figure 2. Block diagram of the proposed architecture

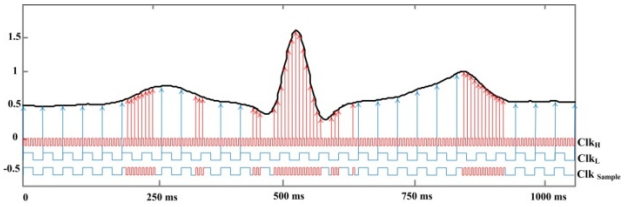

Figure 3. A cycle of ECG signal sampled with the proposed technique.

III. THE NON-UNIFORM ADAPTIVE-SAMPLING SA-ADC

The technique presented above has the ability to be incorporated in an SA-ADC easily. The SA-ADC is suitable for slow to moderate sampling rates and low power applications. Hence, it is a good choice for bio-medical applications [6-7]. Moreover, in an SA-ADC before a sampling starts the analog value of the previous sample is saved on the capacitors of its DAC. This is what we need in the proposed technique. Also, the addition and subtraction of the V_{th} can be accomplished in the digital control block of the SA-ADC using a digital adder.

A conventional N-bit SA-ADC consisting of a sample and hold (S/H), a comparator, a successive approximation register (SAR) and a capacitive digital-to-analog converter (DAC). In the sampling phase, the analog input signal is sampled and held on capacitor C_s. At the same time the SAR is reset and all DAC capacitors are discharged. In the next N clock phases, the SA-ADC uses the binary search algorithm to find the digital code corresponding to the analog voltage stored on C_s [5]. At the end of a conversion, the analog value of the N-bit digital number is stored on the DAC capacitors.

The structure of the proposed SA-ADC is shown in Fig. 4. Compared to a conventional SA-ADC, this structure has a multiplexer, an N-bit adder, and a control logic block. All these blocks are implemented using digital circuit. Hence, they are not power hungry. The proposed ADC requires two more clock cycles for each conversion. These extra cycles are used to check whether the absolute value of the input signal variation is larger than V_{th} or not. The operation of the proposed architecture is as follows. First, V_i is sampled on the sampling capacitor C_s ($V_i(nT_H)$ or $Vi(n)$, in short). Next, $V_i(n)$ is compared with the voltage stored on the DAC capacitors, which is due to the last conversion ($V_{DAC(PS)}$). Depending on

the value of $V_i(n)$ two different directions may be taken the ADC.

If $V_i(n)>V_{DAC(PS)}$, the comparator output is zero. The output of the comparator is latched in the control circuit and is applied to the carry input of the adder. Therefore, *Dx* (the digital number representing V_{th}) is added to the last sampled digital code (available at the output of the multiplexer). In the next clock cycle, $V_i(n)$ is compared with the new value stored in the DAC, i.e. $V_{DAC(PS)}+V_{th}$. If $V_i(n)<V_{DAC(PS)}+V_{th}$ then the signal variation has not been large enough and the ADC does not convert the signal into digital. In this case the control circuit subtracts V_{th} from the DAC voltage using 2's complement of *Dx*. Otherwise, the input signal ($V_i(n)$) is converted to digital and, as a result, $V_i(n)$ is stored in the DAC capacitors for the next sampling.

If $V_i(n)<V_{DAC(PS)}$, the comparator output is one. The output of the comparator is latched in the control circuit and is applied to the carry input of the adder. In this case *Dx* is subtracted from $V_{DAC(PS)}$ to generate $V_{DAC(PS)}-V_{th}$. In the next clock cycle, $V_i(n)$ is compared with the new value stored in the DAC. If $V_i(n)>V_{DAC(PS)}-V_{th}$ then the signal variation has not been large enough and the ADC does not convert the signal into digital. Otherwise, the input signal ($V_i(n)$) is converted to digital and the value of the DAC voltage is updated.

IV. Mixed FSK and OOK Data Transmission

Digital signal processing (DSP) and wireless data transmission are the most power hungry blocks in the wireless sensor interface circuits, increasing the significance of research on ultra-low-power DSP and radio platforms [1].

The proposed system generates a 10-bit digitized analog waveform from one electrode. To transmit this data wirelessly, a radio-frequency FSK transmitter is used. The operating frequency is chosen at 403 MHz to minimize attenuation of high frequencies by tissue and to operate in the FCC-approved MICS (Medical Implant Communication System) band at 402–405 MHz. Parity bits are added to facilitate error detection, and a data frame containing 11 bits is assembled. Each data frame contains 1 successive ADC sample and parity bit. This data stream is sent to the FSK transmitter in a serial bit stream at a rate of 309kb/s. In addition, due to using adaptive sampling we should send exact time of each sample. However, sending these time flags needs extra bits, which would increase data volume and power consumption. To solve this issue, we have used a modified OOK transmitter mixed with FSK transmitter. In other words, we have used Clk_{sample} signal, generated by ADC block, to turn on the RF transmitter just when the digital signal is prepared by ADC. Hence, for the significant rest of the time the transmitter is not working and power consumption would be saved considerably. Because of adaptive sampling off-time of transmitter is different each time and this represents the time space between each sample. Hence, it is worth mentioning that our adaptive sampling technique do not need extra bits for time flags and can result to lower transmission power as explained.

The schematic of the voltage-controlled oscillator (VCO) modified for mixed FSK and OOK transmitter is shown in

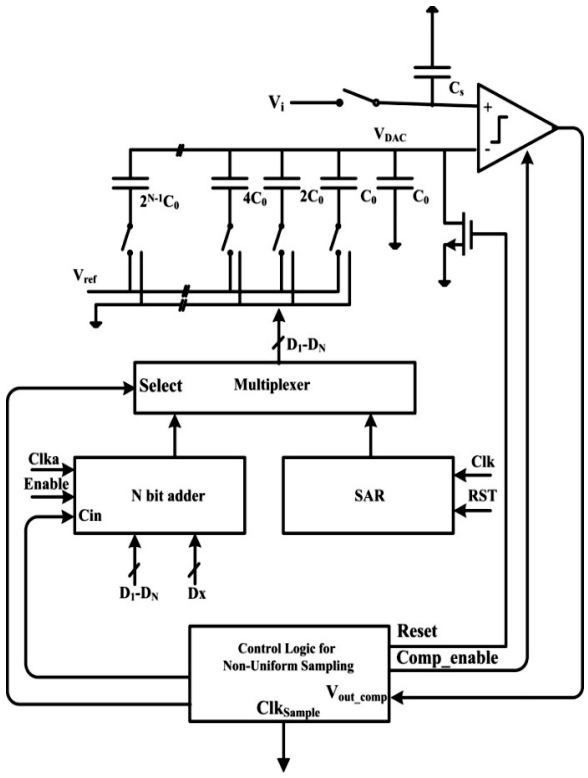

Figure 4. The proposed structure

Fig. 5. Transistors M_{C1}-M_{C4} are accumulation-mode MOS varactors which implement capacitors in *LC* tank circuit. The operating frequency is adjusted by changing the voltage V_{tune}, and modulation is obtained by transferring a digital signal of ADC on V_{data}. To modulate the frequency by an appropriate Δf for FSK operation width of M_{C3}-M_{C4} are drawn 100 times smaller than M_{C1}-M_{C2}. The transistors M_1-M_4 supply enough power to the LC tank circuit to overcome losses and sustain oscillations. The dominant losses in the integrated *LC* tank are due to the series resistance of the inductor [10]. Turning on transmitter for sending data just when the data is prepared by ADC block is done by controlling the bias current of the tail current in the VCO block (see Fig. 5).

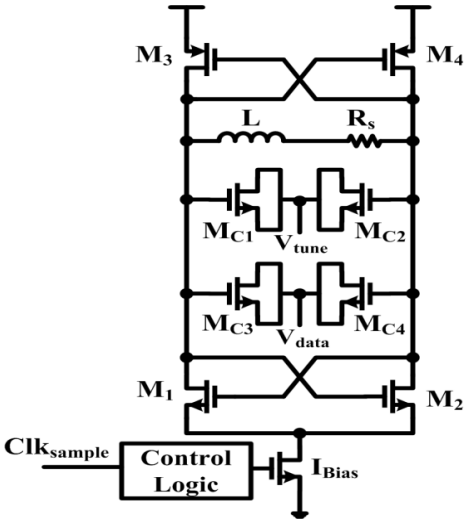

Figure 5. Schematic of VCO used for mixed FSK and OOK transmission

The recovery of the original signal from the sampled data in the external side requires the exact time of the samplings if a non-uniform sampling and transmission is used. The method of saving these time flags is important in reducing the volume of data. The technique that we have used for this is as follow. The ratio of f_H to f_L is 16. Hence, we can assign a 4-bit counter in external side for representing the sampling time with respect to the received previous sampled data. A counter in the receiver counts the time interval during which receiver did not receive the data. In this technique counter output shows the distance of a sample from the previous one, in terms of the number of CLK_H pulses. The main advantage of this is that we do not need to send extra bits for time flag. So, in this non-uniform adaptive sampling system compression ratio is not affected by time flags and is increased more than previous non-uniform sampling techniques [1, 11, 12].

V. Simulation Result

The proposed non-uniform adaptive sampling SA-ADC and mixed FSK and OOK transmitter are implemented in the 0.18µm CMOS technology for the supply voltage of 1V. The resolution of the ADC is 10-bits.

Fig. 6 illustrates sampling clock, output voltage of the DAC, the supply current of VCO, the comparator and the adder, as well as the current taken from V_{ref}. The Clk_{sample} signal shows the periods in which the sampling is done. Whenever Clk_{sample} is high a conversion has happened and when it is low, the input is not converted to digital. During the periods that Clk_{sample} is low, the input has been less than ±60LSB. The current waveforms in this figure show the times that each block is not active. When a block is active a current is taken from the supply or V_{ref}.

In order to check the performance of the system an ECG signal from the MIT-BIH data base (record 231) [13] is applied. Fig. 7 depicts the original and the recovered signals.

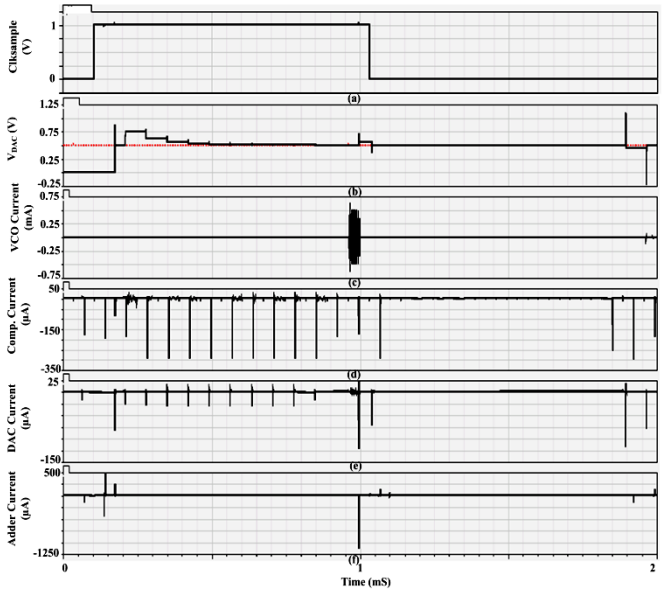

Figure 6. Waveforms of a) Sampling Clock, Clksample, b) DAC output voltage, VDAC, c) supply current of VCO, d)the comparator, e) DAC current taken from Vref and f) supply current of the adder.

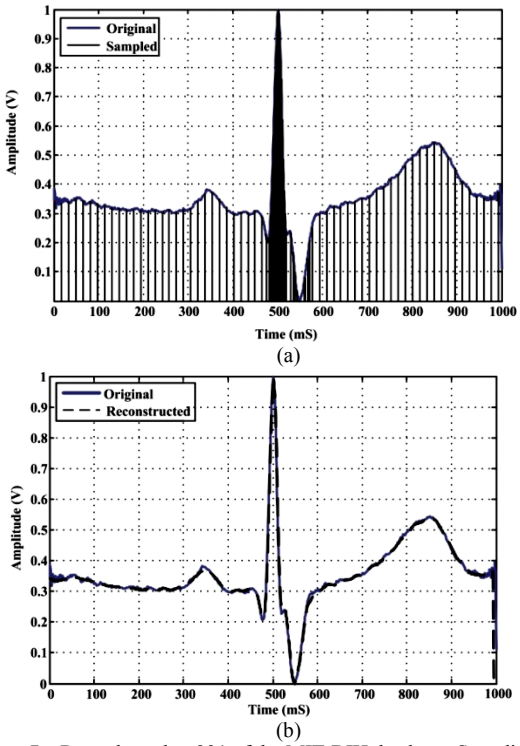

Figure 7. Record number 231 of the MIT-BIH database. Sampling times (a), Original and recovered signals (b)

TABLE I. Simulation results of the proposed SA-ADC and FSK transmitter.

		Proposed adaptive sampling off	Proposed adaptive sampling on
Average Sampling Rate		1000Hz	95Hz
Data Size		10 bit	10 bit
Data Rate		10000 bit/S	950 bit/S
Average power over one ECG period	**ADC**	570 nW	54 nW
	Mixed FSK and OOK Transmitter	118.6 µW	11.24 µW
Power Saving		90.5%	

Simulation results of the SA-ADC and mixed FSK and OOK transmitter are shown in Table 1. As can be seen, the average sampling rate is reduced to 95Hz. The average power consumption of the proposed system is lowered by 90.5%.

VI. Conclusions

A new non-uniform signal specific sub-Nyquist sampling system for sparse signals has been proposed. The presented algorithm monitors the signal with a high frequency and adaptively adjusts the sampling rate based on the activity of the signal. Hence, the average sampling rate is reduced, resulting in considerable power saving and smaller memory size requirement. The sampled data are transmitted to a base station wirelessly. Circuit level simulations of the proposed technique show a compression ratio of 10.5 for the ECG signal and a power saving of 90.5%.

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