Publication Year: 2013 , Page(s): 1 - 4
IEEE CONFERENCE PUBLICATIONS

| | Quick Abstract | PDF (853 KB)

A new rail-to-rail ultra low voltage high speed comparator

Akbari, Masoume ; Maymandi-Nejad, Mohammad ;
Mirbozorgi, S.Abdollah
Electrical Engineering (ICEE), 2013 21st Iranian Conference on
Digital Object Identifier: 10.1109/IranianCEE.2013.6599850
Publication Year: 2013 , Page(s): 1 - 6
IEEE CONFERENCE PUBLICATIONS

| | Quick Abstract | PDF (857 KB)

This paper presents a new rail-to-rail input highperformance regenerative comparator suitable for low-voltage low-power applications, e.g. bio-implantable circuits. In this circuit the body of the PMOS transistor is used as comparator's input. A technique is proposed to increase the speed of the circuit. The proposed comparator has a good performance in weak inversion (sub-threshold). Simulations are done in the 0.18-µm CMOS technology with a supply voltage of 0.5 V. The propagation delay time of the second proposed comparator is 16.4 ns, the power dissipation is 20 nW and the power delay product is 0.33 fJ in clock frequency of 5 MHz and input voltage of 500 µV. Also the supply voltage can be decreased to 0.3 V.
View full abstract»

Sort by: Relevance

A New Rail-to-Rail Ultra Low Voltage High Speed Comparator

Masoume Akbari and Mohammad Maymandi-Nejad
Department of Electrical Engineering
Ferdowsi University of Mashhad
Mashhad, Iran
akbari.masoume@gmail.com , maymandi@um.ac.ir

S. Abdollah Mirbozorgi
Electrical and Computer Engineering Department
University of Laval
Laval, Canada
sa.mirbozorgi@gmail.com

***Abstract*— This paper presents a new rail-to-rail input high-performance regenerative comparator suitable for low-voltage low-power applications, e.g. bio-implantable circuits. In this circuit the body of the PMOS transistor is used as comparator's input. A technique is proposed to increase the speed of the circuit. The proposed comparator has a good performance in weak inversion (sub-threshold). Simulations are done in the 0.18-µm CMOS technology with a supply voltage of 0.5 V. The propagation delay time of the second proposed comparator is 16.4 ns, the power dissipation is 20 nW and the power delay product is 0.33 fJ in clock frequency of 5 MHz and input voltage of 500 µV. Also the supply voltage can be decreased to 0.3 V.**

Index Terms - Regenerative, rail-to-rail, comparator, weak inversion, body driven.

I. INTRODUCTION

Comparators are used in many integrated circuits. The rail-to-rail operation of these circuit blocks is very desirable in low voltage applications and makes the design of the comparator more challenging. To achieve rail to rail operation, typically parallel connection of NMOS and PMOS differential pairs followed by a regenerative latch is employed [1]. A different structure is presented in [2] that uses the body of the PMOS transistors to get a rail-to-rail input range.

One of the most popular comparator structures is based on cross-coupled inverters. The strong positive feedback of this structure results in a fast decision. We can minimize the number of required gain stages to achieve a given resolution by using a track and latch structure for the comparator. Thereby this architecture decreases the area and power dissipation of the circuit. Also it reduces the settling time of the comparator [3].

A latch-type sense amplifier for SRAMs is presented in [4,5]. No static power dissipation, high-impedance input and rail-to-rail output swing, make it a commonly used structure in circuit design. A drawback of this structure is that in low supply voltage, the circuit speed degrades due to stacking transistors [6].

In [6,7] the double-tail structure is presented as a solution to avoid this drawback. It consists of one tail for the input stage and another for the latch. The problem is that it consumes static current to design the latch [8].

In this paper we present a low voltage rail to rail comparator and a novel technique to speed up the transient behaviour of the circuit. In section II the core of the proposed circuit is described. The transient behaviour of the comparator is explored in section III. In section IV a technique is proposed which improves the speed of the comparator. The design steps of the comparator are reviewed in section V. Conclusions are drawn in section VI.

II. THE CORE OF THE PROPOSED COMPARATOR

Figure 1 shows the core of the proposed comparator. It consists of a cross-coupled inverter that acts as a latch. As stated, the bodies of the PMOS transistors of the inverter can be utilized as inputs of the comparator. In [2] two NMOS transistors create the cross-coupled structure, the gates of PMOS input transistors are connected to ground and hence, input transistors were out of the latch positive feedback loop. In our design the gates of the input transistors are connected to the output terminals, therefore they have direct effect on the latch loop. By this method, the speed of the latch increases. Transistor M_0 plays an important role in decreasing the power consumption; because it limits the total current drown from the power supply. Note that the gate of the M_0 is connected to the clock signal (*clk*) instead of a bias voltage. This helps reduce the power consumption and increase the speed during the track (or reset) phase (when the clock signal is high).

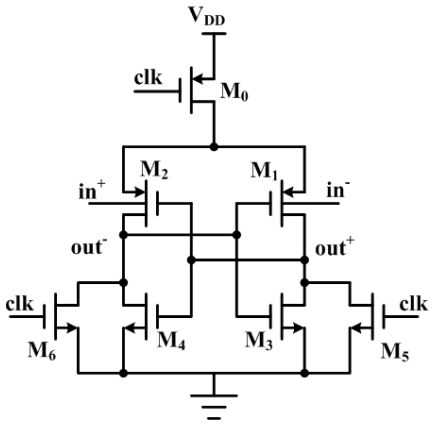

Figure 1. The schematic of the core of the proposed comparator

III. TRANSIENT BEHAVIOUR OF THE LATCH

The transient behaviour of the regenerative comparator described above is shown in Figure 2. During the tracking phase, the clock is high and no current flows in the tail

transistor M_0. Therefore no static power is consumed. Shorting outputs to each other in the track phase is not suitable for low voltage track and latch comparators. This is because turning on the switch is difficult when the supply voltage is low. Hence, to create a meta-stable situation the output nodes out^+ and out^- are connected to *GND* by transistors M_5 and M_6 [2].

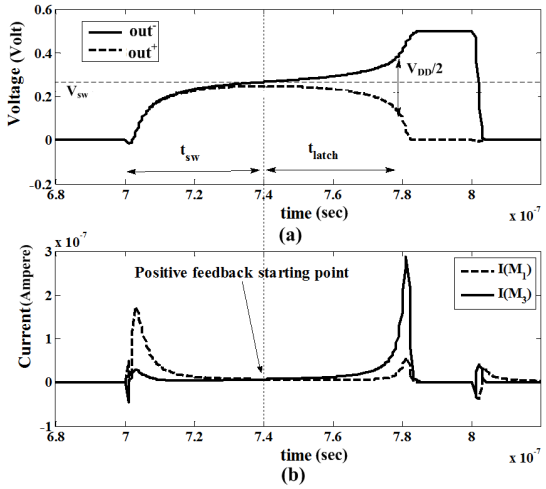

Figure 2. Transient behavior of the proposed latch

When *clk* goes low, the comparator operation starts. Figure 2 shows that comparator operation in the latch phase occurs in two sub-phases. During sub-phase 1, positive feedback has not started yet, and both output terminals get charged until a certain switching point (t_{sw}, V_{sw}).

In the case of strong inversion comparators, the positive feedback activation voltage, V_{sw}, is typically assumed to be equal to the threshold voltage of MOS transistors, V_{Th} [4]. Assuming a constant tail current, t_{sw} can be calculated from Equation (1).

$$t_{sw} = \frac{CV_{Th}}{I_{tail}} . \qquad (1)$$

In Equation (1), C is the output load capacitance, V_{Th} is threshold voltage and I_{tail} is the tail current.

However, the proposed structure works in weak inversion region and has a cross-coupled structure. Hence, the onset of the positive feedback is when the currents of the two transistors of each inverter (M_1 and M_3 or M_2 and M_4) are equal [9].

During the latching period the comparator acts as the following. Unequal input voltages that are applied to the bodies of the input transistors cause different output voltages. At the end of sub-phase 1 there is a difference between output voltages, $\Delta V_o'$. During sub-phase 2 (represented by t_{latch} in Figure 2-a) this difference will be enhanced by strong positive feedback and depending on the polarity of the voltage difference between the inputs, the comparator will flip in one or the other direction [4]. The cross-coupled structure forces one of the transistor's current in each inverter (M_1 and M_4 or M_2 and M_3) to become zero and consequently the current flow stops in both inverters automatically after the outputs are settled.

IV. Speed Enhancement of The Comparator

In this section, a new technique is proposed to speed up the comparator of Figure 1. Figure 3 shows the modified circuit. Transistors M_7 to M_{10} are added to the comparator. During the latch phase a constant current is drawn from the output ports by these transistors. It will be shown later in this paper that this technique can increase the speed of the circuit. By changing the bias voltage which is applied to the gates of M_7 and M_8, we can change the sinking current, I_x. This current can be increased to the extent that tail transistor allows. By increasing I_x, the comparator speed is enhanced.

In Figure 3 in order to avoid speed degradation caused by increasing the load capacitance as a result of the addition of M_7 and M_8, M_3 and M_4 are removed since M_7 and M_8 can take on their role. Therefore the onset of the positive feedback is when the current of PMOS input transistor equals to I_x. To avoid dc current being taken from V_{DD} after the outputs of the comparator are settled, the *ctrl* signal turns off M_9 and M_{10} after the comparator reaches its decision [10].

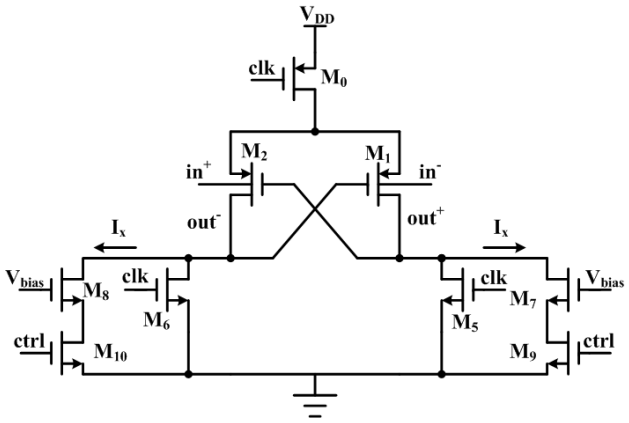

Figure 3. The modified comparator circuit

As a result of the above mentioned technique, the speed improvement is seen in both sub-phases of the operation in the latch phase. As will be explained in the next section, according to the sub-threshold current expression, increasing I_x decreases the drain-source voltage of M_7 and M_8. It means the output needs reaching to a lower voltage with a higher current, and hence t_{sw} decreases. Moreover, increasing this current provides a larger trans-conductance (g_m) for M_1 and M_2, therefore t_{latch} decreases. The comparators of Figure 1 and Figure 3 are simulated in 0.18µm CMOS technology. Figure 4 compares the transient behaviour of the comparator with and without speed enhancement technique. Clearly, the proposed technique has been very effective increasing the speed of the comparator.

V. CIRCUIT DESIGN

A. Propagation Delay Time

In this section, we present an analytical calculation of the comparator's delay time. Although the analysis is done for the comparator shown in Figure 3, results are applicable to the circuit of Figure 1 as well. These calculations help us reach the most efficient design of the comparator.

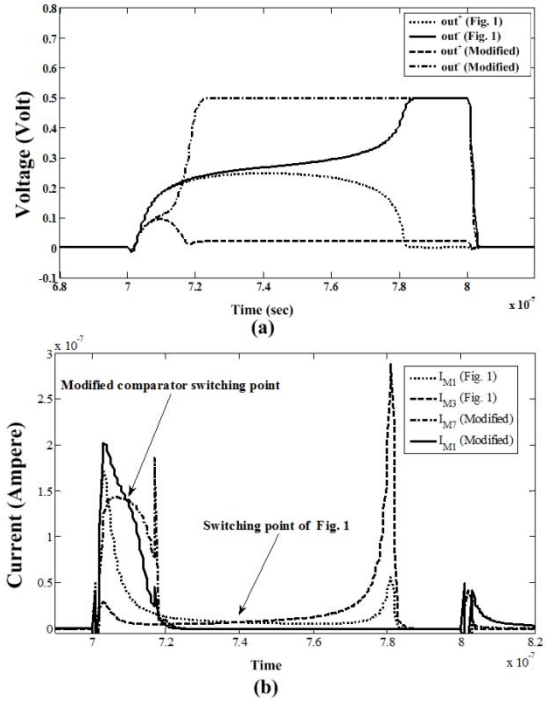

Figure 4. Comparison of transient behaviour of the proposed comparator in Figure 1 and the modified comparator in Figure 3 (a) voltage of output terminals (b) current flows in transistors

Total propagation delay time can be obtained from Equation (2).

$$t_{delay} = t_{sw} + t_{latch} . \tag{2}$$

We assume that the voltage of the input terminal in^+ is lower than that of in^-.

To reach the switching point (t_{sw}, V_{sw}), first we need to find an expression for the output voltage of the time before t_{sw}. According to Figure 4-a, we assume the output voltage can be approximated by the following equation.

$$V_{o2} = kV_{sw}\left(1 - e^{-\alpha t}\right). \tag{3}$$

in which:

$$\alpha = \frac{mI_x}{C}. \tag{4}$$

where V_{o2} is voltage of out^- output terminal. V_{sw} is obtained by setting the current of M_1 equal to I_x and the tail current sets to $2I_x$.

The drain current of a MOSFET in sub-threshold is given by the following equation.

$$I_D = 2\mu C_{ox}\frac{W}{L}nV_T^2 e^{\frac{V_{GS}-V_{Th}}{nV_T}}. \tag{5}$$

V_{sw} can be calculated by equality of Equation (5) (for transistor M_1) to I_x; as follow:

$$V_{sw} = V_{DD} - V_{Thp1} - nV_T \ln\frac{I_x}{I_{0p}} - V_T \ln\left(1 - \frac{2}{A}\frac{I_x}{I_{0p}} e^{\frac{-V_{DD}+V_{Thp0}}{nV_T}}\right). \tag{6}$$

or

$$V_{sw} = V_{DD} - V_{Thp1} - nV_T \ln\frac{I_x}{I_{0p}} - V_T \ln\left(1 - \frac{2}{A}\frac{I_x}{I_{0p}} e^{\frac{-V_{DD}+V_{Thp0}}{nV_T}}\right). \tag{7}$$

I_{0p} and V_{Thp1} (the threshold voltage of input PMOS) can be calculated from equations (8) and (9) below.

$$V_{Thp1} = V_{Thp0} + \gamma\left(\sqrt{2|\phi_p| + V_{SB}} - \sqrt{2|\phi_p|}\right). \tag{8}$$

$$I_{0p} = 2\mu_p C_{ox}\frac{W}{L}nV_T^2 . \tag{9}$$

n (sub-threshold slope factor) for NMOS and PMOS is assumed to be equal and the size of M_0 is 'A' times greater than other transistors.

We also need to find the coefficients of 'k' and 'm' (in Equations (3) and (4)) to find t_{sw}. An equation extracted from curve fitting analysis shows that 'k' is equal to 1.11 and the value of 'm' can be related to I_x as shown in Equation (10).

$$m = 49.18(I_x)^{-0.523} . \tag{10}$$

Figure 5 shows curves which are fitted to simulation result for obtaining 'k' and 'm'.

By substituting 'k', 'm' and equation (4) in equation (3), and replacing V_{o2} by V_{sw}; t_{sw} is given by Equation (11).

$$t_{sw} = \frac{C}{49.18(I_x)^{0.477}} \ln(10) = 23 \times \frac{C}{49.18(I_x)^{0.477}}. \quad (11)$$

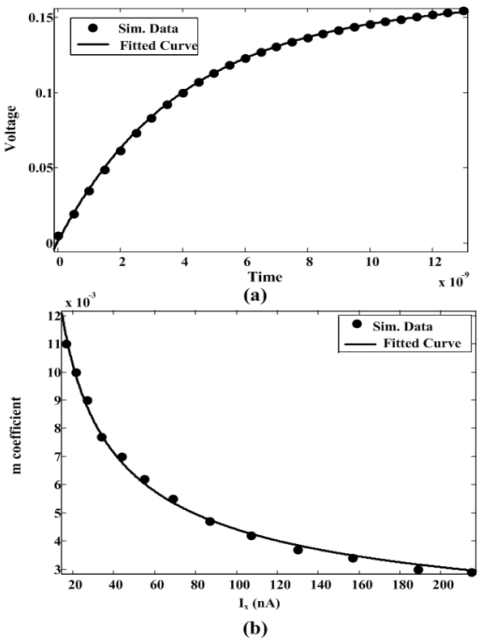

Figure 5. Curve fitting results for (a) finding the output voltage equation variables (b) finding the parameter '*m*'.

Here we use a combination of large-signal and small-signal expressions for the current difference of input transistors. Therefore, we can consider two equations for the current difference.

$$\begin{aligned} \Delta I_p &= g_{mbp1}\left(V_{DD} - V_{\text{in-}}\right) \\ &- g_{mbp2}\left(V_{DD} - (\Delta V_i + V_{\text{in-}})\right). \end{aligned} \quad (12)$$

where g_{mb} is the body-source transconductance, and ΔV_i is the input difference voltage.

$$\begin{aligned} \Delta I_p &= I_{p2} - I_{p1} \\ &= I\left[e^{\frac{V_{DD} - V_{o1} - V_{Thp1}}{nV_T}} - e^{\frac{V_{DD} - V_{o2} - V_{Thp2}}{nV_T}} \right]. \end{aligned} \quad (13)$$

The latch time delay is defined as the time it takes for the difference of the output voltages to reach to $V_{DD}/2$, i.e.:

$$t_{latch} = \frac{C}{g_m} \ln\left(\frac{V_{DD}}{2\Delta V_o^{'}}\right). \quad (14)$$

The initial difference between the outputs out^+ and out^-, $\Delta V_o^{'}$, can be calculated by setting Equation (12) to Equation (13) as follows.

$$\begin{aligned} \Delta V_o^{'} &= \left(V_{Thp2} - V_{Thp1}\right) \\ &+ nV_T \ln \frac{1 + \dfrac{\gamma(V_{DD} - V_{\text{in-}})}{2\sqrt{2|\phi_p| + V_{DD} - V_{\text{in-}}}}}{1 + \dfrac{\gamma\left(V_{DD} - (V_{\text{in-}} + \Delta V_i)\right)}{2\sqrt{2|\phi_p| + V_{DD} - (V_{\text{in-}} + \Delta V_i)}}}. \end{aligned} \quad (15)$$

g_m for a transistor operating in sub-threshold region is defined as below:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_T}. \quad (16)$$

In Equation (16), I_D is assumed to be equal to I_x.

The total propagation delay can now be obtained:

$$\begin{aligned} t_{delay} &= t_{sw} + t_{latch} \\ &= \frac{C}{I_x}\left(0.02(I_x)^{0.523} + nV_T \ln\left(\frac{V_{DD}}{2\Delta V_o^{'}}\right)\right). \end{aligned} \quad (17)$$

In equation (17) the capacitance C is the sum of the external load and the inverter capacitance. The inverter capacitance in sub-threshold regime is a function of gate-source voltage of the transistors and becomes very large near the moderate inversion region.

Equation (17) explains the effect of various parameters on propagation time. As expected, the delay time is related to the output load capacitance directly and is inversely proportional to the sinking current, I_x.

B. Power Dissipation

As it can be seen in Figure 4-b, the current in transistor M_1 has an average near to I_x so we approximate the current of $2I_x$ is drawn from voltage source. Therefore, an analytical equation for the comparator's power dissipation can be derived:

$$\begin{aligned} P_{dissipation} &= P_{leakage} + P_{dynamic} \\ &= P_{leakage} + f_{clk} t_{delay} (2I_x V_{DD}). \end{aligned} \quad (18)$$

where f_{clk} is the clock frequency and $P_{leakage}$ is the power dissipation of the circuit in clock transitions. Figure 6 shows transient behavior of the current which is drawn from the voltage source. Also the leakage current value is marked in Figure 6.

C. Power Delay Product

There is a trade-off between speed and power in most circuits. Hence, a better parameter for comparison is the Power Delay Product (PDP).

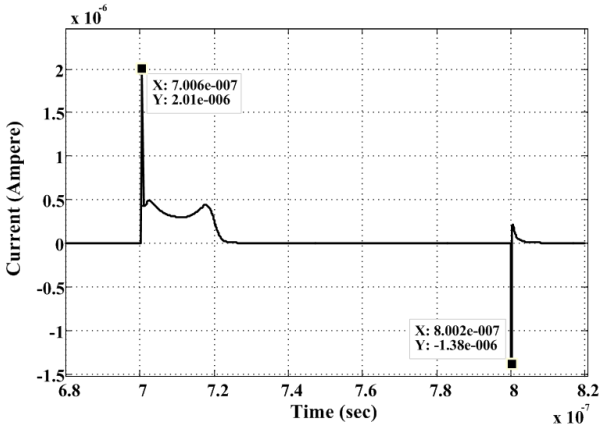

Figure 6. Transition behavior of current which is drawn from the voltage source

An expression for PDP is derived by multiplying Equation (17) and Equation (18)

$$PDP = 2 f_{clk} C V_{DD} \left(0.02(I_x)^{0.523} + nV_T \ln\left(\frac{V_{DD}}{2\Delta V_o'} \right) \right)^2 + P_{leakage} \frac{C}{I_x} \left(0.02(I_x)^{0.523} + nV_T \ln\left(\frac{V_{DD}}{2\Delta V_o'} \right) \right). \quad (19)$$

As it can be seen, the PDP is a function of output load capacitance, clock frequency, initial output voltage difference of sub-phase 2 and the I_x current that is drawn from the output by transistor M_7.

VI. Simulation Results

To prove that the analytical calculations are in agreement with simulation results, some parameters which extracted from calculation and simulation have been compared. All the parameters were found as a function of I_x and all results are normalized to values related to I_x=70 nA. Figure 7 shows the comparison of calculated and simulated results for the switching voltage of the modified proposed circuit as a function of sinking current, I_x.

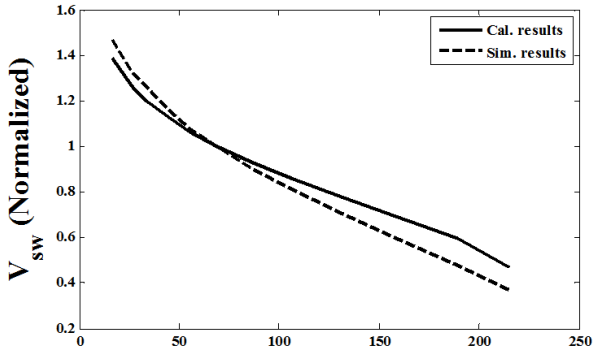

Figure 7. Simulation and calculation results of the second proposed comparator for V_{sw} voltage as a function of I_x, normalized to V_{sw} related to I_x=70 nA.

This comparison is illustrated for t_{sw}, t_{latch}, t_{delay} and PDP in Figure 8. Table I contains the simulation and calculation results for the comparator of Figure 1.

Also TABLE II shows simulation results for the modified comparator I_x=140 nA.

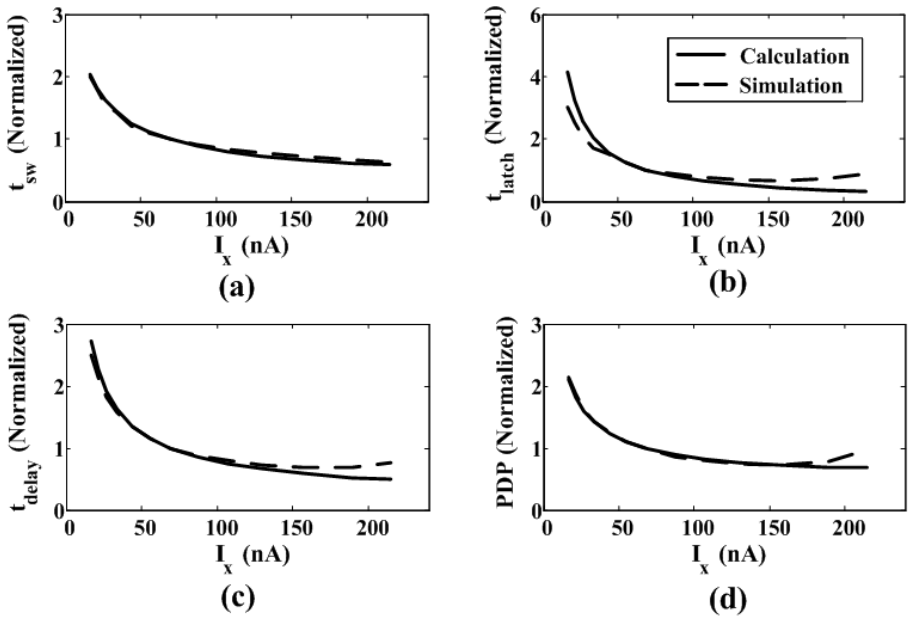

Figure 8. Simulation and calculation results of the second proposed comparator characteristic as a function of I_x, normalized to values related to I_x=70 nA. (a) sub-phase 1 delay time, t_{sw} (b) sub-phase 2 delay time, t_{latch} (c) total propagation delay time, t_{delay} (d) Power Delay Product, PDP.

TABLE I. COMPARISON OF CALCULATION AND SIMULATION RESULTS OF THE COMPARATOR OF FIGURE 1.

Results	t_{sw} (ns)	t_{latch} (ns)	t_{delay} (ns)	V_{sw} (V)	Power (nW)	PDP (fJ)
Simulation	39	39.3	78.2	0.266	14.5	1.14
Calculation	32	39	71	0.25	8.5	0.6

TABLE II. SIMULATION RESULTS OF THE MODIFIED COMPARATOR CIRCUIT IN CLOCK FREQUENCY OF 5 MHZ. (I_X=140 NA).

Results	t_{sw} (ns)	t_{latch} (ns)	t_{delay} (ns)	V_{sw} (V)	Power (nW)	PDP (fJ)
Simulation	8.8	7.6	16.4	0.093	20.2	0.331

Simulation results for our proposed circuits and the circuit presented in [4] with 0.3 V supply voltage is shown in TABLE III.

TABLE IV contains the summarized performance of the proposed comparator, in comparison to the designs in [4], [6], [7] and [8].

TABLE III. SIMULATION RESULTS OF CIRCUITS IN 0.3 V IN CLOCK FREQUENCY OF 62.5 KHZ.

Simulation results	t_{delay} (us)	Power (pW)	PDP (fJ)
[4]	5.3	75	0.397
Comparator in Figure 1	1.7	79	0.135
Modified Comparator	0.98	100	0.098

TABLE IV. PERFORMANCE COMPARISON

Item	[4]	[6]	[7]	[8]	This work (Figure 3)	This work (Figure 3)
Supply voltage	1.5 V	0.65 V	1.2 V	0.6 V	0.5 V	0.3 V
Clock Freq.	-	0.6 GHz	2 GHz	700 MHz	5 MHz	62.5 kHz
Delay time	119 ps	1.66 ns	500 ps	900 ps	16.4 ns	980 ns
Input difference	100 mV	12.1 mV	-	90.2 mV	500 µV	500 µV
Power	-	128 µW	225 µW	47 µW	20.2 nW	100 pW
PDP	-	212 fJ	112.5 fJ	42.3 fJ	0.33 fJ	0.098 fJ
Tech. CMOS	0.13 µm	65 nm UDSM	90 nm	65 nm	0.18 µm	0.18 µm

VII. CONCLUSION

A new rail-to-rail track-and-latch comparator and a technique to improve its speed have been presented. This structure provides a low power dissipation and high speed in sub-threshold regime. The rail-to-rail input capability makes the circuit suitable for high-speed high-resolution applications such as flash, pipelined, and successive approximation ADCs. Separation of input and output terminals enables the circuit to be used in some applications such as SRAMs as a high speed sense amplifier structure. The analytical calculation is used to achieve an efficient design of the proposed circuits.

Simulation results in 0.3 V shows considerable improvement in comparison to the structure of [4] which is a widely used structure in circuit design. All the simulations were done for minimum size of transistors. Using larger transistors, we can achieve faster operation. However, more power will be dissipated.

REFERENCES

[1] H. Pekau, L. Hartley, and J. W. Haslett, "A Re-configurable High-Speed CMOS Track and Latch Comparator with Rail-to-Rail Input for IF Digitization," Proc. International Symposium on Circuits and Systems (ISCAS), vol. 6, pp. 5369 - 5372, July 2005

[2] M. Maymandi-Nejad, and M. Sachdev, "1-bit Quantiser with Rail to Rail Input Range for Sub-1 V ∑Δ Modulators," Electronic Letters, vol. 39, pp. 894-895, June 2003.

[3] B. Fayomi, W. Roberts, and M. Sawan, "Low Power/Low Voltage High Speed CMOS Differential Track and Latch Comparator with Rail-to-Rail Input," Proc. International Symposium on Circuits and Systems , vol. 5, pp 653 -656, May 2000

[4] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier," IEEE Journal of Solid-State Circuits, vol. 39, No. 7, July 2004.

[5] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture," IEEE Journal of Solid-State Circuits, vol. 28, pp. 523–527, April 1993.

[6] B. Goll and H. Zimmermann, "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V," IEEE Tran. On Circuits and Systems-II: Express Briefs, vol. 56, No. 11, November 2009.

[7] D. Schinkel, E. Mensink, E. Kiumperink, E. Tuijl, B. Nauta "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," IEEE Int'l Solid-State Circuits Conference Dig. Tech. Papers, pp. 314-315, February 2007.

[8] B. Goll and H. Zimmermann, "A 65nm CMOS Comparator with Modified Latch to Achieve 7GHz/1.3mW at 1.2V and 700MHz/47µW at 0.6V," IEEE Int'l Solid-State Circuits Conference Dig. Tech. Papers, pp. 327-329, February 2009.

[9] J. Tolbert and S. Mukhopadhyay, "Accurate Buffer Modeling with Slew Propagation in Subthreshold Circuits," IEEE Int'l Symposium on Quality Electronic Design, 2009.

[10] A. Valaee and M. Maymandi-Nejad, "An Ultra Low-Power Low-Voltage Switched-Comparator Successive Approximation Analog to Digital Converter." IECE Electronics Express, vol. 6, No. 15, pp. 1098-1104, August 2009.