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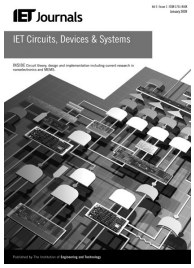

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Analytical model for CMOS cross-coupled LC-tank oscillator

Mojtaba Daliri, Mohammad Maymandi-Nejad

Electrical Engineering Department, Integrated Systems Laboratory, Ferdowsi University of Mashhad, Mashhad 91775-1111, Iran
E-mail: mojtaba.daliri@gmail.com; m_daliri2003@yahoo.com

Abstract: Periodic steady-state behaviour of cross-coupled LC-tank oscillator is of critical importance in ultra-low power, low-voltage transceiver circuits. Understanding the major factors affecting amplitude, oscillation frequency and power consumption would lead to more optimised oscillator design particularly for short-range wireless transceivers. This study presents a new approach for evaluating the amplitude of the main component, oscillation frequency and power consumption of cross-coupled LC-tank oscillator. Three major factors, affecting oscillator functionality are examined. In order to obtain a general design methodology, the effects of oscillator parameters such as transistors' sizes, inductor and capacitor values are investigated. An intuitive discussion about oscillator behaviour and a design procedure are presented. The theoretical results are verified by circuit simulations in the 0.18 μm CMOS process.

1 Introduction

Oscillators are one of the most common functional blocks in communication systems. Integrated LC voltage-controlled-oscillators (VCOs) are used to up- and down-convert signals and have particular importance in fully integrated transceivers [1]. Proper estimation of amplitude and oscillation frequency is a key factor in achieving suitable performance for a VCO [2, 3]. Owing to the fact that a VCO is a non-linear circuit, during the design phase, it is difficult to accurately predict the output voltage, oscillation frequency and power consumption. Therefore a comprehensive analysis which clearly defines the relations between oscillation amplitude, oscillation frequency and power consumption is of critical importance to the designer. Phase noise is another important parameter in the design of oscillators. However, in short range bio-implantable transceivers phase noise would be less problematic and the designer can trade it with other parameters like power consumption.

Some of the previous analytical works on oscillators relate the amplitude of oscillation to bias current and parasitic parallel resistance of the LC tank. In [4, 5] a complex set of equations requiring mathematical computer aided solutions are used for estimating the amplitude. In other works, such as [5–8] the operation of oscillators are analysed under two different regimes:

- Current-limited regime where single-ended peak amplitude is proportional to bias current times tank parallel losses.
- Voltage-limited regime where the amplitude is limited by supply voltage.

In these two regimes, the effects of inductance and capacitance values are not considered and the only important parameter affecting amplitude is considered to be the parasitic losses of the LC tank. A major drawback of these analyses is that the effect of cross-coupled transistors in determining oscillation amplitude and frequency is ignored. Moreover, in these works, the border between these two regimes is not clarified. In this paper, we will define this border and behaviour of the oscillator in these two regimes is described.

Another parameter affecting oscillation amplitude is oscillation frequency. The effect of frequency on amplitude is not considered in most analytical approaches. The frequency variations lead to amplitude changes, hence, an FM to AM modulation happens in many oscillators. This FM to AM conversion is more apparent especially in short-range oscillator transmitters in which the oscillator is directly connected to the antenna [9]. In [7], an equation is derived for oscillation amplitude. However, in the equation for the amplitude, the effect of frequency variation is not considered.

In [10], the LC tank of an oscillator is analysed using perturbation analysis to find out the effect of varactor non-linearity on oscillation frequency. It is shown that the non-linearity of the oscillator varactor changes the frequency in a way which is different from what is obtained from the well known $1/\sqrt{LC}$ equation. A similar approach is taken in [11] to examine the effect of mismatch. However, the non-linearity of transistors is not considered.

In this paper, an analytical method is presented that provides a quantitative understanding of output voltage amplitude, oscillation frequency and power consumption and will allow us to design an optimised CMOS oscillator.

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The analysis approach focuses on the effects of transistors sizes, inductance and capacitance values. According to the derived equations, a discussion about oscillator functionality is presented and finally a design procedure for having minimum power consumption is presented. This paper is organised as follows. In Section 2, the model of the CMOS oscillator used in this paper is introduced. Analytical relations for transistor current and output voltage are derived, too. The oscillation frequency and the effects of oscillator parameters are discussed in detail in Section 3. Section 4 is focused on power consumption. The behaviour of the oscillator in the two above mentioned working regimes is discussed in Section 5. A design procedure to minimise power consumption for a specific oscillation frequency and output voltage amplitude is presented in Section 6. Finally, conclusions are drawn in Section 7.

2 Output voltage amplitude

The schematic of the VCO studied in this work and its equivalent circuit model are shown in Figs. 1*a* and *b*, respectively. According to Fig. 1*a* the oscillator consists of two identical cascaded sections whose outputs are 180° out of phase. The two transistors of the VCO are modelled by two non-linear current sources as shown in Fig. 1*b*. The resistor R in this model is the series resistance of the inductor. In our analysis, we would like to replace the series combination of R and L with its equivalent parallel combination (R_{eq} and L_{eq}). If the quality factor of the RLC tank is high, this conversion can be achieved using the following equations

$$R_{\text{eq}} = R\left(1 + Q_L^2\right) \tag{1}$$

$$L_{\text{eq}} = L\left[\frac{Q_L^2 + 1}{Q_L^2}\right] \tag{2}$$

where Q_L is the quality factor of the inductor (L) and can be found from

$$Q_L = \frac{X_L}{R} = \frac{L\,\omega}{R} \tag{3}$$

To obtain the analytical equations, we consider a half circuit model for the oscillator as demonstrated in Fig. 2. In this figure, L_{eq} is the equivalent parallel inductance of the LC tank at the frequency of ω, and C is the total capacitance at the output node including the varactor, parasitic capacitance of transistors and load capacitance. R_{eq} is the equivalent parallel resistance of the inductors at the frequency of ω. i_{S1} is a non-linear current source by which a transistor is modelled.

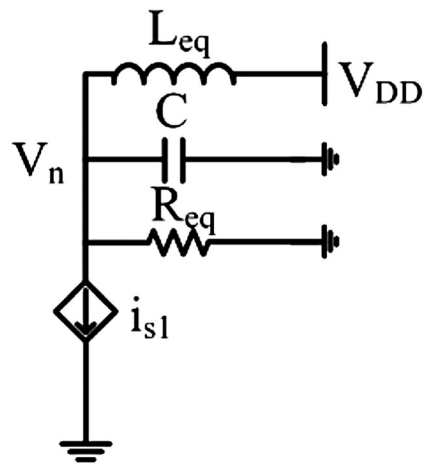

Fig. 2 *Oscillator half circuit model*

Since the two outputs of the oscillator are 180° out of phase, the two output voltages of Fig. 1*a* can be expanded in a Fourier series as the following

$$V_n = A_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t) + \sum_{n=1}^{\infty} B_n \sin(n\omega t) \tag{4}$$

$$V_P = A_0 + \sum_{n=1}^{\infty} (-1)^n A_n \cos(n\omega t) + \sum_{n=1}^{\infty} (-1)^n B_n \sin(n\omega t) \tag{5}$$

where A_0, A_n and B_n are the Fourier series coefficients.

Fig. 3 shows the typical waveform of the drain current of M_1, which is modelled by i_{S1} in Fig. 2. In general, the output currents of transistors are not symmetric. Therefore neither A_n nor B_n coefficients can be assumed zero. Although the current

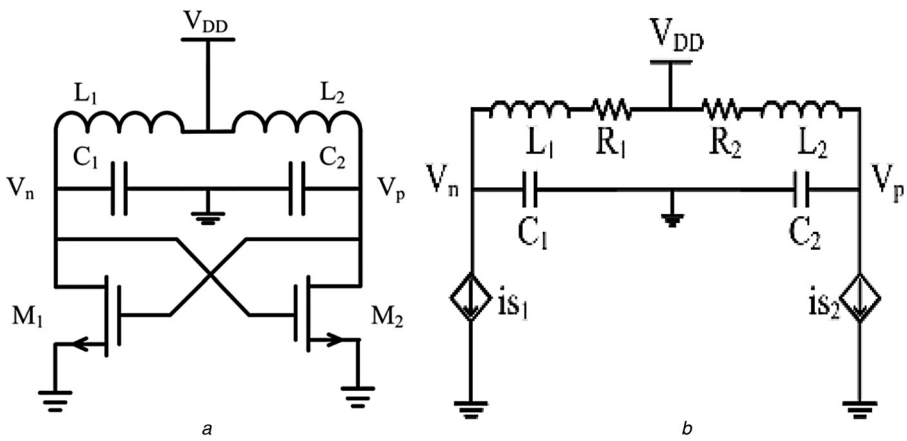

Fig. 1 *CMOS VCO*

a Cross-coupled LC-tank CMOS oscillator
b Oscillator analytical model

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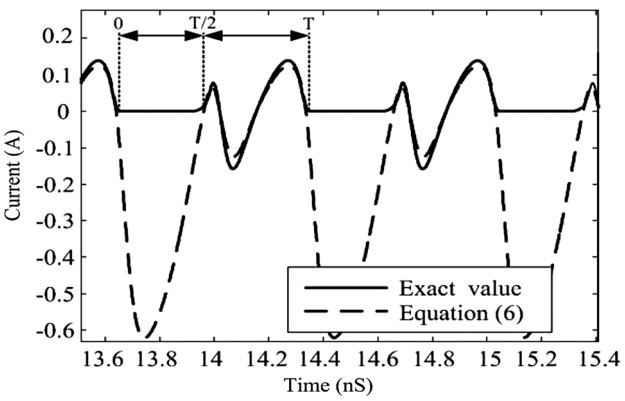

Fig. 3 *Waveform of the current of the oscillator transistor*

is not symmetric, in many works, the symmetry of transistor current is assumed for the sake of simplicity [5].

Owing to the fact that MOSFETs are acting like switches, we can approximately consider the transistor current to be zero for half of each period, that is, $0 \le t \le T/2$ (Fig. 3). During the second half period ($T/2 \le t \le T$) the transistor is on and passes through the saturation region very rapidly and remains in the triode region for most of the time. For simplicity, here it is assumed that the transistor is in the triode region during the second half cycle and its current can be obtained from the following equation

$$i_{S1} = \mu_n C_{\text{ox}} \frac{W}{L_G}\left[\left(V_P - V_{\text{T}}\right)V_n - \frac{1}{2}V_n^2\right] \tag{6}$$

where μ_n is inversion layer mobility, C_{ox} is gate oxide capacitance per unit area, V_{T} is threshold voltage, and W and L_G are the width and length of M_1, respectively.

To check the validity of the above assumption, the current of transistor represented by (6) is drawn in Fig. 3 by the dashed line. Comparing the current obtained from (6) (dashed line) and the exact current obtained from simulation (bold line), it is clear that when the transistor is on, (6) faithfully represents the actual transistor current. Hence, we will use (6) for the half period when the transistor is on and assume the current is zero for the other half period.

Since the drain current is periodic, it can be represented by the Fourier series as the following

$$i_{s1} = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{7}$$

In (7), a_n and b_n are given by

$$a_n = \frac{\omega}{\pi}\left[\int_0^{(\pi/\omega)} 0\,\cos(n\omega t)\,\mathrm{d}t + \int_{(\pi/\omega)}^{(2\pi/\omega)} i_{s1}(t)\cos(n\omega t)\,\mathrm{d}t\right]$$
$$b_n = \frac{\omega}{\pi}\left[\int_0^{(\pi/\omega)} 0\,\sin(n\omega t)\,\mathrm{d}t + \int_{(\pi/\omega)}^{(2\pi/\omega)} i_{s1}(t)\sin(n\omega t)\,\mathrm{d}t\right] \tag{8}$$

Now using the half circuit model of Fig. 2, the nth harmonic of the output voltage in (4) could be computed by multiplying the nth harmonic of the output current by the output impedance.

Using this method, $2n$ equations for $2n$ variables, that is, $A_1, \ldots, A_n$, and $B_1, \ldots, B_n$, can be obtained. Solving these $2n$ equations, all A_n and B_n coefficients can be found. However, solving these $2n$ equations simultaneously in terms of circuit parameters are very complicated and the results would not convey any useful qualitative information about the amplitude of the output voltage harmonics. To overcome this problem, we assume that the second and higher order harmonic can be neglected. Fig. 4 shows the ratio of the amplitude of the second harmonic to the amplitude of the first harmonic for different values of inductance and transistors sizes. As shown in Fig. 4, in the worst case, the first harmonic is nearly five times larger than the second harmonic. Assuming that the amplitude of higher order harmonics decreases as the harmonic order increases, we can ignore the harmonics and use the following equation to obtain the amplitude of the main component. Although this technique does not provide any information about the amplitudes of harmonics, it can estimate the amplitude of the main component quite accurately as will be seen later. Therefore for the sake of simplicity, Fourier series of (4) and (5) and (7) are simplified to the following equation

$$\begin{aligned} V_n(t) &= A_0 + A_1\cos(\omega t) + B_1\sin(\omega t) \\ V_P(t) &= A_0 - A_1\cos(\omega t) - B_1\sin(\omega t) \\ i_{s1}(t) &= a_0 + a_1\cos(\omega t) + b_1\sin(\omega t) \end{aligned} \tag{9}$$

Therefore the output voltage is equal to

$$\begin{aligned} V_n(t) &= -R_{\text{eq}}\, i_{s1}(t) \\ &\Rightarrow A_0 + A_1\cos(\omega t) + B_1\sin(\omega t) \\ &= -R_{\text{eq}}\big(a_0 + a_1\cos(\omega t) + b_1\sin(\omega t)\big) \end{aligned} \tag{10}$$

According to (10), the Fourier series coefficients of the output current could be found as a function of the output voltage Fourier components. That is

$$\begin{aligned} A_1 &= -R_{\text{eq}} a_1 \\ B_1 &= -R_{\text{eq}} b_1 \end{aligned} \tag{11}$$

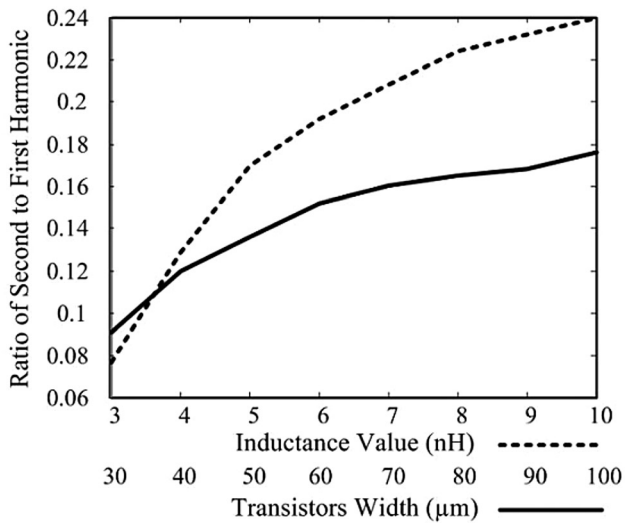

Fig. 4 *Ratio of second harmonic to first harmonic amplitudes for different values of inductance and transistors size values*

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Using (6), (8), (9) in (11) and solving for A_1 and B_1 leads to

$$A_1 = \sqrt{A_0(A_0 - 2V_T)} \tag{12}$$

$$B_1 = \frac{\pi}{4}(A_0 + V_T) - \frac{\pi}{2xR_{eq}} \tag{13}$$

where $x = \mu_n C_{ox} W/L_G$ and A_0 is the DC component of the output voltage ($A_0 \simeq V_{DD}$ if the series resistance is negligible). According to (12) and (13) in order to find the amplitude of the main component the parameter A_0 should be known. Unfortunately, finding an exact equation for A_0 is a non-trivial task and the result is so complicated that it would not be very useful for designing the oscillator. One way to overcome this problem is to assume $A_0 \simeq V_{DD}$. A better approximation for A_0 can be found by assuming that A_0 is less than V_{DD} by an amount equal to the DC voltage drop across the series resistance of the inductor (R). According to Fig. 1*b* A_0 can approximately be estimated from

$$A_0 = V_{DD} - R\,I_D = V_{DD} - R\frac{1}{2}x(A_0 - V_T)^2 \tag{14}$$

$$A_0 = V_T + \frac{\sqrt{1 + 2Rx(V_{DD} - V_T)} - 1}{Rx} \tag{15}$$

and the amplitude of the main component is

$$\text{first harmonic } h_1 = \sqrt{A_1^2 + B_1^2} \tag{16}$$

In order to check the accuracy of (12), (13) and (15) in estimating the amplitude of the main component the main circuit parameters; that is, the capacitance, inductance and transistor sizes, are varied over a relatively large range and the amplitude is obtained from simulations and calculation. The results are illustrated in Fig. 5. As can be seen in this figure, (12), (13) and (15) predict the amplitude of the main component quite accurately. The error in all cases is less than 10%. Also, note that assuming $A_0 \simeq V_{DD}$ is a good estimate when the size of transistors or the value of the capacitance is changed.

The variations of oscillation frequency (ω) affect R_{eq} and thus B_1 in (13), that is, higher ω results in a bigger R_{eq} and smaller B_1. Therefore the value of oscillation frequency plays a critical role in determining the first harmonic amplitude.

3 Frequency of oscillation

In this section, the non-linear behaviour of transistors will be considered in determining oscillation frequency. As will be shown later in this section, transistor non-linearity has a considerable effect on oscillation frequency of the cross-coupled LC-tank oscillator. According to the circuit model of Fig. 1*b* for the oscillator of Fig. 1*a*, the following

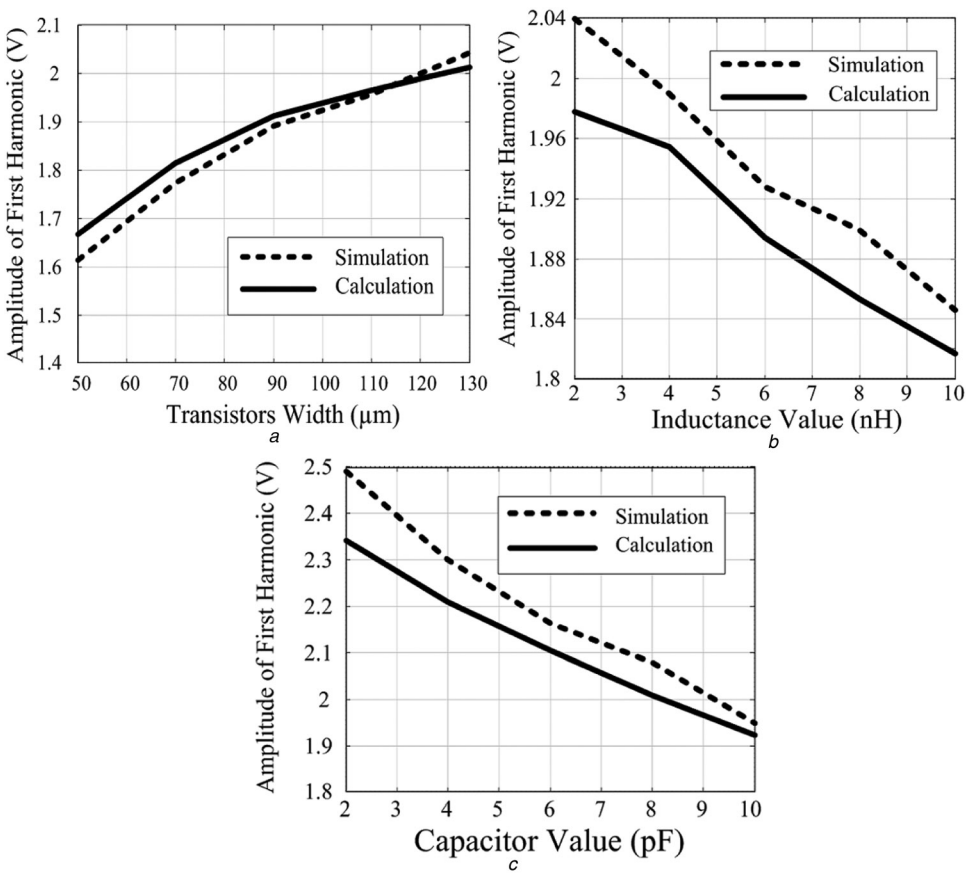

Fig. 5 *Amplitude of the main component*

a Amplitude of first harmonic against transistors sizes. $C = 10$ pF, $L = 5$ nH, $R = 5\ \Omega$
b Amplitude of first harmonic against the variation of inductance values. $C = 10$ pF, aspect ratio = 100 μm/0.18 μm
c Amplitude of first harmonic against the variation of capacitance values. $L = 5$ nH, $R = 5\ \Omega$, aspect ratio = 100 μm/0.18 μm

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differential equation can be easily obtained for the output voltage V_n.

$$LC\frac{\mathrm{d}^2 V_n}{\mathrm{d}t^2} + RC\frac{\mathrm{d}V_n}{\mathrm{d}t} + V_n = V_{DD} - L\frac{\mathrm{d}i_{s1}}{\mathrm{d}t} - Ri_{s1} \qquad (17)$$

Fig. 6 shows two cycles of the two output voltages of the oscillator. The crossing point of the two voltages is denoted by K_0 which is smaller than the supply voltage (V_{DD}). According to. 3, for one half period of the output voltage, M_1 turns off and $i_{s1}(t) = 0$.

Ignoring the effect of the inductor's parasitic resistance the differential (17) can be simplified to (18). Solving (18) leads to (19)

$$LC\frac{\mathrm{d}^2 Vn}{\mathrm{d}t^2} + Vn = V_{DD} \qquad (18)$$

$$V_n(t) = V_{DD} + K_1\sin(\omega\, t) + K_2\cos(\omega\, t) \qquad (19)$$

In (19), ω is equal to $1/\sqrt{LC} = 2\pi/T$. Note that (19) is valid only for the time period in which the current is zero ($T_n/2$ in Fig. 6). The difference between T and T_n (refer to Fig. 6) is 2τ. Hence, in order to find an exact value for oscillation frequency τ should be calculated.

Referring to Fig. 6 and assuming the time origin is where the voltage V_n is equal to V_{DD}, the coefficient K_2 in (19) should be zero. Therefore (19) can be simplified to the following equation

$$V_n(t) = V_{DD} + K_1\sin(\omega\, t) \qquad (20)$$

The parameter τ can be obtained from (20) by setting $V_n(t = \tau) = K_0$, leading to

$$\tau = -\sqrt{LC}\sin^{-1}\left(\frac{V_{DD} - K_0}{K_1}\right) \qquad (21)$$

As shown in Fig. 6, the period of the output voltage of the oscillator (T_n) can be found as the following

$$\frac{T_n}{2} = \frac{\pi}{\omega} + |2\tau| \Rightarrow T_n = 2\pi\sqrt{LC} + 4\sqrt{LC}\sin^{-1}\left(\frac{V_{DD} - K_0}{K_1}\right) \qquad (22)$$

Therefore oscillation frequency is found from the following equation

$$\omega_n = \frac{2\pi}{T_n} = \frac{2\pi}{\sqrt{LC}\left(2\pi + 4\sin^{-1}\left(V_{DD} - K_0/K_1\right)\right)} \qquad (23)$$

To check the validity of the above equation the oscillator is simulated with different parameters in SPICE. Fig. 7 illustrates the oscillation frequency obtained from (23) and compares it with simulation results. As can be seen in Fig. 7, there is a reasonable agreement between circuit simulations and (23). In Fig. 7, in the calculation of frequency using (23), the value of K_0 is obtained from simulation and K_1 is approximated by the first harmonic amplitude.

Also shown in Fig. 7 is the oscillation frequency obtained from the well known equation of $1/\sqrt{LC_{\mathrm{tot}}}$ in which C_{total} is the total capacitor at the output node. As can be seen, there is a relatively large discrepancy between the value obtained from simulation and $1/\sqrt{LC_{\mathrm{tot}}}$. It is typically stated that the reason for this discrepancy is the non-zero resistance of the inductor. Simulations of the oscillator with $R = 0$ and $R = 5\,\Omega$ show that for both cases the difference between the curve of $1/\sqrt{LC_{\mathrm{tot}}}$ and simulations are considerable. This shows that the main reason for the oscillation frequency to be different from $1/\sqrt{LC_{\mathrm{tot}}}$ is the inherent non-linearity of the oscillator. According to (21), the oscillation frequency will be $1/\sqrt{LC_{\mathrm{tot}}}$ only if we can make K_0 equal to V_{DD}. This cannot be achieved in practice when the effect of non-linearity is large.

Referring to (23), K_0 plays a critical role in determining oscillation frequency and without knowing the value of K_0 the frequency cannot be calculated. K_0 is a quantitative parameter of oscillator non-linearity. When the non-linearity of the oscillator is increased, the difference between V_{DD} and K_0 increases, too. Finding an equation for K_0 is a difficult task. Instead, we have run many simulations with different circuit parameters to obtain an empirical equation for K_0. The values of K_0 obtained from these simulations are illustrated in Fig. 8.

Using curve fitting, we have found the following empirical equation for K_0

$$K_0 = \frac{\xi}{\sqrt{W}}\frac{\sqrt[4]{C}}{\sqrt[4]{L}} \qquad (24)$$

where ξ is a constant coefficient that needs to be found only once by simulation. When ξ is found from simulation, (24)

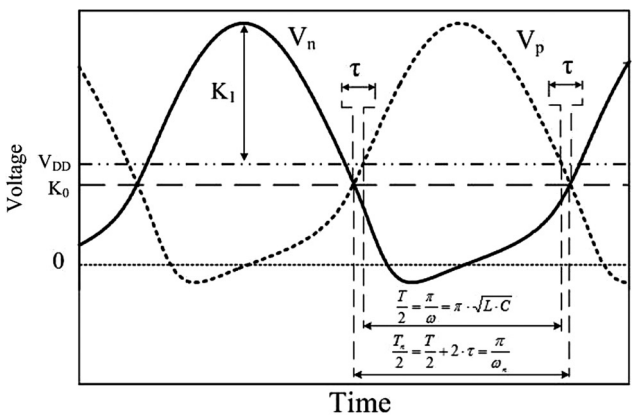

Fig. 6 *Two output voltages of oscillator*

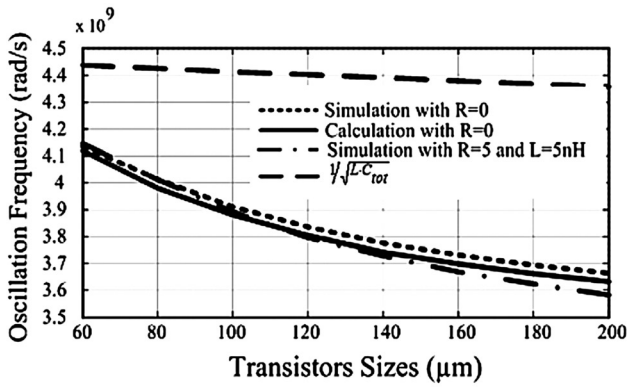

Fig. 7 *Oscillation frequency against transistor sizes (L = 5 nH, C = 10 pF)*

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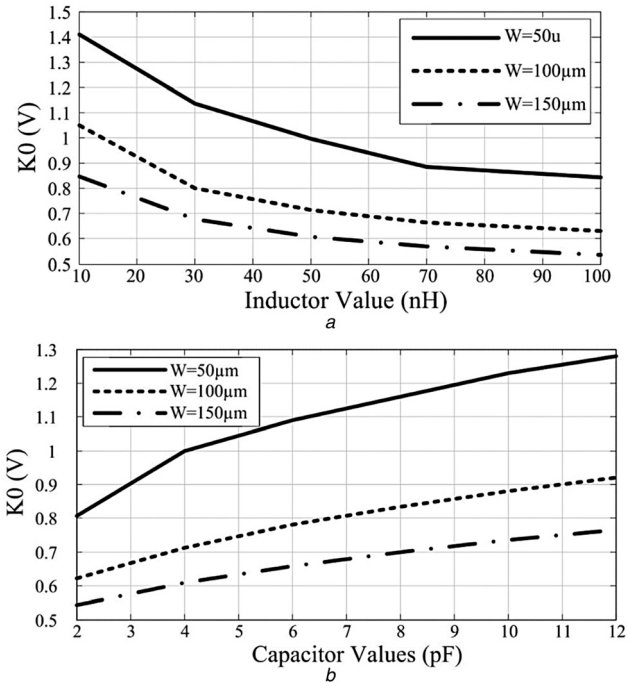

Fig. 8 *K_0 value in (20)*

a Against the variation of inductance values for three different aspect ratios ($C = 10$ pF, $L_G = 0.18$ μm and $V_{DD} = 1.8$ V)
b Against the variation of capacitor values for three different aspect ratios ($L = 20$ nH, $L_G = 0.18$ μm and $V_{DD} = 1.8$ V)

can be used for other circuit parameters to obtain K_0 and to find the oscillation frequency.

To verify (24), the oscillation frequency is obtained from (23) and (24) and is compared with simulations. The results are illustrated in Fig. 9. These curves clearly show the accuracy of (23) and (24). In these calculations the coefficient ξ is equal to 0.052.

According to (24), K_0 is proportional to $1/\sqrt{W}$ ($L_G = 0.18$ μm). As mentioned above, K_0 is an indication of the non-linearity of the oscillator. Hence, transistors with higher aspect ratios lead to a smaller K_0 and consequently more non-linearity. As the non-linearity of the circuit increases, (23) gives the frequency of oscillation more accurately than $1/\sqrt{LC_{\text{tot}}}$.

As (24) indicates, K_0 is an increasing function of the capacitor value. This means increasing the capacitance leads to less non-linearity and the oscillation frequency will be closer to the ideal value of $1/\sqrt{LC_{\text{tot}}}$. The inductor has an opposite effect on the non-linearity of the oscillator and as L is chosen larger the non-linearity increases. Note that the size of transistors has the greatest effect on the non-linearity compared with the capacitor and inductor.

4 Power consumption

In order to have a quantitative estimation of the oscillator power dissipation, the DC current drawn from supply by the oscillator should be obtained. According to (7), a_0 is the DC component of each transistor current. Using (6)–(8) a_0 is equal to

$$a_0 = \alpha x - \frac{\beta}{x} + \gamma \tag{25}$$

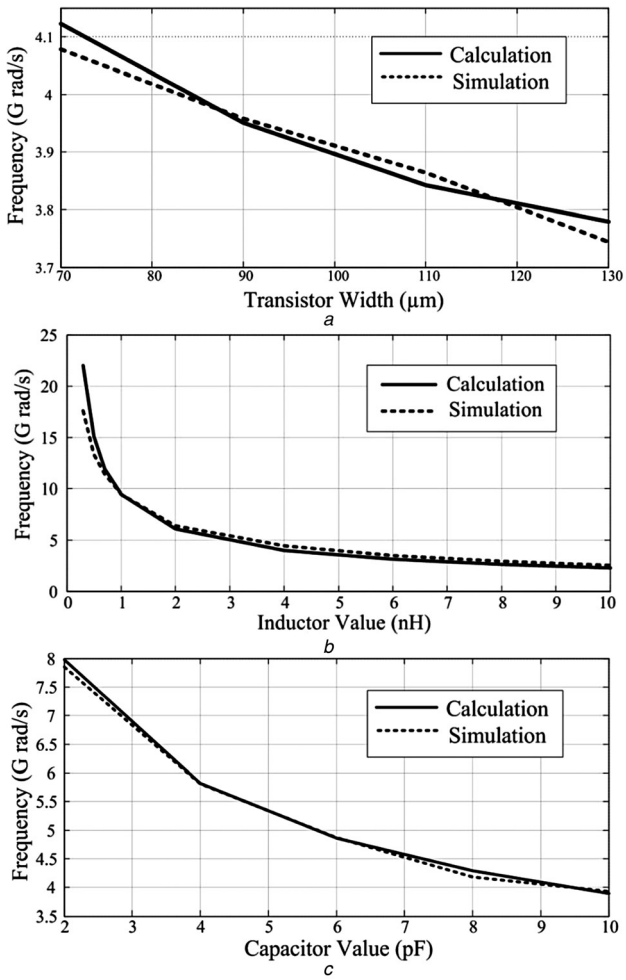

Fig. 9 *Oscillation frequency is obtained from (23) and (24)*

a Oscillation frequency against transistors' sizes, $C = 10$ pF, $L = 5$ nH, $R = 5\ \Omega$
b Oscillation frequency against the variation of inductance values, $C = 10$ pF, aspect ratio = 100 μm/0.18 μm
c Oscillation frequency against the variation of capacitance values, $L = 5$ nH, $R = 5\ \Omega$, aspect ratio = 100 μm/0.18 μm

where

$$\alpha = \frac{1}{128}\left[\left(16 - 3\pi^2\right)\left(A_0 + V_{\text{T}}\right)^2 + 64A_0\ VT + 16V_{\text{T}}^2\right]$$

$$\beta = \frac{12\pi^2}{R_{\text{eq}}^2}, \quad \gamma = \frac{A_0 + V_{\text{T}}}{R_{\text{eq}}}\left(12\pi^2 - 64\right)$$

If we ignore the variation of A_0, α is constant and (25) could be written as the following

$$a_0 = \underbrace{\alpha x}_{(1)} - \underbrace{\frac{12\pi^2}{R_{\text{eq}}^2 x}}_{(2)} + \underbrace{\frac{\gamma'}{R_{\text{eq}}}}_{(3)} \tag{26}$$

where $\gamma' = A_0 + V_T(12\pi^2 - 64)$. As can be seen in (26), the DC current of each transistor depends on the size of transistors (x) and the equivalent parallel resistance of the LC tank. The total power consumption of the oscillator can now be found as the following

$$P_{\text{av}} = 2V_{DD}a_0 \tag{27}$$

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Fig. 10 shows the effect of transistors sizes, as well as inductor and capacitor values on power dissipation of the oscillator.

5 Discussion

In [8], two operating modes are defined for an oscillator, that is,

- Current-limited or inductance-limited regime.
- Voltage-limited regime.

In the current-limited regime, the tank amplitude linearly grows with the bias current until the oscillator enters the voltage-limited regime. In the voltage-limited regime, the amplitude is limited to a voltage, which is determined by supply voltage and/or a change in the operation mode of active devices (e.g. MOS transistors entering triode region).

In the current-limited regime, the tank amplitude grows with L for given a E_{tank} and ω_0 as indicated in [8]. In this region, the inductance can be supposed to be the independent variable and it is possible to describe the oscillator behaviour as a function of L. This alternative denomination will facilitate the understanding of various tradeoffs in oscillator design throughout this work. Once the tank amplitude reaches V_{limit}, it stops increasing with further increase of the inductance and the oscillator will enter the voltage-limited regime as before and increasing the inductance value only increases the non-linearity of the circuit and changes the oscillation frequency [(23) and (24)].

To investigate this phenomena, a series of calculations for different values of inductance and current is performed using (12), (13), (16) and (25) for a constant oscillation frequency. To keep the oscillation frequency constant, the production of L and C is kept constant (ω is assumed to be $1/\sqrt{LC}$). For ten different inductance values (from 1 to 10 nH) the width of transistors is swept and the values of the first harmonic and the DC current (a_0) are obtained. The calculation results are shown in Figs. 11 and 12.

According to Fig. 11, increasing the bias current for low inductance values leads to larger output voltage amplitude. For large inductance values, increasing the bias current does not have any major effect on the amplitude of the voltage.

Since the bias current is mainly determined by the size of transistors, the current limited regime can be viewed from a different perspective, that is, the transistors sizes can be used as the independent variable instead of bias current.

As shown in Fig. 12, the output voltage amplitude depends on the size of transistors only for small inductance values and when the inductance values are increased, the output voltage is approximately constant and transistors' sizes do not have any major effects on voltage amplitude.

Based on (12) and (13), three parameters (A_0, x and R_{eq}) determine the values of A_1 and B_1. A_0 is not a strong function of transistors sizes. It can be assumed to be constant; consequently A_1 and the first part of B_1 in (13) will be approximately constant. The second part of (13) is an inverse function of both x and R_{eq}. Small value of inductance leads to a smaller value of series resistance (R) and consequently R_{eq}, therefore B_1 will be a stronger

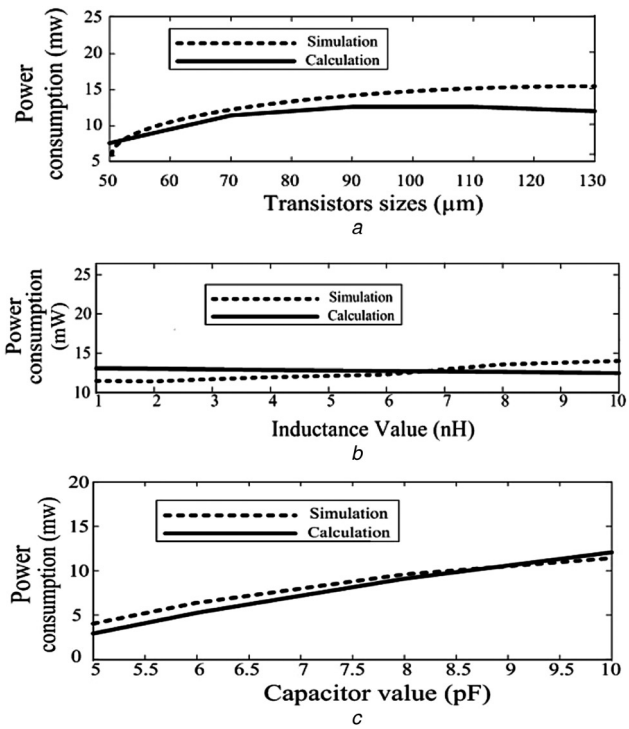

Fig. 10 *Effect of transistors sizes, as well as inductor and capacitor values*

a Power consumption against transistors sizes. $C = 10$ pF, $L = 5$ nH, $R = 5\ \Omega$
b Power consumption against the variation of inductance values. $C = 10$ pF, aspect ratio = 100 μm/0.18 μm
c Power consumption against the variation of capacitance values. $L = 5$ nH, $R = 5\ \Omega$, aspect ratio = 100 μm/0.18 μm

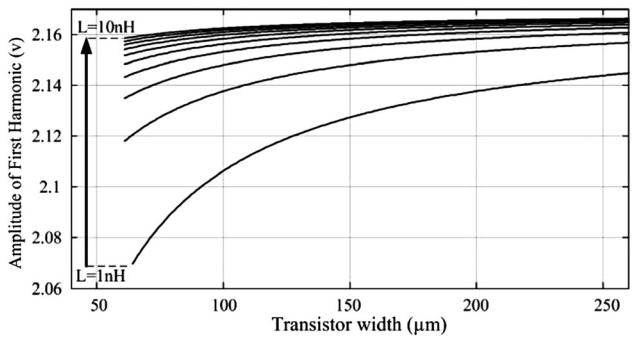

Fig. 11 *Variations of output voltage amplitude with regards to inductance value and bias current*

Inductance value is swept from 1 to 10 nH by 1 nH increment. ($f = 1.5$ GHz and is kept constant and the aspect ratios of transistors are equal to 100 μm/0.18 μm)

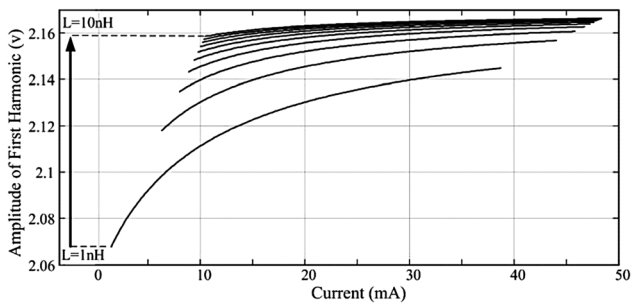

Fig. 12 *Variations of output voltage amplitude with regards to inductance value and transistors sizes*

Inductance value is swept from 1 to 10 nH by 1 nH increment. ($f = 1.5$ GHz and is kept constant and the aspect ratios of transistors are equal to 100 μm/0.18 μm)

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function of x or transistors sizes. When the inductance is increased, the second part of (13) becomes smaller and it does not have any critical effect on B_1 and the value of first harmonic will be approximately constant [according to (1) and (3), if the Q and ω are constant, R_{eq} is a direct function of R which is increased by increasing the inductance value].

In [8], two important concepts of 'waste of inductance' and 'waste of power' in the voltage-limited regime are defined. In this work, two similar concepts of 'waste of inductance' and 'waste of transistors sizes' are presented. Increasing L beyond the value that puts the oscillator at the edge of the voltage-limited regime will degrade the noise performance in proportion to the excess inductance [8], and hence will result in waste of inductance. Similarly, increasing the transistors sizes which lead to a higher bias current in excess of the value that places the oscillator at the borderline of the two regimes will not improve the noise performance of the oscillator and therefore induces the more commonly appreciated concept of waste of power [8]. The borderline of these two regimes can be obtained from (13). When the second part in (13) becomes very smaller than the first part, oscillator enters the voltage-limited regime. Therefore the condition of entering the voltage-limited regime is

$$xR_{eq} \gg \frac{2}{A_0 + V_T} \tag{28}$$

A smaller inductance results in better noise performance for a given bias current [8]. The optimum inductance for optimum noise performance is obtained when the design lies at the verge of the tank amplitude or startup constraint.

Another effect of increasing the inductance value is on oscillation frequency. According to (23) and (24), a larger inductance leads to a smaller K_0 (or higher non-linearity behaviour) and therefore more frequency error occurs for a constant production of L and C. The variations of oscillation frequency as a function of inductance and transistors sizes are shown in Fig. 13. According to Fig. 13, the minimum achievable inductance value is desirable to have more precise oscillation frequency.

6 Design procedure

Design constraints for a LC VCO are imposed on power dissipation, output voltage swing, frequency tuning range, startup condition and die area.

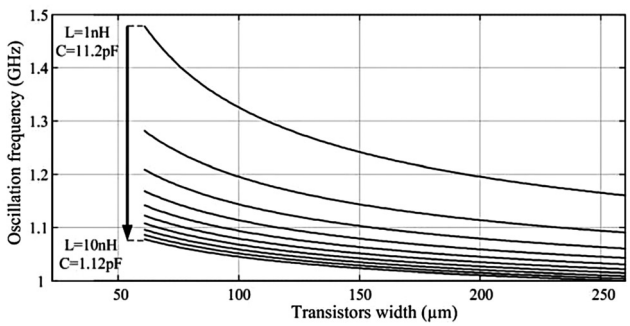

Fig. 13 *Variations of output voltage oscillation frequency with regards to inductance value and transistors sizes*

Inductance value is swept from 1 to 10 nH by 1 nH increment (production of L and C is kept constant for $f = 1.5$ GHz and the aspect ratios of transistors are equal to 100 μm/0.18 μm)

First, the maximum power constraint is imposed in the form of the maximum bias current drawn from a given supply voltage, that is

$$V_{supply} I_{bias} \leq P_{DC,MAX} \tag{29}$$

Second, the tank amplitude is required to be larger than a certain value determined by the succeeding stage.

The tuning range of a VCO is required to be in excess of a certain minimum percentage of the centre frequency, ω_0. The LC tank is made tunable by implementing the capacitor of the LC tank using a varactor.

Finally, the on-chip spiral inductors take a relatively large area. Therefore the length of the edge of the square in which the inductor is laid out should be smaller than a specified value ($d < d_{max}$) [8].

Now, according to the above mentioned constraints, a design procedure is presented. The goal of the design is to develop a LC VCO which meets the above constraints with minimum power. The design procedure is as follows:

(i) For a certain oscillation frequency (for a constant product of L and C) and according to (12), (13) and (16) a set of curves similar to Fig. 12 can be plotted. These curves show the amplitude of the output voltage as a function of the inductance and transistor sizes. Then, the crossing points of the line specifying the desired amplitude and the curves show the appropriate range of inductance and transistors sizes when the required amplitude can be achieved. According to the previous section, the smallest values of inductance and transistors sizes are the best choices.

(ii) According to the obtained values of stage (i) and (23), (24), the oscillation frequency as a function of the capacitor is obtained. Then, by solving the non-linear (23), the value of C for a specific oscillation frequency is achieved.

7 Conclusion

In order to obtain a better understanding of the cross-coupled oscillator, analytical equations were obtained in this paper. Based on these equations it is possible to estimate the effect of different circuit parameters on oscillation amplitude and frequency. For the frequency, an empirical equation was found by curve fitting which has an excellent agreement with simulations. Using this equation, it was shown that the non-linearity of the transistors has a great effect on oscillation frequency and makes it different from what is obtained from the well known $1/\sqrt{LC_{tot}}$ equation. According to the equations, a discussion about the circuit behaviours were presented and a design procedure for having minimum power is introduced.

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