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Step-by-step design and tuning of VOC control loops for grid connected rectifiers

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ABSTRACT

To address major concerns about the grid connected phase-controlled rectifiers, such as highly distorted grid currents, a poor input power factor, and a very slow dynamic performance, the voltage source PWM rectifiers have attracted great attentions today. As an advanced control strategy, the voltage-oriented control (VOC), is widely used to control the grid connected converters. The VOC uses the concept of decoupled active and reactive current components in the synchronous reference frame (SRF). Though, the VOC has been well documented in its theoretical aspects, but the absence of systematic design guidelines, that also cover the practical aspects such as analog anti-aliasing filtering and digital implementation delays, is obvious.

Based on the symmetrical optimum (SO), and its extended version (ESO), this paper presents step-by-step guidelines for designing the near-optimum ac current and dc voltage controllers of the VOC controlled grid connected rectifiers, with considering all practical aspects. Also, the effect of controllers' parameters on the performance of the converter is explained. Extensive simulation and experimental results are provided which confirm the validity of the proposed technique.

Introduction

Addressing the ever increasing global demand on power quality issues associated to the grid connected rectifier circuits, the use of pulse width-modulated (PWM) rectifiers, consisting of the same power circuit topology as PWM inverters, has grown rapidly. If wisely controlled, these circuits can meet the guidelines for harmonic mitigation [1,2], while providing bidirectional power flow capability, and low distortions at the dc-side voltage. Another promising feature is that they can independently control the dc-link voltage and the power factor; therefore, they can improve the voltage profile, and are able to operate in weak ac systems [3-11].

Advanced control strategies for grid connected converters use the concept of decoupled active and reactive power control which is realized in the synchronous reference frame (SRF). In this way, which is known as the voltage-oriented control or VOC, the ac current is decoupled into active and reactive components, i_d and i_q, respectively. These current components are then regulated in order to eliminate the error between the reference and measured values of the active and reactive powers. In most cases, the active current component, i_d, is regulated through a dc-link voltage control aiming at balancing the active power flow in the system, and the reactive component, i_q, is set to zero to achieve the unity power factor operation. The VOC for grid connected rectifiers has been well documented in its theoretical aspects [9-11]. However, the absence of systematic design guidelines, that also cover the practical aspects such as analog anti-aliasing filtering and digital implementation delays, is obvious.

Based on the symmetrical optimum (SO), and its extended version (ESO), this paper presents step-by-step guidelines for designing the near-optimum ac current and dc voltage controllers of the VOC controlled grid connected rectifiers, with considering all practical aspects. Also, the effect of controllers' parameters on the performance of the converter is explained. Theoretical achievements are confirmed through extensive simulations and experiments.

Inner current control loop

As mentioned before, the inner current control is performed in the synchronous reference frame (SRF) where all quantities are dc. So due to the great simplicity of dealing with dc systems, the controller design and parameters tuning are also performed in the SRF

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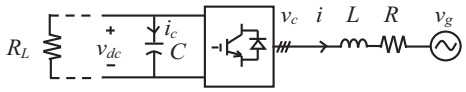


Fig. 1. Power circuit of grid-connected voltage-source converter.

[10,15]. To derive the equations of the grid-connected converter, we start with the following equations obtained from the power circuit of Fig. 1.

$$\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} - \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{1}$$

By applying the Park transformation in the stationary reference frame to (1), then we will obtain

$$\vec{v}_{c\alpha\beta} - \vec{v}_{g\alpha\beta} = L\frac{d}{dt}\vec{i}_{\alpha\beta} + R\vec{i}_{\alpha\beta}. \tag{2}$$

Considering that $\vec{x}_{\alpha\beta} = \vec{x}_{dq}e^{j\omega t}$, (2) will change to (3) in the SRF.

$$\vec{v}_{cdq} - \vec{v}_{gdq} = L\frac{d}{dt}\vec{i}_{dq} + (R + jL\omega)\vec{i}_{dq} \tag{3}$$

Eq. (3) is decoupled to d and q components and transformed to the Laplace domain as shown in equation set (4), where s in the Laplace operator.

$$\begin{cases} v_{cd} - v_{gd} = (Ls + R)i_d - L\omega i_q \\ v_{cq} - v_{gq} = (Ls + R)i_q + L\omega i_d \end{cases} \tag{4}$$

It is clear from (4) that the converter equations in the d and q axes are coupled to each other through $L\omega i_d$ and $L\omega i_q$ terms. Assuming that $G_c(s)$ is the current controller transfer function in the SRF, then the block diagram of the closed-loop current control scheme for the d-axis is shown in Fig. 2. The PWM modulator delay and the sampling and calculation time of the discrete control system are included in this model as a pure time delay T_d. A time delay of T_d in the Laplace domain is described as $e^{-T_d s}$. In order to include the effect of control delay in the system modeling and controller design, $e^{-T_d s}$ is replaced by a first-order lag approximation, i.e. $1/(1 + T_d s)$. The $LPF(s)$ represents the overall effect of the hardware anti-aliasing filter at the A/D input and a possible digital low-pass filter in the current loop with the time constants T_{aaf} and T_{lfc}, respectively. Assuming the first-order low-pass transfer functions for these filters, the LPF block can be approximated in the low frequency region as

$$LPF(s) = \frac{1}{1 + \underbrace{\left(T_{aaf} + T_{lfc}\right)}_{T_{Fc}}s} = \frac{1}{1 + T_{Fc}s}. \tag{5}$$

As mentioned before and is obvious in Fig. 2, the controller in the d-axis is coupled to the q-axis current through $L\omega i_q$. So by adding the inverse term (i.e. $-L\omega i_q$) to the controller output, the control of i_d will be almost decoupled of i_q. Also, from the control point of view, adding the feedforward term v_d to the controller output reduces the feedback control effort, and offers faster and at the same time smoother transient response, especially at start-ups. On the other hand, adding the decoupling and feedforward terms reduces the current loop to a first-order plant and greatly simplifies the converter model and the controller design while improves the tracking performance. The resultant control scheme in presence of the decoupling and feedforward expressions is depicted in Fig. 3(a), which can be readily redrawn as Fig. 3(b).

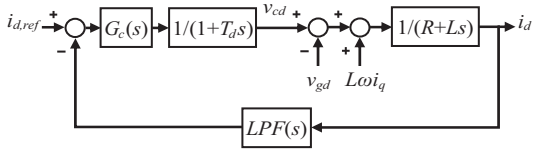


Fig. 2. Current control in SRF (d-axis).

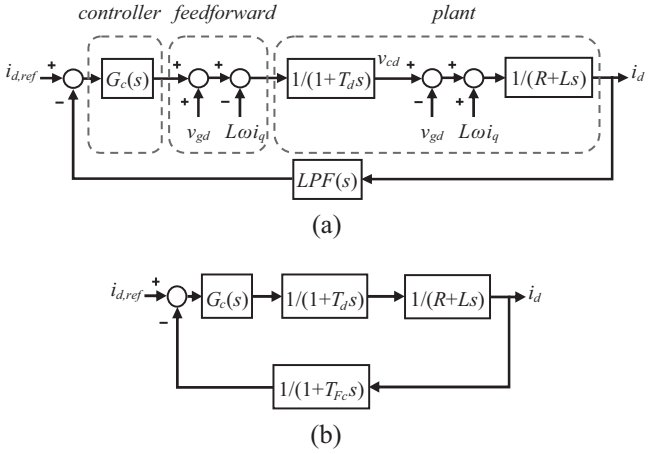


Fig. 3. (a) Current control in SRF with feedforward terms, and (b) simplified representation (d-axis).

While Figs. 2 and 3 are obtained for the d-axis, the same procedure as described before can be applied to the q-axis. In this case, the decoupling and feedforward terms are $+L\omega i_d$ and v_q, respectively, and the controller block diagram is again as Fig. 3(b). Accordingly the VOC in the SRF can be presented as Fig. 4.

Assuming a PI controller with the gain k_c and integrating time constant T_c for $G_c(s)$, the open current loop is concluded from Fig. 3(b) to be

$$H_c(s) = \underbrace{\frac{k_c(T_c s + 1)}{T_c s}}_{\text{PI controller}} \underbrace{\frac{1}{1 + T_{Fc}s}}_{\text{LPF}} \underbrace{\frac{1}{1 + T_d s}}_{\text{delay}} \underbrace{\frac{1}{R + Ls}}_{\text{inductive filter}}. \tag{6}$$

As mentioned before, T_d represents the delay introduced by the analog to digital converters, the program execution, and the PWM modulator. In most available digital platforms, this delay have a small value $T_d = 1.5T_s$, where T_s is the sampling period of the digital control system. Hence the loop gain transfer function is approximated by:

$$H_c(s) = \underbrace{\frac{k_c(T_c s + 1)}{T_c s}}_{\text{PI controller}} \underbrace{\frac{1}{1 + (T_{Fc} + T_d)s}}_{\text{LPF+delay}} \underbrace{\frac{1}{R + Ls}}_{\text{inductive filter}}. \tag{7}$$

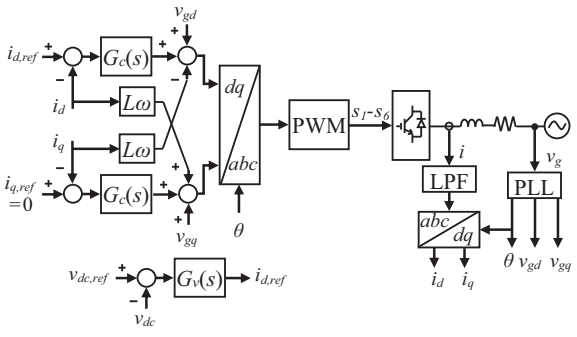


Fig. 4. Block diagram of VOC for grid-connected voltage-source converters.

For a system whose open-loop transfer function is given in (7), the parameters k_c and T_c may be chosen in accordance with the extended symmetrical optimum (ESO) which is developed in [12]. The ESO technique lets obtain the maximum possible phase margin (PM) at the specific control crossover frequency, ω_{cc}, by optimum shaping of the control loop Bode plots. Assuming that

$$m = \frac{T_{Fc} + T_d}{L/R} \ll 1 \tag{8}$$

then the best choice of control parameters is

$$T_c = \frac{b^2 T \Delta}{1 + m^2} \tag{9}$$

$$k_c = \frac{R\Delta}{bm} \tag{10}$$

where

$$\Delta = m^2 + (2 - b)m + 1 \tag{11}$$

$$T = \frac{T_{Fc} + T_d}{1 + m} \tag{12}$$

and b is determined from the desired PM

$$\mathrm{PM} = \tan^{-1}\left(\frac{b^2 - 1}{2b}\right). \tag{13}$$

Considering that the damping and PM of the system are related to each other, it can be concluded that the design constant b also plays a decisive role in the system transient response. Once a proper PM is chosen to achieve a sufficient stability margin as well as a fast dynamic response, b and consequently PI parameters are determined from (8) to (13). A phase margin in the range of 30–60° is recommended for most power electronic applications. Substituting PM = 45° into (13) gives $b = 1 + \sqrt{2}$.

According to the ESO method, the crossover frequency is related to b by (14).

$$\omega_{cc} = \frac{1}{b(T_{Fc} + T_d)} \tag{14}$$

As mentioned before, $T_d = 1.5T_s$. Also the anti-aliasing filter bandwidth is decided such that a proper attenuation at the half of the sampling frequency is achieved. However, a low bandwidth for the anti-aliasing filter limits the maximum achievable dynamic performance of the current loop and degrades the control loop stability. Then a bandwidth not greater than half of the sampling frequency may be a good compromise, i.e. $T_{Fc} = 2T_s$. With PM = 45° and $T_d + T_{Fc} = 3.5\ T_s$, the crossover frequency, f_{cc}, is obtained from (14) as:

$$f_{cc} = \frac{\omega_{cc}}{2\pi} \cong \frac{f_s}{50}. \tag{15}$$

It means that the bandwidth of the current regulator is approximately 50 times smaller than the sampling frequency, which may not be acceptable in most applications. For example, for this case that $f_s = 5$ kHz, then $f_{cc} = 100$ Hz which directly translates to a very slow dynamic performance as well as a poor harmonic rejection capability [13]. In order to improve the tracking performance and increase the rejection of external voltage disturbances, additional delays in the current control loop must be avoided. A solution to this problem is to minimize T_{Fc} by avoiding excessive anti-aliasing filtering. Synchronous sampling is a mean to reduce the risk of aliasing and to prevent the phase-lag associated to the analog anti-aliasing filters [14]. However, in particular cases where the performance of the synchronous sampling may not meet expectations and an analog anti-aliasing filter is employed, it is highly recommended to compensate the phase-lag in the ac signals by simply advancing the phase locked loop (PLL) output by the phase-lag of the anti-aliasing filters at the fundamental frequency. The amplitude at the concerned frequency usually remains unchanged and does not require any compensation. Once the phase-lag compensation is included in the control scheme, it can be readily assumed that $T_{Fc} = 0$ and (15) becomes

$$f_{cc} \cong \frac{f_s}{23} \tag{16}$$

which shows about 250% increase in the attainable crossover frequency.

Tuning of current controller parameters with the system parameters listed in Table 1 and $T_{Fc} = 0$ gives $T_c = 0.0017$, and $k_c = 5.4819$. The Bode plots of the open-loop current transfer function of (7) with these parameters are depicted in Fig. 5. As expected, the maximum PM (47°) happens at the crossover frequency (220 Hz as already predicted by (16)).

Outer dc voltage control loop

Considering the converter power circuit of Fig. 1, and neglecting the instantaneous power of the inductive filter, the input–output power balance equation, $p_{ac} = p_{dc}$, can be written as

$$-(v_{gd}i_d + v_{gq}i_q) = i_c v_{dc} + \frac{v_{dc}^2}{R_L} = C\frac{dv_{dc}}{dt}v_{dc} + \frac{v_{dc}^2}{R_L} = \frac{1}{2}C\frac{dv_{dc}^2}{dt} + \frac{v_{dc}^2}{R_L} \tag{17}$$

where C, v_{dc}, and R_L are the dc-link capacitance, voltage, and load, respectively. For a balanced three-phase grid and by using a PLL the SRF is oriented with the grid voltage vector. In other words, $v_{gq} = 0$, and $v_{gd} = \sqrt{3}/2V_g$; so dc-link voltage is proportional to d-axis component of the converter current. Applying the small-signal linearization to (17), while assuming that the dc load, R_L, exhibits a negligible dynamic behavior, gives (18), in which quantities with ^ are small perturbations around the dc values denoted by capital letters.

$$-\sqrt{\frac{3}{2}}V_g\left[I_d + \hat{i}_d\right] = \frac{1}{2}C\frac{d}{dt}\left[V_{dc}^2 + 2V_{dc}\hat{v}_{dc} + \hat{v}_{dc}^2\right] + \frac{\left[V_{dc}^2 + 2V_{dc}\hat{v}_{dc} + \hat{v}_{dc}^2\right]}{R_L} \tag{18}$$

Neglecting the high-order perturbations, the small-signal part of (18) can be extracted as:

$$-\sqrt{\frac{3}{2}}V_g\hat{i}_d = V_{dc}C\frac{d\hat{v}_{dc}}{dt} + \frac{2V_{dc}}{R_L}\hat{v}_{dc} \tag{19}$$

and the result in the Laplace domain (indicating with s the Laplace operator) becomes

$$\frac{v_{dc}(s)}{i_d(s)} = -\sqrt{\frac{3}{2}}\frac{V_g R_L}{V_{dc}(2 + CR_L s)}. \tag{20}$$

Table 1
System parameters.

Parameter	Symbol	Unit	Value
Filter inductance	L	mH	4
Filter resistance	R	Ω	0.25
Dc-link capacitance	C	μF	6000
Dc-link voltage	V_{dc}	V (dc)	120
Grid phase voltage	V_g	V (peak)	60
Grid voltage frequency	$f\,(\omega/2\pi)$	Hz	50
Nominal power	P	W	500
Sampling and switching frequency	$f_s\,(1/T_s)$	kHz	5

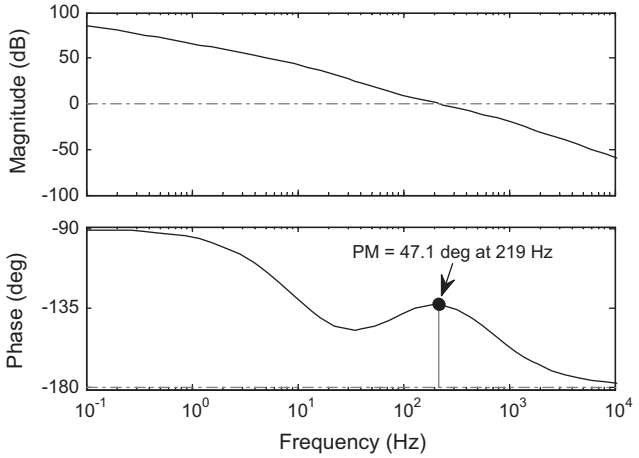


Fig. 5. Bode plots of $H_c(s)$ according to ESO method.

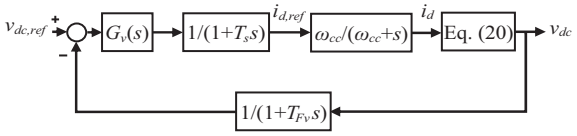


Fig. 6. Dc-link voltage control.

To control the dc voltage v_{dc} through the i_d current component, a PI controller is employed as presented in Fig. 6, where $G_v(s)$ is the voltage controller transfer function. The digital control system delay is modeled by a first-order low-pass filter with the time constant T_s and the overall effect of the anti-aliasing filter and the low-pass filter in the voltage loop is accounted for with a filter with the time constant T_{Fv} ($=T_{aaf}+T_{lfv}$) in the feedback path. The closed-loop current controller is also approximated in the low frequency range of interest, simply by a first-order low-pass filter with the cross-over frequency of ω_{cc} given in (14).

Assuming that the PI controller parameters are k_v, and T_v, the voltage loop gain is

$$H_v(s) = -\underbrace{\frac{k_v(T_v s+1)}{T_v s}}_{\text{PI controller}}\underbrace{\frac{1}{1+T_{Fv}s}}_{\text{LPF}}\underbrace{\frac{1}{1+T_s s}}_{\text{digital delay}}\underbrace{\frac{\omega_{cc}}{\omega_{cc}+s}}_{\text{current loop}} \times \underbrace{\frac{\sqrt{3}V_g}{\sqrt{2}V_{dc}\left(\frac{2}{R_L}+Cs\right)}}_{\text{DC link}}. \quad (21)$$

The dc-link voltage follows a very low bandwidth reference, such that the above transfer function can be effectively approximated by:

$$H_v(s) = \frac{K(1+T_v s)}{s(1+T_{sum}s)\left(\frac{2}{R_L}+Cs\right)} \quad (22)$$

in which $K = -\sqrt{\frac{3}{2}}\frac{k_v V_g}{T_v V_{dc}}$ and $T_{sum} = T_{Fv} + T_s + \frac{1}{\omega_{cc}}$.

It is obvious from (22) that the performance of dc-link voltage controller depends on the loading condition, i.e. R_L. From the stability point of view, the worst case is the no-load condition, where (22) simplifies to

$$H_v|_{R_L\to\infty}(s) = \frac{K(1+T_v s)}{Cs^2(1+T_{sum}s)}. \quad (23)$$

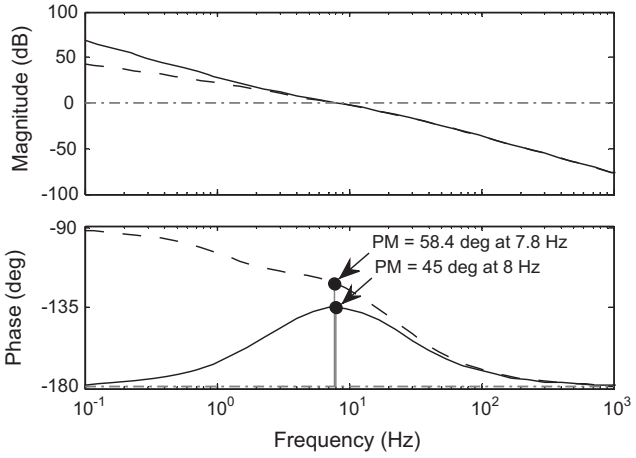
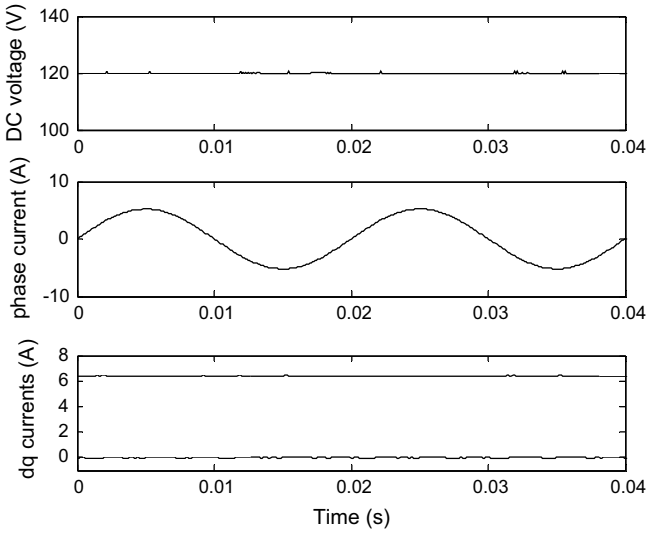
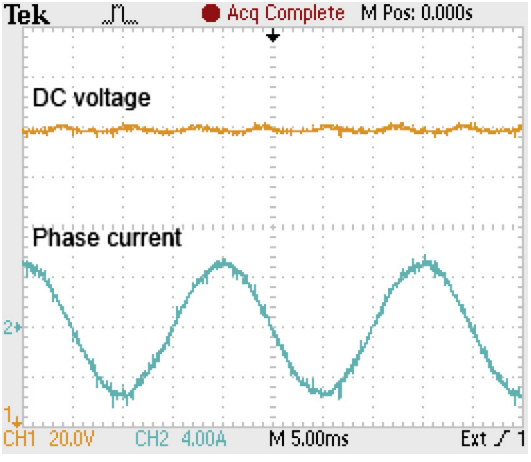


Fig. 7. Bode plots of $H_v(s)$ according to SO method under (dashed line) nominal load, and (solid line) no-load.



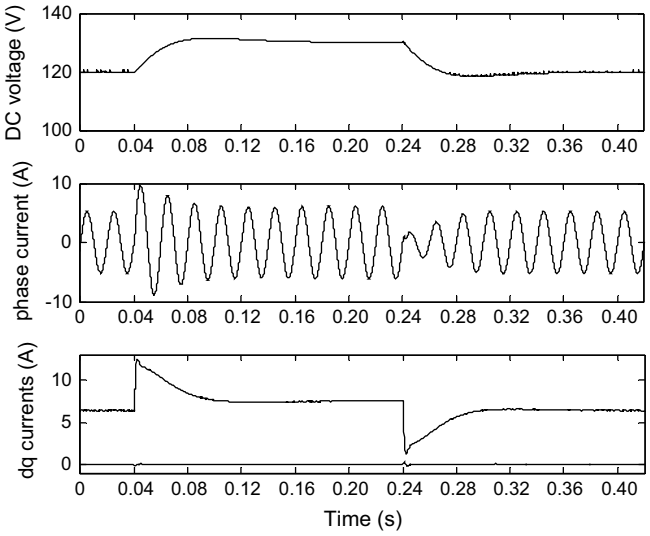
(a)



(b)

Fig. 8. Steady-state performance under nominal load: (a) simulated, and (b) experimental waveforms.

Although conservative, once the controller parameters are designed under the no-load condition, the minimum stability requirements will be certainly satisfied under all conditions from



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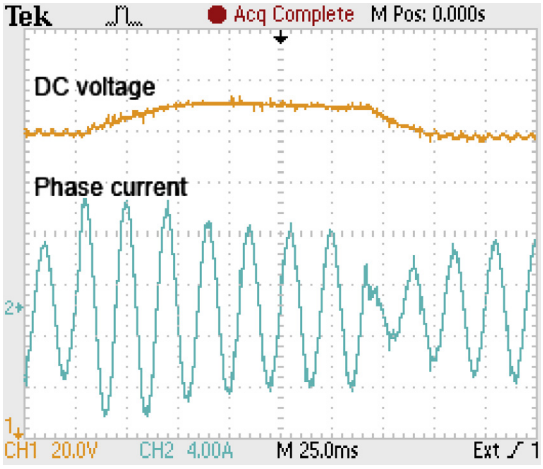


(b)

Fig. 9. Transient performance in response to step changes of dc voltage reference: (a) simulated, and (b) experimental waveforms.

no-load to full-load [15]. So, the voltage controller will be tuned under the no-load condition, then the stability requirements will be examined under different loading conditions.

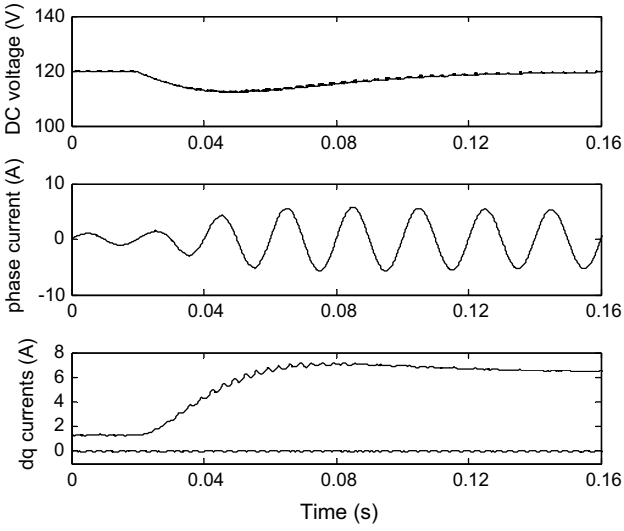
According to the symmetrical optimum (SO) method, for a system with an open-loop transfer function of the form (23) the control parameters are determined as [16]

$$T_v = \frac{b}{\omega_{cv}} \tag{24}$$

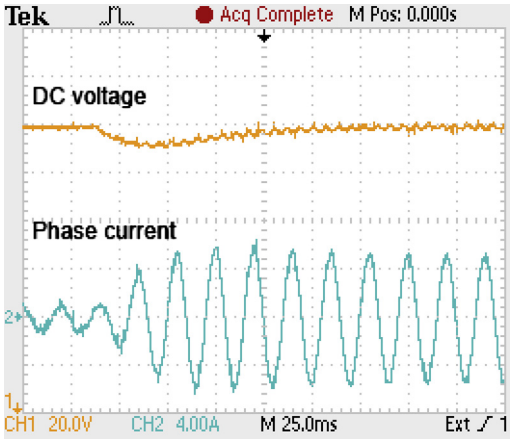
$$k_v = -\sqrt{\frac{2}{3}}\frac{CV_{dc}\omega_{cv}}{V_g} \tag{25}$$

$$T_{Fv} = \frac{1}{b\omega_{cv}} - T_s - \frac{1}{\omega_{cc}} \tag{26}$$

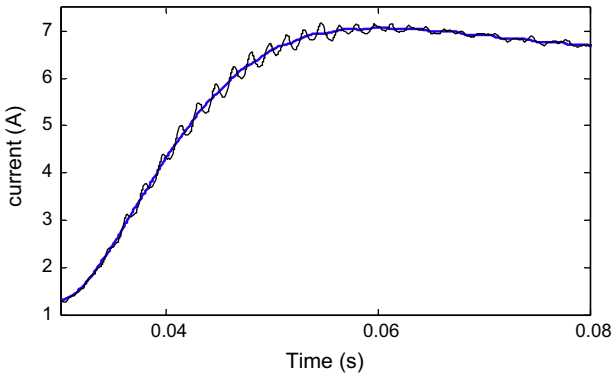
where ω_{cv} is the crossover frequency, and b is a design constant which determines the PM as shown in (14). The value of $1+\sqrt{2}$ is again selected for the design constant b, as this value makes the transient response well-damped and provides a PM of 45°. A bandwidth not bigger than one tenth of ω_{cc} ensures no interaction between current and dc voltage control loops. Any possible



(a)



(b)



(c)

Fig. 10. Transient performance in response to a jump of load current: (a) simulated, (b) experimental waveforms, and (c) zoomed view of d-axis current with its command.

interaction would cause deterioration in the dc voltage control loop performance. Practically, voltage loop bandwidth can be selected much lower, for example one tenth of the grid frequency, to prevent the low frequency oscillations of dc-link voltage to appear in the generated reference current. With this particular selection, the dynamic performance is sacrificed for better ac current [17]. In this work the crossover frequency is set as $\omega_{cv} = 50$ rad/s ($f_{cv} = 8$ Hz),

and consequently, T_v, k_v, and T_{Fv} are determined from (24) to (26) to be 0.0483, −0.49, and 7.4×10^{-3}, respectively. As can be seen, T_{Fv} is much higher than the time constant of any possible anti-aliasing filter for the dc voltage, so the controller is not almost affected by the analog filter. Besides the synchronous sampling, usually a low bandwidth analog anti-aliasing filter is used for the dc voltage, particularly when more than one static converter is connected to a common dc-link. For instance, a first-order filter with the time constant 0.6×10^{-3}, which can be safely ignored when compared with $T_{Fv} = 7.4 \times 10^{-3}$, attenuates the measured signal at the half of the sampling frequency of 5 kHz by a factor of 10. Next, in order to investigate the effect of rectifier load on the system performance, the Bode plots of the open-loop transfer function $H_v(s)$ under nominal load (dashed line), and no-load (solid line) are plotted in Fig. 7. From these plots, it can be concluded that, the design criteria are exactly attained under no-load design condition, while the PM and the closed-loop stability are slightly improved under nominal load condition.

Performance evaluation

To confirm the effectiveness of the proposed control strategy, the converter of Fig. 1 was simulated in MATLAB/Simulink. Practical effects such as regular sampling with 5 kHz frequency, non-ideality of IGBT switches, and dead-time delays are included in simulations to emulate the real system performance as closely as possible. Also, experimental verifications have been performed based on a TMS320F28335 digital signal controller from Texas Instruments. System parameters are the same for simulations and experiments and are summarized in Table 1.

The steady-state performance, the reference tracking capability, and the disturbance rejection are shown in Figs. 8–10, respectively. Fig. 8 demonstrates how the proposed control system can successfully provide an accurate regulation of dc-link voltage and at the same time, produce a perfect sinusoidal current with minimum switching noises and total harmonic distortion (THD = 0.56%) and a unity power factor ($i_q = 0$). Fig. 9 shows the performance of the proposed control scheme in response to step changes of dc voltage reference. One can see that while a fast voltage tracking with no over or undershoots in the dc voltage is obtained, but the ac current experiences high overshoots following a jump of voltage reference. This relieves that the output of dc-link voltage controller must be limited (saturated) to the overcurrent rating of the converter circuit. This limit will definitely increase the settling time of the dc-link voltage at step increases of its reference value. Fig. 10 shows the load disturbance rejection for an 80% step change in the load current. Only a slight decrease in the dc voltage can be observed at the instance of applying the full-load and the dc voltage recovers in less than three cycles, indicating that the proposed control technique brings a stiff dc voltage. Fig. 10(c) shows the commanded and measured d-axis current which confirms that the inner current controller response is almost instantaneous with negligible transients. This promising behavior is a consequence of providing enough control bandwidth (about 220 Hz) for the current control loop.

Conclusions

Based on the symmetrical optimum (SO), and its extended version (ESO), step-by-step guidelines for designing the near-optimum ac current and dc voltage controllers of the VOC controlled grid connected rectifiers in the frequency domain are proposed. Practical aspects such as delays introduced by analog anti-aliasing filtering and digital implementation are also considered. Extensive simulation and experimental results are provided which confirm the validity of the proposed technique.

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Appendix A.

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix}$$

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