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Radio-frequency modeling of square-shaped extended source tunneling field-effect transistors

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ABSTRACT

The radio-frequency (RF) performances and small-signal parameters of double-gate (DG) square-shaped extended source tunneling field-effect transistors (TFETs) with different gate lengths have been extracted and compared with those of conventional TFETs in terms of cut-off frequency, maximum oscillation frequency, current gain, unilateral power gain, gate-source capacitance, gate-drain capacitance, channel resistance, time constant and transconductance. The small-signal parameters have been extracted by using of a nonquasistatic radio-frequency model, which were verified up to 250 GHz. Because of the higher transconductance and current drivability and smaller gate capacitance of DG square-shaped extended source TFETs compared to conventional TFETs, DG square-shaped extended source TFETs have higher cut-off and maximum oscillation frequencies and smaller switching time. The impact of high-κ gate dielectric on RF figures of merit and device performance has also been investigated for extended source TFET. The results showed close agreement between the *Y*-parameters and the extracted parameters of modeling, SPICE simulation and device simulation for high frequency range up to the cut-off frequency.

1. Introduction

In the recent decade, due to unique characteristics such as steep sub-threshold slope (SS) and a very low leakage current, band-to-band tunneling (BTBT) tunneling field-effect transistors (TFETs)

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have attracted considerable attention as one of the promising candidates to replace MOSFET for ultra-low power applications [1–5]. TFET is basically a reverse biased gated p^+–i–n^+ structure where the gate bias modulates the position of energy bands in order to control interband tunneling between the source and the drain. In off-state for N-type TFET, the source valence band is located below the channel conduction band. Due to the large tunneling barrier in between the source and channel, the probability of the tunneling of electrons is negligible. So, the small off-state leakage current flows because of the reverse biased operation. Since the off-current induced by the tunneling directly from source to drain is very low, The TFET has higher scalability and better SCE immunity than a conventional MOSFET. Under the on-state condition, applying a positive gate voltage pulls the energy bands down and the channel conduction band goes below the source valence band and the band pass window is created. Thus, a sufficiently high lateral electric field is created at the source-channel junction, which forces the electrons to tunnel from the occupied valence band states of the source to the unoccupied conduction-band states of the channel through the narrow tunneling barrier between the source and the channel. For more details about working principles and advantages of TFET with the help of band diagrams can be found in [1].

Recently, researchers have reported devices with SS below 60 mV/decade at room temperature, both theoretically and experimentally [6–8]. Although a silicon-based TFET exhibits a minimized sub-threshold swing with a low off-current, their low on-current (typically 3–5 decades lower than MOSFET) was problematic due to the low interband tunneling [1]. In addition, the low on-current causes low transconductance and cut-off frequency. On the other hand, In terms of the 2015 International Technology Roadmap for Semiconductors (ITRS) requirements for multi-gate (MG) MOSFETs [9], an on-current of 614×10^{-6} A/μm is required, with a cut-off frequency of 443 GHz. Therefore, the biggest challenge is to successfully design and fabricate optimized TFETs that show simultaneously high on-current, low off-current and sub-threshold slope at room temperature. Due to low on-current of silicon-based TFETs, different techniques have been suggested to improve the on-current. On-current of TFETs can be enhanced by using band-gap engineering [10–17], small band-gap materials [18,19], high-κ dielectric materials [20], pocket doping [21–23], vertical direction tunneling [24] and extended source [25]. Second challenge is not fully the understanding device physics that causes questionable the applicability of WKB approximation for phonon or impurity scattering and indirect bandgap semiconductors, such as Si and Ge [26]. The analytical model for TFET that includes the effect of channel transport is the last challenge.

By extending the source into the middle of the TFET body underneath the gate, high electric field extends along the source-channel interface into the middle of the channel and many tunneling paths with short lengths are formed in the on-state, leading to an increase in on-current. The sub-threshold slope is also improved due to the better uniformity distribution of the high electric field along source-channel region [25,27]. In addition, for the TFET with short extended source length, effectively boosting the on-current with off-current being unchanged. This explains the large improvement in the I_{ON}/I_{OFF} ratio (more than 11 orders of magnitude) that is the importance of the extended source TFET [25]. The benefit of extended source design is more obvious for TFET when it is combined with other structures, such as the small band-gap materials or high-κ dielectric materials.

Although there have been reports on the design and optimization of square-shaped extended source structure for better performance in terms of sub-threshold swing and drive current [25,27], their RF characterization and modeling have been seldom reported.

In this paper, the double-gate (DG) square-shaped extended source TFETs with different gate lengths have compared with conventional TFETs in terms of RF performances and small-signal parameters. The small-signal parameters were extracted from the analytical equations for the Y-parameters of a nonquasistatic (NQS) radio-frequency model for analysis of cut-off frequency, maximum oscillation frequency, gate-source capacitance, gate-drain capacitance, channel resistance, time constant and transconductance. The rest of this paper is organized as follows: Section 2 describes the device structures, calibration of the nonlocal band-to-band tunneling model and radio-frequency model of extended source TFETs. Section 3 presents the results and discussion. In Section 4, validation of the radio-frequency model of extended source TFETs is presented. Finally, we conclude in Section 5.

2. Device structure, calibration of the nonlocal band-to-band tunneling model and radio-frequency model of extended source TFETs

Fig. 1(a) and (b) shows cross-sectional views of the DG square-shaped extended source and conventional TFET devices used in the two-dimensional device simulation [28]. The simulated device is a Si-channel doping concentrations $N_A = 1 \times 10^{15}\,cm^{-3}$ with a 30 nm channel length, source and drain doping concentrations $N_A = N_D = 1 \times 10^{20}\,cm^{-3}$ with extension length of 25 nm, silicon body thickness of 15 nm, 2 nm gate oxide thickness, 10 nm extended source length, 5 nm extended source thickness and gate metal work functions of 3.8 eV. In order to meet ITRS requirement, the device was also compared with two different gate dielectrics: SiO_2 ($\kappa = 3.9$) and ZrO_2 ($\kappa = 29$) [20]. For higher accuracy, band-to-band tunneling has been modeled using a nonlocal path tunneling approach for the device performance calculations. The nonlocal band-to-band tunneling model used in the two-dimensional device simulation was previously calibrated [29] with the experimentally reported data [30] for HfO_2 at $V_{DS} = -1$ V. The rest mass of an electron, electron effective mass and hole effective mass are the band-to-band tunneling parameters of the nonlocal band-to-band tunneling model in the device simulation. Since the tunneling probability depends exponentially on the effective masses, band-to-band tunneling current is most sensitive to them. Therefore, to calibrate the nonlocal band-to-band tunneling model, should be specified the values of effective mass [28]. Fig. 2 shows the comparison of our simulation results of the nonlocal band-to-band tunneling model with the experimental data [30] for SiO_2 at $V_{DS} = -1$ V. The electron and hole effective masses are replaced from 0.322 to 0.4 and 0.549 to 0.52 to obtain the best fit with the experimental data [30], while rest mass of an electron is its default value of 0.25. Due to high doping concentration and high impurity atom in the channel, band-gap narrowing and Shockley–Read–Hall recombination models are also enabled. The mobility, auger recombination and trap-assisted-tunneling models are also activated [3,31,32].

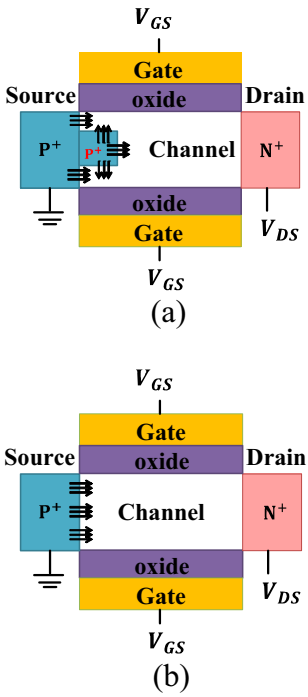

Fig. 1. Cross-section views of the (a) square-shaped extended source TFET and (b) conventional TFET structures.

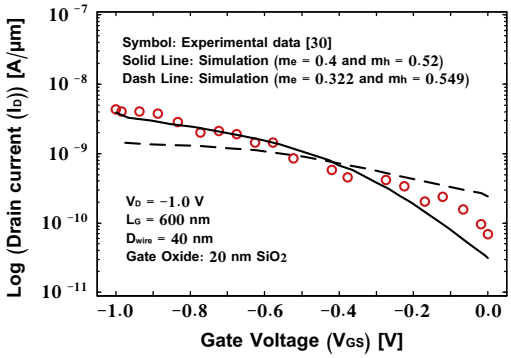

Fig. 2. Comparison of our simulation results of the nonlocal band-to-band tunneling model with the experimental data [30] for SiO_2 at $V_{DS} = -1$ V.

For a conventional TFET structure, the DG architecture has already been demonstrated experimentally [33] that the fabrication process is similar to that described in [34] except that the source and drain are doped p^+ and n^+, respectively. Furthermore, the fabrication of a silicon nanowire (Si NW) TFET with different gate stacks was presented in [30]. Many of the process steps involved in fabrication of square-shaped extended source TFET are the same as the DG and NW conventional TFET technology. One of the different possible process flow compatible with conventional TFET process to fabricate the square-shaped extended source TFET is the modification of ion implantation steps in the conventional TFET fabrication process proposed in [30] or [33]. Before the gate stack formation, square-shaped doping region is formed by B^+ implantation with high energy and low current using a separate mask. A process flow for vertical square-shaped extended source TFET has already been proposed in [27], wherein p^+-core can be achieved by the nanocluster-catalyzed vapor–liquid–solid (VLS) method and then deposition of the intrinsic outer shell at a higher temperature and lower pressure than for p-core growth as reported in [35].

Fig. 3(a) and (b) compare BTBT generation rate for square-shaped extended source and conventional TFET with 30 nm gate length in the on-state ($V_{GS} = V_{DS} = 0.7$ V) in contour plot and horizontal cut-line at 1 nm below the oxide–silicon interface, respectively. As seen, an extensive high BTBT generation rate region is observed along the source-channel edge for the square-shaped extended source TFET. In other words, square-shaped extended source increases tunneling junction area. Also due to the higher total electric field between the source and channel at 1 nm away from the oxide–silicon interface, square-shaped extended source TFET shows the higher BTBT generation rate, as seen from Fig. 3(b). As a result, due to the larger region available for electrons to tunnel from the source to the channel, the total tunneling current increases in the on-state [25].

Fig. 4 shows the nonquasistatic equivalent circuit of a transistor to extract small-signal parameters of square-shaped extended source and conventional TFETs that is based on a conventional small-signal model of MOSFETs for microwave modeling [36]. Recently, it has been shown that the conventional small-signal model of MOSFETs could be adopted to evaluate RF performance of nanoscale TFETs [37]. R_g is the effective gate resistance. C_{gs}, C_{gd} and C_{sd} are the gate-source, gate-drain and source-drain capacitance values, respectively. Time constant τ, g_m and g_{ds} are the charge transport delay, transconductance and source-drain conductance, respectively. The Y-parameters of the NQS model equivalent circuit can be expressed as follows [36]:

$$Y_{11} = \frac{\omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega(C_{gs} + C_{gd})}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} \tag{1}$$

$$Y_{12} = \frac{-\omega^2 R_g C_{gd}(C_{gs} + C_{gd}) - j\omega C_{gd}}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} \tag{2}$$

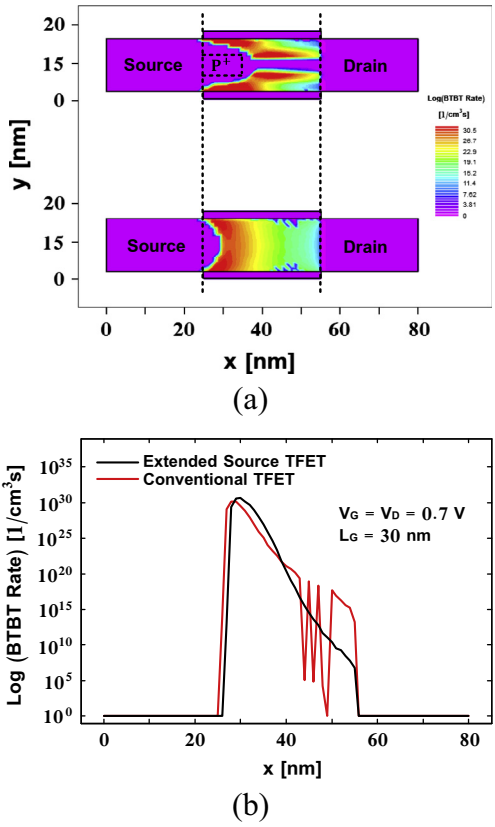

Fig. 3. Comparison of BTBT generation rate for square-shaped extended source and conventional TFET with 30 nm gate length in the on-state ($V_{GS} = V_{DS} = 0.7$ V). (a) Contour plots and (b) along the horizontal cut-line at 1 nm below the oxide-silicon interface.

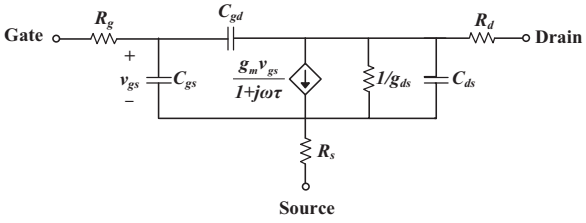

Fig. 4. Nonquasistatic equivalent circuit of a transistor to extract small-signal parameters of square-shaped extended source TFETs by the *Y*-parameter analysis.

$$Y_{21} = \frac{-j\omega C_{gd} - \omega^2 R_g C_{gd}(C_{gs}+C_{gd})}{1+\omega^2 R_g^2 (C_{gs}+C_{gd})^2} + \frac{g_m - j\omega g_m[\tau + R_g(C_{gs}+C_{gd})] - \omega^2 R_g g_m \tau (C_{gs}+C_{gd})}{[1+\omega^2 R_g^2 (C_{gs}+C_{gd})^2](1+\omega^2\tau^2)} \tag{3}$$

$$Y_{22} = g_{ds} + j\omega(C_{gd}+C_{sd}) + \frac{\omega^2 R_g C_{gd}^2}{1+\omega^2 R_g^2 (C_{gs}+C_{gd})^2} + \frac{j\omega R_g g_m C_{gd} + \omega^2 R_g g_m C_{gd}[\tau + R_g(C_{gs}+C_{gd})]}{[1+\omega^2 R_g^2 (C_{gs}+C_{gd})^2](1+\omega^2\tau^2)} \tag{4}$$

In order to extract the small-signal parameters appropriate for low-frequency region, assumptions that $\omega^2 R_g^2 (C_{gs} + C_{gd})^2 \ll 1$ and $\omega^2 \tau \ll 1$ have been used [36]. However, the validity of the assumptions will be checked by using the extracted parameters. Consequently, the equations of *Y*-parameters can be approximated into simple forms as follows [36]:

$$Y_{11} \approx \omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega (C_{gs} + C_{gd}) \tag{5}$$

$$Y_{12} \approx -\omega^2 R_g C_{gd} (C_{gs} + C_{gd}) - j\omega C_{gd} \tag{6}$$

$$Y_{21} \approx g_m - \omega^2 R_g (C_{gs} + C_{gd})(C_{gd} + \tau g_m) - j\omega [C_{gd} + \tau g_m + g_m R_g (C_{gs} + C_{gd})] \tag{7}$$

$$Y_{22} \approx g_{ds} + \omega^2 R_g C_{gd} \{C_{gd} + g_m [\tau + R_g (C_{gs} + C_{gd})]\} + j\omega [C_{gd} + C_{sd} + R_g g_m C_{gd}] \tag{8}$$

By using real and imaginary parts of Eqs. (5)–(8) and the *Y*-parameters from the simulation results, the small-signal parameters governing the RF behaviors can be extracted. The analytical values of g_m, g_{ds}, R_g, C_{gd}, C_{gs}, C_{sd} and τ can be obtained by Eqs. (9)–(15) as follows [36]:

$$g_m = \mathrm{Re}[Y_{21}]|_{\omega^2=0} \tag{9}$$

$$g_{ds} = \mathrm{Re}[Y_{22}]|_{\omega^2=0} \tag{10}$$

$$R_g = \frac{\mathrm{Re}[Y_{11}]}{(\mathrm{Im}[Y_{11}])^2} \tag{11}$$

$$C_{gs} = \frac{\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}]}{\omega} \tag{12}$$

$$C_{gd} = -\frac{\mathrm{Im}[Y_{12}]}{\omega} \tag{13}$$

$$\tau = -\frac{\frac{\mathrm{Im}[Y_{12}]}{\omega} + C_{dg} + g_m R_g (C_{gs} + C_{gd})}{g_m} \tag{14}$$

$$C_{sd} = \frac{\mathrm{Im}[Y_{22}]}{\omega} - C_{gd} - R_g g_m C_{gd} \tag{15}$$

3. Results and discussion

Fig. 5(a) and (b) illustrates the drain current (I_D) and transconductance (g_m) dependence of an extended source and conventional TFET with different gate lengths on the gate voltage (V_{GS}), respectively. Since the current conduction is caused by the band-to-band tunneling in the source side, effective tunneling width is constant with varying gate length. Therefore, the values of on-current and transconductance are invariable for different gate lengths. As shown in Fig. 5(a), extended source TFETs have higher on-current than conventional TFETs. It should be mainly due to the higher tunneling junction area and total electric field between the source and channel that increase the total band-to-band generation [25]. So, the more electrons in the valence band of the source can tunnel through the barrier and reach the conduction band of the channel, which results higher on-current than conventional TFETs. For modeled conventional TFET structure with 30 nm gate length, on-current and off-current are 2.23×10^{-7} A/μm and 1.12×10^{-16} A/μm, respectively, which have close to the experimental results of around 0.55×10^{-7} A/μm and 1×10^{-16} A/μm, respectively [33]. As can be seen in Fig. 5(b), the improvement of I_D leads to an increase in the transconductance of extended source TFETs. The I_{ON}/I_{OFF} ratio as a function of gate length for extended source and conventional TFET at $V_{DS} = 0.7$ V is shown in Fig. 5(c). Off-current (I_{OFF}) is defined to be the minimum drain current, occurring at $V_{GS} = 0$ V and $V_{DS} = 0.7$ V, while on-current (I_{ON}) is defined at $V_{GS} = V_{DS} = 0.7$ V. As seen,

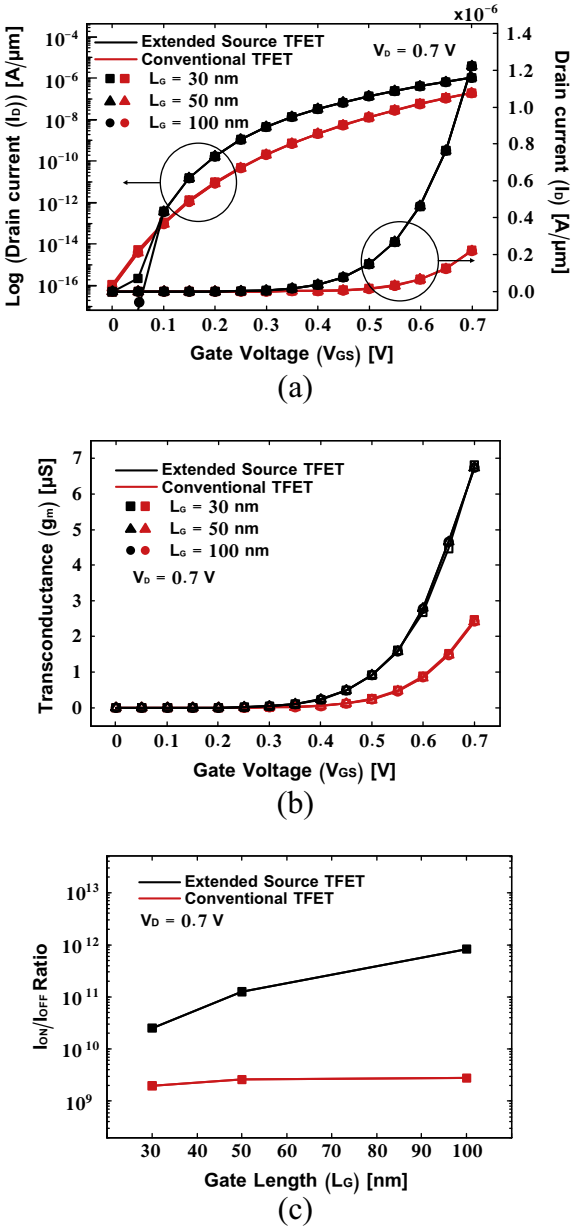

Fig. 5. (a) The transfer characteristics comparison of an extended source and conventional TFET in linear and logarithm scales at V_{DS} = 0.7 V with different gate lengths and (b) comparison of transconductance (g_m) between an extended source and conventional TFET at various gate lengths values as a function of gate voltage (V_{GS}). (c) The I_{ON}/I_{OFF} ratio versus gate length for extended source and conventional TFET at V_{DS} = 0.7 V.

I_{ON}/I_{OFF} ratio increases more than one order of magnitude for the shortest gate length devices. The 100 nm extended source TFET retains the excellent ON–OFF switching up to 8.4×10^{11}.

Fig. 6 displays the gate capacitance values of the extended source and conventional TFET with different gate lengths as a function of V_{GS}. C_{gd} is the preponderant component in the capacitance between the gate and the inversion layer which should be mainly due to the formation of inversion layer of a

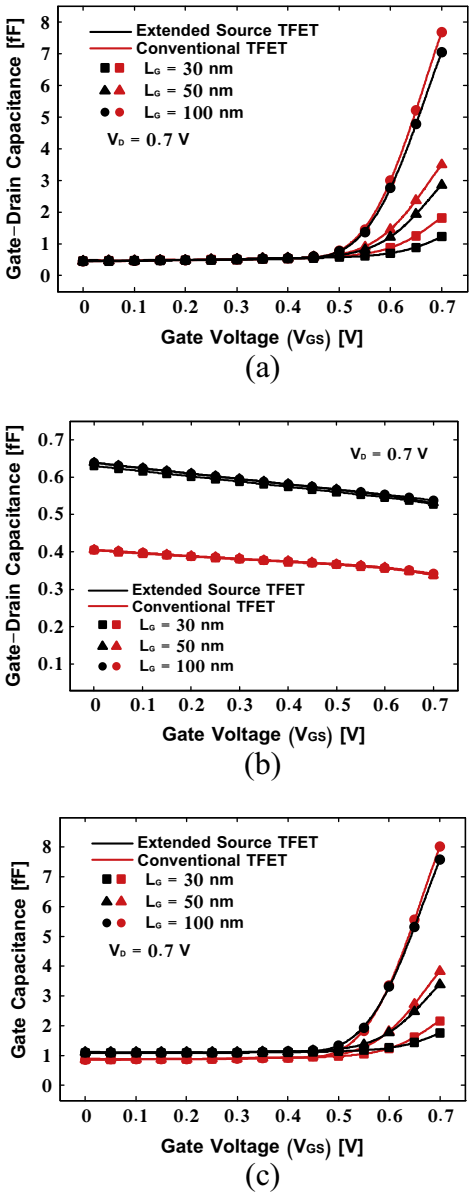

Fig. 6. Gate capacitance values of the extended source and conventional TFET at various gate lengths values as a function of V_{GS}. (a) Gate-drain capacitance, (b) gate-source capacitance and (c) gate capacitance.

TFET from the drain side toward the source side with increasing of V_{GS} [38]. Increase in the V_{GS} causes gate-drain capacitance extremely increases which is proportional to gate length, as can be confirmed in Fig. 6(a). On the other hand, the extension of the inversion layer from the drain side toward the source side leads to fewer coupling between the gate and the source [38]. Therefore, the gate-source capacitance monotonically decreases with increasing V_{GS}, as shown in Fig. 6(b). In the case of the extended source TFET, the values of C_{gs} are larger than those of the conventional TFET. Because the

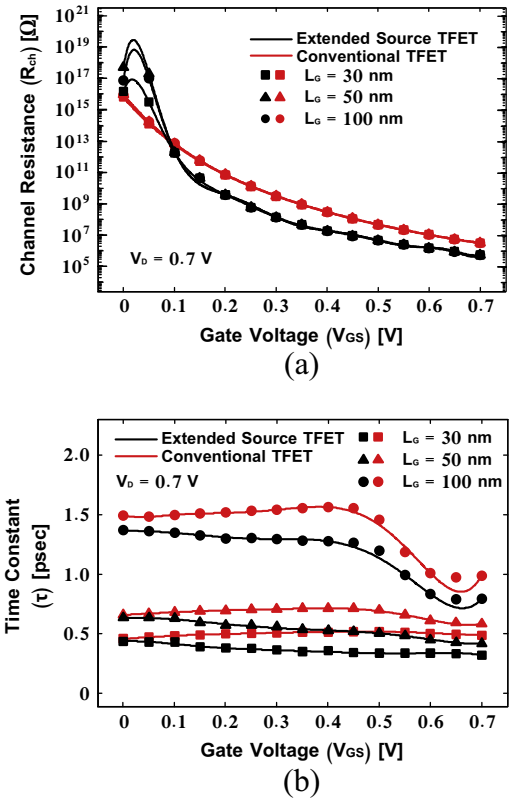

Fig. 7. (a) Channel resistance (R_{ch}) and (b) time constant of the extended source and conventional TFETs as a function of gate voltage (V_{GS}) for different gate lengths.

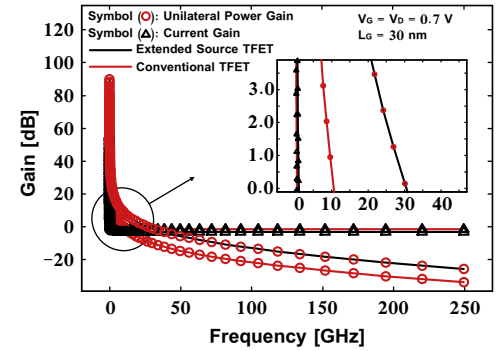

Fig. 8. The current gain and unilateral power gain of the extended source TFETs and the conventional TFETs with 30 nm gate length at $V_{GS} = V_{DS} = 0.7$ V.

source area in the extended source TFET is much larger than that of conventional TFET. From Fig. 6(c), it turns out that the C_{gg} values of the extended source TFET are close to those of conventional TFET in the low V_{GS} region because of larger source area in the extended source TFET before the formation of

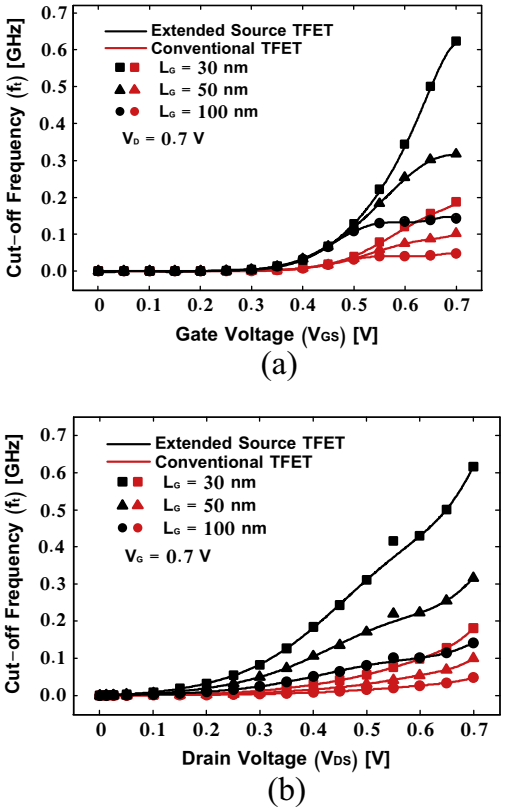

Fig. 9. Comparison of the f_T value between the extended source TFETs and the conventional TFETs with different gate lengths for different gate length values as a function of (a) V_{GS} and (b) V_{DS}.

inversion layer. In the high V_{GS} region, due to the formation of inversion layer, C_{gd} is the preponderant component. Consequently, C_{gg} values of the extended source TFET are lower than that of conventional TFET.

Fig. 7 demonstrates the influences of the gate voltage on the channel resistance (R_{ch}) and time constant of the extended source and conventional TFETs for different gate length values. Channel resistance is calculated by voltage divided by current in the device simulation and is equivalent to the inverse of g_{ds} in the Y-parameters. Since the on-current of a TFET did not change with gate length, the channel resistance is invariant with gate length as V_{GS} increases above 0.1 V. As seen from Fig. 7(a), the extended source TFET has smaller R_{ch} than the conventional TFET because of large channel conductivity induced by larger of the tunneling area and the total band-to-band tunneling rate in the on-state. Generally, the switching speed and time constant for the charging delay of transistors are dependent on gate capacitance and channel resistance [39]. Time constant for the charging delay is an important parameter in the NQS effects which shows how fast the channel charges respond to the input signal. The time constant for extended source TFET is much lower than that for conventional TFET, because extended source TFET has smaller channel resistance and gate capacitance at high voltages than conventional TFET, as can be confirmed from the data of transport delay (Fig. 7(b)). Consequently, switching speed of extended source TFETs can be higher than that of conventional TFETs.

The RF figures of merit for extended source TFETs are analyzed in terms of cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}). The values of the cut-off and maximum oscillation frequencies have been extracted by high-frequency current gain and unilateral power gain using the device-simulated Y-parameter data, respectively. The current gain and unilateral power gain of the extended

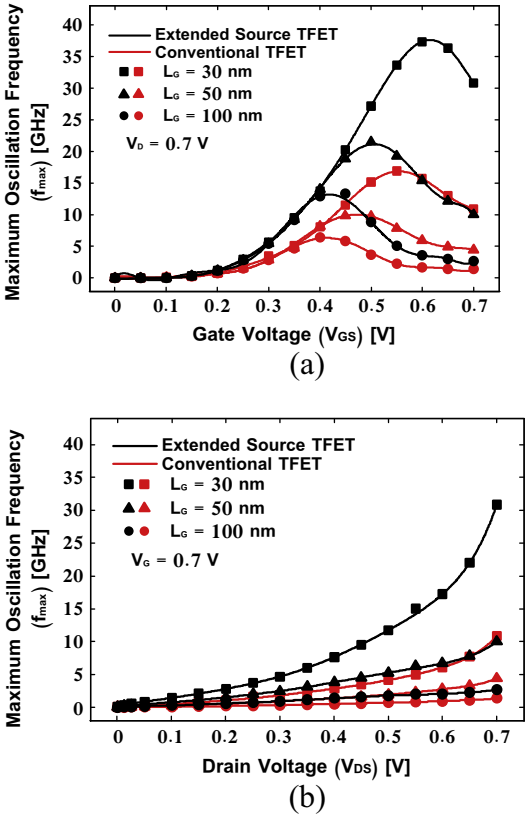

Fig. 10. Comparison of the f_{max} values between the extended source and conventional TFETs obtained from unilateral power gains at various gate lengths values as a function of (a) V_{GS} and (b) V_{DS}.

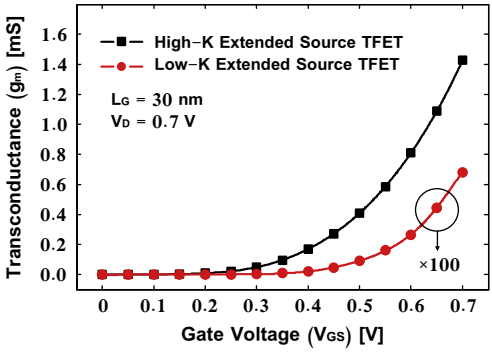

Fig. 11. The transconductance (g_m) comparison of the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length at V_{DS} = 0.7 V.

source TFETs and the conventional TFETs with 30 nm gate length at $V_{GS} = V_{DS} = 0.7$ V are presented in the Fig. 8. f_T is extracted when the current gain is unity, and f_{max} is extracted when Mason's unilateral power gain drops to unity [40]. The cut-off frequency and maximum frequency of oscillation obtained

are 0.62 GHz and 30.91 GHz for extended source TFET and 0.18 GHz and 10.9 GHz for the conventional TFET at $V_{GS} = V_{DS} = 0.7$ V, respectively.

Fig. 9 compares the f_T values of the extended source TFETs and the conventional TFETs for different gate length values as a function of V_{GS} and V_{DS}. Generally, the cut-off frequency depends on the g_m and C_{gg} ($f_T \sim \frac{g_m}{2\pi \times C_{gg}}$), which C_{gg} is the gate capacitance as the sum of C_{gs} and C_{gd}. Since the transconductance of a TFET is nearly constant and C_{gg} is proportional to gate length, the cut-off frequency of a TFET is inversely proportional to gate length. Due to the monotonic increase of g_m and C_{gg} with the increase of V_{GS} as shown in Figs. 5(b) and 6(c), f_T of TFETs have the rising tendency as a function of V_{GS}. It can be seen that the extended source structure shows the better RF performances as well as the switching speed than conventional TFETs because of the higher transconductance and current drivability and smaller gate capacitance at high V_{GS}. As V_{DS} increases, the gate capacitance decreases, and the transconductance rapidly increases because of the improvement in drain current [37]. Consequently, the cut-off frequency increases, as can be confirmed in the Fig. 9(b).

Fig. 10 demonstrates the effect of the gate and drain voltage on the f_{max} values of the extended source and conventional TFETs with different gate lengths obtained from unilateral power gains. As previously shown in Fig. 6(c), Figs. 7 and 9(a); due to lower channel resistance and C_{gg} at high voltages and higher f_T, extended source TFETs have higher f_{max} values than conventional TFETs. The maximum f_{max} values of the extended source and conventional TFETs were about 37.6, and 16.9 GHz at $V_{DS} = 0.7$ V for 30 nm gate length, respectively. Because the higher cut-off frequency and lower gate capacitance at higher V_{DS}, as shown in Fig. 10(b), TFET exhibits higher the maximum oscillation frequencies.

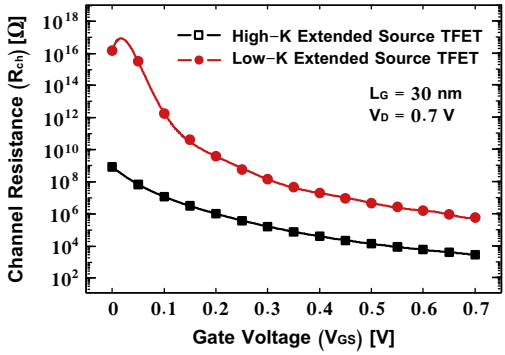

Fig. 12. Channel resistance (R_{ch}) of the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length at $V_{DS} = 0.7$ V as a function of gate voltage (V_{GS}).

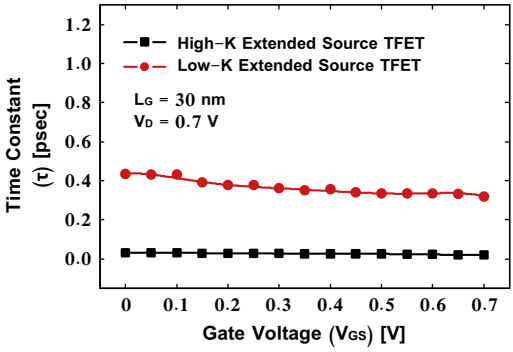

Fig. 13. Time constant of the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length at $V_{DS} = 0.7$ V as a function of gate voltage (V_{GS}).

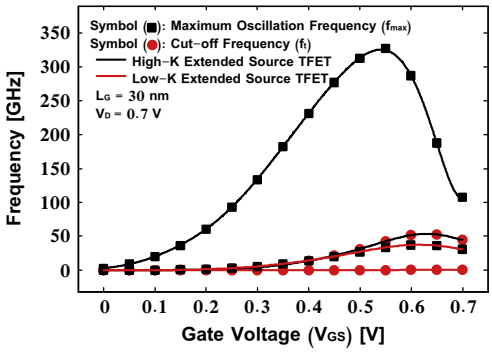

Fig. 14. Comparison of the f_T and f_{max} values between the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length at V_{DS} = 0.7 V as a function of gate voltage (V_{GS}).

The results indicate that extended source TFETs have higher cut-off and maximum oscillation frequencies and smaller switching time than conventional TFETs for high-frequency and high-switching-speed electronics applications.

In order to achieve improved RF figures of merit and performance with the aim of meeting the International Technology Roadmap for Semiconductors (ITRS) requirements for multi-gate (MG) MOSFETs projected to year 2015 [9], a high-κ gate dielectric is used, where high-κ material is ZrO_2 (κ = 29) whereas low-κ material is SiO_2 (κ = 3.9). Recently, *I–V* and capacitance characteristics of high-κ gate dielectric TFETs have been compared with that of low-κ gate dielectric TFETs [20,41]. Therefore, we have focused on the transconductance, channel resistance, time constant dependence and RF figures of merit in terms of cut-off frequency and maximum frequency of oscillation. Fig. 11 compares the transconductance values of the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length as a function of V_{GS} at V_{DS} = 0.7 V. Since high-κ gate dielectric TFET has smaller equivalent oxide thickness (EOT) compared to low-κ gate dielectric TFET, gate control over the channel of TFET enhances by high-κ gate dielectric, leading to an increase of the on-current [20]. As a result of enhanced on-current, TFET with high-κ gate dielectric shows a significant boost in transconductance as shown in Fig. 11.

Figs. 12 and 13 illustrate the channel resistance and time constant dependence of high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length on the gate voltage at V_{DS} = 0.7 V. Due to current improvement in the TFET with high-κ gate dielectric, TFET with high-κ gate dielectric shows much larger conductivity than low-κ gate dielectric TFET. Therefore, high-κ gate dielectric extended source TFETs show smaller channel resistance, as seen from Fig. 12. As can be confirmed from the data of time constant (Fig. 13), because of the smaller channel resistance, the time constant of a high-κ gate dielectric extended source TFET is much lower than that of the TFET with low-κ gate dielectric.

A comparative study of RF figures of merit between the high-κ and low-κ gate dielectric extended source TFETs with 30 nm gate length at V_{DS} = 0.7 V, is shown in Fig. 14. It can be seen that extended source TFET with the high-κ gate dielectric exhibits higher the cut-off and maximum oscillation frequencies. It should be mainly due to the higher transconductance as shown in Fig. 11. The DC and RF characteristics of the high-κ and low-κ gate dielectric extended source TFET in comparison with ITRS requirements, previous experimental results [37,41] and previous simulation results [33,42,43] are listed in Table 1. As seen, the high-κ gate dielectric extended source TFET is too high to fulfill the low-standby-power (LSTP) requirements for MG MOSFETs as well with the exception of the cut-off and maximum oscillation frequencies. Generally, the cut-off frequency of a TFET is lower than that of MOSFET. It should be mainly due to lower transconductance of TFETs than that of MOSFETs by more than an order of magnitude, and partially due to the higher gate capacitance [41].

Table 1
Comparison of the DC and RF between the 30 nm high-κ and low-κ gate dielectric extended source TFET with ITRS requirements for multi-gate (MG) MOSFETs projected to year 2015 and previous results.

Requirements	LSTP 2015 for MG MOSFETs [9]		Experimental results			Simulation results			
		Parameters	Double-gate Si TFETs [33]	InGaAs/GaAsSb near broken-gap TFET [42]	SOI TFET [43]	Double-gate TFETs [41]	Gate-all-around TFETs [37]	Current work with low-κ gate	Current work with high-κ gate
		L_G (nm)	15	200	170	50	30	30	30
		V_{GS} (V)	1.2	2.5	2.0	1.0	1.0	0.7	0.7
		Gate dielectric	0.7 nm non-defined	1 nm Al_2O_3	4.5 nm non-defined	1 nm EOT	Non-defined	2 nm SiO_2	2 nm ZrO_2
V_{DD} (V)	0.81		0.7	0.5	1.2	1.0	1.0	0.7	0.7
I_{ON} (A/μm)	614×10^{-6}		0.55×10^{-7}	7.4×10^{-4}	2×10^{-9}	5×10^{-6}	–	1.22×10^{-6}	4.13×10^{-4}
I_{OFF} (A/μm)	10×10^{-12}		$\sim 1 \times 10^{-16}$	$\sim 0.5 \times 10^{-5}$	2×10^{-14}	1.5×10^{-17}	–	4.82×10^{-17}	1.03×10^{-16}
I_{ON}/I_{OFF}	61.4×10^{6}		$\sim 5.5 \times 10^{8}$	~ 150	1×10^{5}	3.33×10^{11}	–	2.5×10^{10}	4.01×10^{12}
τ (ps)	0.79		–	–	–	–	0.05	0.321	0.021
f_t (GHz)	443		–	19	–	7	12	0.682	54
f_{max} [GHz]	383		–	–	–	–	316	37.34	327

4. Validation of radio-frequency model of extended source TFETs

The values of modeling capacitances and effective gate resistance as a function of the frequency for a square-shaped extended source TFET with 30 nm gate length at $V_{GS} = V_{DS} = 0.7$ V are presented in the Fig. 15. It is observed excellent agreement between parameters obtained from the modeling (solid line) and the device simulation (symbol). Due to the frequency independence of modeling parameters, model is highly reliable and accurate. Furthermore, for different gate voltage and frequency (at $V_{GS} = 0.3$ and 0.7 V with $V_{DS} = 0.7$ V up to 250 GHz) of a square-shaped extended source TFET device, all the extracted parameters used in the verifications have been summarized in Table 2. As can be seen from the values of approximations, the assumptions and equations for approximations in the previous section are valid.

In order to validate the accuracy of the proposed models for extended source TFET and parameter extraction, we executed verifications of the *Y*-parameters from modeling using SPICE simulation and device simulation. Figs. 16 and 17 compare the modeled *Y*-parameters of square-shaped extended source and conventional TFET for 30 nm gate length with the values obtained from SPICE simulation and device simulation as a function of frequency up to 250 GHz, which covers the cut-off and maximum oscillation frequencies. It is observed that *Y*-parameters obtained from the NQS model equivalent circuit (solid line) showed excellent agreement with the calculation results by the SPICE simulation (symbol) and device simulation (dash line). Without any optimization, the root-mean-square errors of the model were calculated to be within 3.3% and 4.6% up to 250 GHz for the SPICE simulation and device simulation, respectively. These verification results strongly support that the

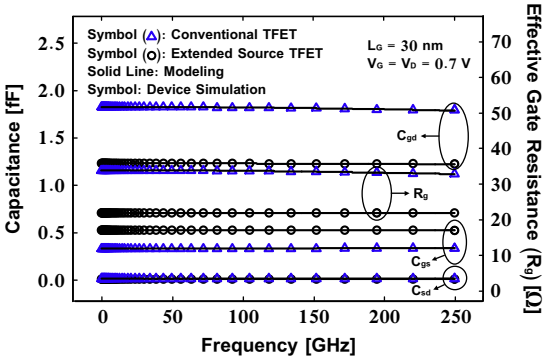

Fig. 15. Modeling (solid line) and the device simulation (symbol) of capacitances and effective gate resistance as a function of the frequency for a square-shaped extended source TFET with 30 nm gate length at $V_{GS} = V_{DS} = 0.7$ V.

Table 2
The summary of the extracted parameters and approximations values in different gate voltage ($V_{GS} = 0.3$ and 0.7 V with $V_{DS} = 0.7$ V) for 30 nm square-shaped extended source TFET.

Parameter	$V_G = 0.3$ $V_D = 0.7$ at 100 GHz	$V_G = 0.7$ $V_D = 0.7$ at 100 GHz	$V_G = 0.3$ $V_D = 0.7$ at 250 GHz	$V_G = 0.7$ $V_D = 0.7$ at 250 GHz
C_{gs}	0.588 fF	0.528 fF	0.588 fF	0.527 fF
C_{gd}	0.508 fF	1.233 fF	0.508 fF	1.234 fF
C_{sd}	5.915 aF	14.649 aF	5.965 aF	13.992 aF
R_g	12.04 Ω	20.932 Ω	12.043 Ω	20.929 Ω
τ	0.362 ps	0.321 ps	0.361 ps	0.321 ps
g_m	34.455 nS	6.817 μS	34.455 nS	6.817 μS
g_{ds}	0.184 nS	52.45 nS	0.184 nS	52.45 nS
$\omega^2 R_g^2 (C_{gs} + C_{gd})^2$	1.74×10^{-6}	13.59×10^{-6}	0.109×10^{-6}	0.839×10^{-6}
$\omega^2 \tau^2$	1.31×10^{-3}	1.03×10^{-3}	8.1×10^{-3}	6.4×10^{-3}

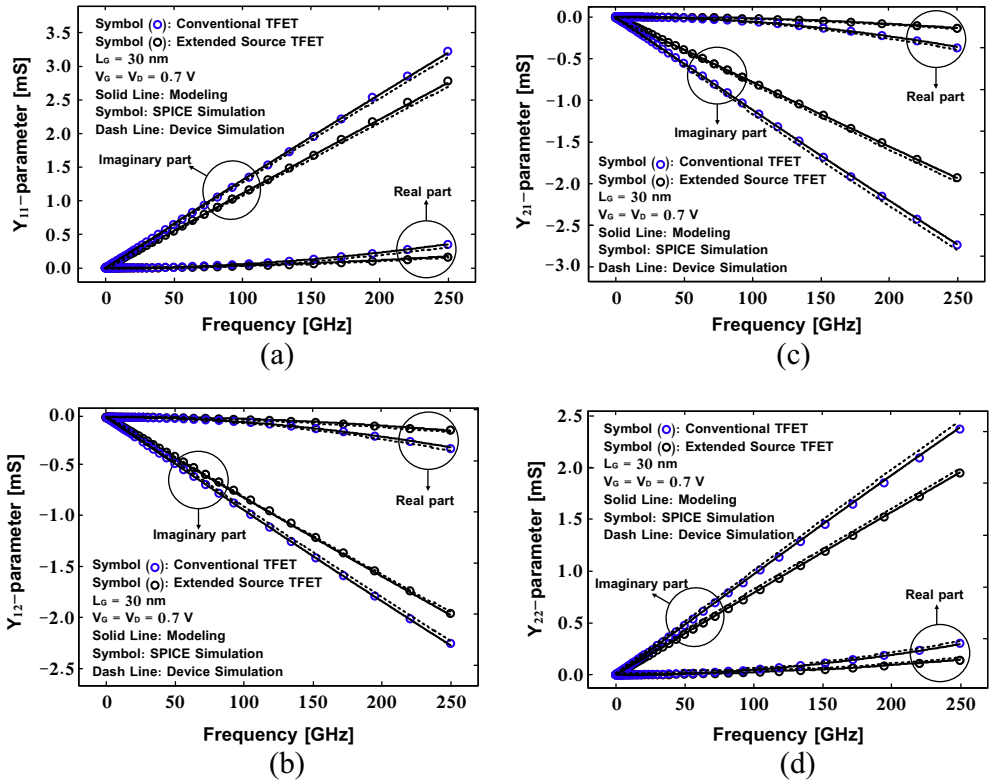

Fig. 16. Comparison of modeled (solid line) and values obtained from SPICE simulation (symbol) and device simulation (dash line) *Y*-parameters of square-shaped extended source and conventional TFET with 30 nm gate length as a function of frequency at $V_{GS} = V_{DS} = 0.7$ V. (a) Y_{11}, (b) Y_{12}, (c) Y_{21} and (d) Y_{22}.

proposed model is accurate and valid for extended source TFETs up to the extremely high frequency range. Extracted small-signal parameters from *Y*-parameters of device simulation have been used not for the cut-off and maximum oscillation frequencies extraction but for the evaluation of the RF performances. Consequently, we use the modeling parameters in the rest of paper except the cut-off and maximum oscillation frequencies extraction. The cut-off and maximum oscillation frequencies of TFETs have been obtained from the high-frequency current gain and unilateral power gain data of the device simulation, respectively.

5. Conclusion

The RF performance of DG square-shaped extended source TFETs have been compared with the conventional TFETs based on parameter extractions from the NQS model equivalent circuit in terms of the cut-off frequency, maximum oscillation frequency, current gain, unilateral power gain and small-signal parameters. Due to the higher transconductance and current drivability and smaller gate capacitance, the square-shaped extended source TFETs have higher RF performances and switching-speed than conventional TFETs. In addition, the RF figures of merit dependence of extended source TFET on the high-κ gate dielectric has been studied. The high-κ gate dielectric extended source TFET showed improved characteristics including higher cut-off and maximum oscillation frequencies and lower channel resistance and time constant. According to the modeling results, the RF equivalent circuit has high accuracy for square-shaped extended source TFETs.

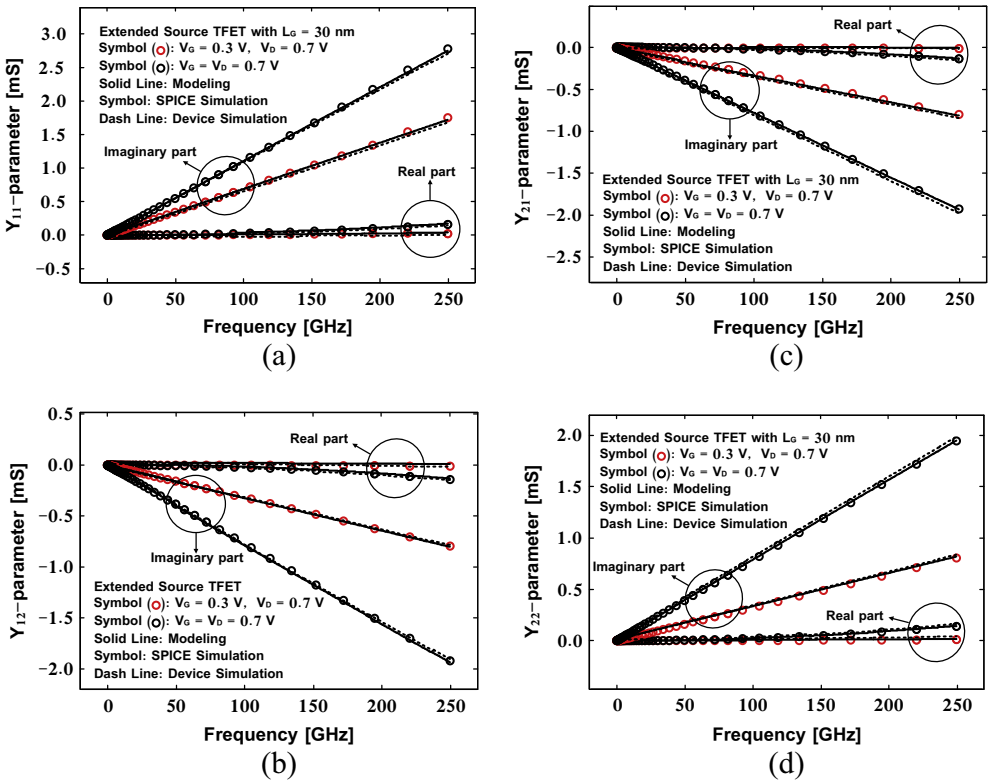

Fig. 17. Comparison of modeled (solid line) and values obtained from SPICE simulation (symbol) and device simulation (dash line) *Y*-parameters of square-shaped extended source TFET with 30 nm gate length at V_{GS} = 0.3 and 0.7 V with V_{DS} = 0.7 V. (a) Y_{11}, (b) Y_{12}, (c) Y_{21} and (d) Y_{22}.

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