A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter

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***Abstract*—This brief presents a power-efficient voltage level-shifter architecture that is capable of converting extremely low levels of input voltages to higher levels. In order to avoid the static power dissipation, the proposed structure uses a current generator that turns on only during the transition times, in which the logic level of the input signal is not corresponding to the output logic level. Moreover, the strength of the pull-up device is decreased when the pull-down device is pulling down the output node in order for the circuit to be functional even for the input voltage lower than the threshold voltage of a MOSFET. The operation of the proposed structure is also analytically investigated. Post-layout simulation results of the proposed structure in a 0.18-μm CMOS technology show that at the input low supply voltage of 0.4 V and the high supply voltage of 1.8 V, the level shifter has a propagation delay of 30 ns, a static power dissipation of 130 pW, and an energy per transition of 327 fJ for a 1-MHz input signal.**

***Index Terms*—Power efficiency, subthreshold operation, voltage-level converter.**

I. Introduction

In digital circuits, reducing the supply voltage is one of the most effective ways to reduce their dynamic and short-circuit power dissipation [1]–[3]. On the other side, in analog circuits, this smaller supply voltage not only increases the sensitivity of the analog blocks to the noise by decreasing their dynamic range but also makes the required switches more challenging to implement [1]. Hence, in moderate-speed mixed-signal circuits or in digital circuits where different blocks operate at different speeds, employing two or more different supply voltages is advantageous from the power dissipation viewpoint [1]. However, between the part of having a low supply voltage of $V_{\rm DDL}$ and the other part of having a high supply voltage of $V_{\rm DDH}$, a voltage level shifter is needed to convert the logic levels of $(V_{\rm SS}, V_{\rm DDL})$ to $(V_{\rm SS}, V_{\rm DDH})$ with minimum additional power dissipation and propagation delay. Therefore, several attempts have been reported to reduce the power dissipation and the delay of the level converters [2]–[7].

One of the conventional structures for a voltage level shifter is depicted in Fig. 1(a). In this circuit, when the input signal IN is switched from $V_{\rm SS}$ to $V_{\rm DDL}$, $\rm M_{N2}$ turns off and $\rm M_{N1}$ turns on trying to pull down node Q_1. Consequently, $\rm M_{P2}$ is gradually turned on to pull node Q_2 up to $V_{\rm DDH}$ and to turn $\rm M_{P3}$ off. It can be observed that there is a contention at the nodes Q_1 and Q_2 between the pull-down devices (i.e., $\rm M_{N1}$ and $\rm M_{N2}$) driven with the low supply voltage (i.e., $V_{\rm DDL}$) and the pull-up devices (i.e., $\rm M_{P1}$ and $\rm M_{P2}$) driven with the high supply voltage (i.e., $V_{\rm DDH}$). As a result, the conventional level shifter cannot correctly operate when the difference between the values of $V_{\rm DDH}$ and $V_{\rm DDL}$ becomes large. This problem is more critical when $V_{\rm DDL}$ is lower than the threshold voltage of input devices.

One approach to solving this problem is to increase the current of the pull-down transistors by enlarging their widths, leading to an increase in both the delay and the power dissipation [4]. Another solution, as shown in Fig. 1(b), is to reduce the strength of the pull-up devices by limiting their currents using a current mirror [2], [3], [5]–[7]. However, this current mirror leads to more static power dissipation [5]. In order to avoid the static power dissipation, a level shifter with logic-error correction (LSLEC), as shown in Fig. 1(c), uses a distinctive current generator that works only during the transition times, in which the logic level of the input signal is not corresponding to the output logic level [4]. However, as will be discussed in Section II, there is a contention between the pull-up (i.e., $\rm M_{P3}$) and the pull-down (i.e., $\rm M_{N3}$) devices of this structure when the input signal changes from $V_{\rm DDL}$ to $V_{\rm SS}$, leading to an increase in the transition time and the power dissipation. Hence, based on reducing this contention, in this brief, a small-delay and low-power level shifter that is also able to convert subthreshold input voltages is presented.

The rest of this brief is organized as follows. Section II presents the proposed level shifter. In Section III, the operation of the proposed circuit is analytically investigated. Section IV presents post-layout simulation results of our design verifying the efficiency of the proposed circuit. Finally, this brief is concluded in Section V.

II. Proposed Voltage Level Shifter

The schematic of the proposed level shifter is shown in Fig. 2(a). In this circuit, in order to reduce the strength of the pull-up devices, two current generators (i.e., $\rm M_{P3}$, $\rm M_{P4}$, $\rm M_{P5}$, $\rm M_{P6}$, $\rm M_{N3}$, $\rm M_{N4}$, $\rm M_{N5}$, and $\rm M_{N6}$) limit the currents applied to the pull-up transistors (i.e., $\rm M_{P1}$ and $\rm M_{P2}$). Consequently, by decreasing the strength of the pull-up devices, the pull-down transistors (i.e., $\rm M_{N1}$ and $\rm M_{N2}$) would be able to overcome the mentioned contention at the nodes Q_1 and Q_2 and therefore discharge the output nodes to $V_{\rm SS}$ even for the input voltages lower than the threshold voltage. In order to avoid the static power dissipation, the current generators are turned on only during the transition times, in which the logic level of the input signal is not corresponding to the output logic level. The operation of the proposed structure is as follows.

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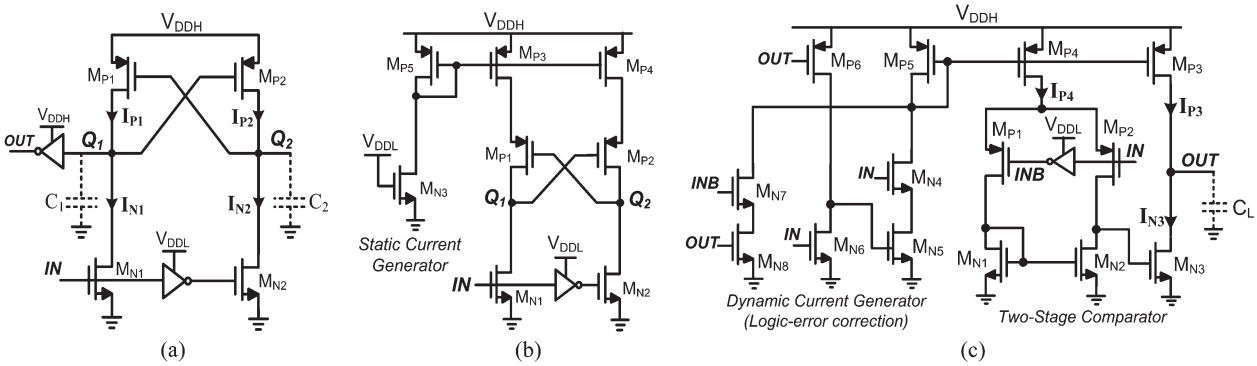

Fig. 1. Schematic of the (a) conventional level shifter, (b) half-latch-based level shifter [5], and (c) LSLEC [4].

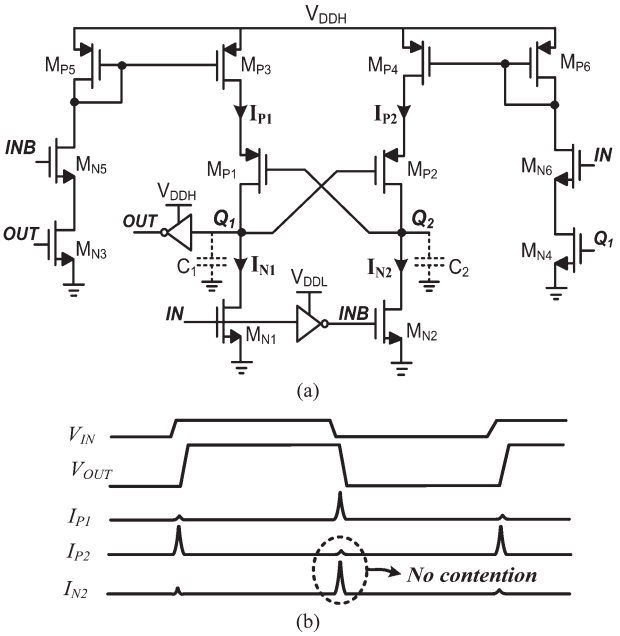

Fig. 2. (a) Schematic of the proposed level shifter. (b) Waveforms of the input voltage, the output voltage, and the currents of $\mathrm{M_{P1}}$, $\mathrm{M_{P2}}$, and $\mathrm{M_{N2}}$.

When the input signal IN is going from V_{SS} to V_{DDL}, $\mathrm{M_{N1}}$ is turned on and $\mathrm{M_{N2}}$ is turned off. Therefore, similar to the conventional counterpart, $\mathrm{M_{N1}}$ tries to pull down the node Q_1, and consequently, $\mathrm{M_{P2}}$ is gradually turned on to pull the node Q_2 up to V_{DDH}. As shown in Fig. 2(b), when IN changes from V_{SS} to V_{DDL}, there is an interval during which Q_1 does not correspond to the logic level of IN. During this period, both $\mathrm{M_{N4}}$ and $\mathrm{M_{N6}}$ turn on, and therefore, a transition current flows through $\mathrm{M_{N4}}$, $\mathrm{M_{N6}}$, and $\mathrm{M_{P6}}$. This current, which is mirrored to $\mathrm{M_{P4}}$, flows into $\mathrm{M_{P2}}$ and then charges the node Q_2. At the same time, on the other side of the circuit, $\mathrm{M_{N5}}$ turns off because INB $= V_{\mathrm{SS}}$, and therefore, there is no current flowing through $\mathrm{M_{P1}}$ (i.e., $I_{P1} \approx 0$), meaning a weak pull-up device. This causes that $\mathrm{M_{N1}}$ be able to pull down the node Q_1 even for the input voltage lower than the threshold voltage of $\mathrm{M_{N1}}$. Finally, when the node Q_1 is pulled down to V_{SS} and Q_2 is pulled up to V_{DDH}, $\mathrm{M_{N4}}$ is turned off, and therefore, no static current flows through $\mathrm{M_{N4}}$, $\mathrm{M_{N6}}$, and $\mathrm{M_{P6}}$. This means that the current-generator structures are turned on only during the transition times, in which the input and the output signals do not correspond, avoiding the static power dissipation. Similarly, when the input signal IN is switched from V_{DDL} to V_{SS}, the operation is forced to reverse states.

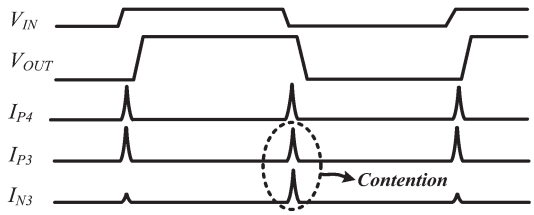

Fig. 3. Waveforms of the input voltage, the output voltage, and the currents of $\mathrm{M_{P3}}$, $\mathrm{M_{P4}}$, and $\mathrm{M_{N3}}$ in the LSLEC structure shown in Fig. 1(c).

In order to have a better compression between the proposed structure and the LSLEC structure shown in Fig. 1(c), we need to explain the existing contention in the output branch of the LSLEC structure. Consider the situation in which the input signal is changed from V_{DDL} to V_{SS}. During the transition time in which the logic level of the output is not corresponding to the logic level of IN, the transition current generated by the dynamic current generator (i.e., $\mathrm{M_{N7}}$ and $\mathrm{M_{N8}}$) is applied into both the first and the second stage of two-stage comparator through $\mathrm{M_{P4}}$ and $\mathrm{M_{P3}}$, respectively, as shown in Fig. 3. As for the first stage, the applied current to $\mathrm{M_{P4}}$ flows through $\mathrm{M_{P2}}$ to pull up the gate of $\mathrm{M_{N3}}$. Therefore, $\mathrm{M_{N3}}$ is turned on trying to pull the node OUT down. At the same time, in the second stage, the transition current applied to $\mathrm{M_{P3}}$ tries to pull the node OUT up. Therefore, there is a contention between the pull-up device (i.e., $\mathrm{M_{P3}}$) and the pull-down device (i.e., $\mathrm{M_{N3}}$), leading to large transition time and, therefore, more power dissipation. It should be noted that this contention results in more power dissipation not only at the branch of $\mathrm{M_{P3}}$ and $\mathrm{M_{N3}}$ but also at the other branches of the circuit due to the fact that the transition times will be increased, and therefore, the current generator will be turned on for a longer time. In addition, the power dissipation increases as the value of V_{DDL} is increased. This is due to the fact that high values of V_{DDL} increase the current of $\mathrm{M_{N7}}$ and, therefore, the current of $\mathrm{M_{P3}}$.

On the other hand, in the proposed circuit, at the transition times, the dynamic current generator applies the transition current into either $\mathrm{M_{P3}}$ or $\mathrm{M_{P4}}$ [the one supposed to pull up the related output node (i.e., Q_1 or Q_2)], as shown in Fig. 2(b). It should be noted that no current is applied to the other branch the output node of which is being pulled down by the pull-down device. Therefore, it can be concluded that in contrast to the LSLEC structure, there is no contention between the pull-up and the pull-down devices of the proposed structure. Thus, the proposed level shifter not only is capable to convert extremely low levels of the input voltages, but also, its transition times and power dissipation considerably decrease due to the fact that the

strength of the pull-up device is decreased when the pull-down device is pulling down the output node.

III. Comparison of the Level Shifters

In order to compare the operation of the conventional, the LSLEC structure, and the proposed level shifters, in this section, the output voltage (i.e., $V_{Q1}(t)$ related to the output node Q_1) of these three structures will be calculated as a function of time. It should be noted that while the $i_D - V_{GS}$ curve of any MOS transistors is nearly quadratic at moderate values of V_{GS}, the characteristic becomes nearly linear for higher values in modern short-channel devices. Applying the simplified piecewise-linear model, the current through each transistor can be expressed as [8]

$$I_D = \begin{cases} G_m(V_{GS} - V_t), & V_{GS} > V_t \\ 0, & \text{others} \end{cases} \quad (1)$$

where G_m represents the slope of a linear curve fit to the "on" region of the transistor, and V_t is given by the intercept of this segment with the axis. Note that V_t is slightly larger than the actual threshold voltage of the device [8].

Now, in order to calculate the output voltage (i.e., $V_{Q1}(t)$) in the conventional level shifter shown in Fig. 1(a), applying Kirchhof's current law (KCL) for the nodes Q_1 and Q_2 gives

$$I_{N1} + C_1\frac{dV_{Q1}}{dt} = I_{P1} \quad I_{N2} + C_2\frac{dV_{Q2}}{dt} = I_{P2} \quad (2)$$

where I_{N1}, I_{N2}, I_{P1}, and I_{P2} are the current of $\mathrm{M_{N1}}$, $\mathrm{M_{N2}}$, $\mathrm{M_{P1}}$, and $\mathrm{M_{P2}}$, respectively. C_1 and C_2 are the total capacitances of the nodes Q_1 and Q_2, respectively.

Now, in order to investigate the transition (e.g., falling-transition) behavior of the conventional level shifter, it should be noted that $\mathrm{M_{N1}}$ and $\mathrm{M_{N2}}$ are on and off, respectively, due to the fact that $V_{GS,N1} = V_{\mathrm{DDL}}$ and $V_{GS,N2} = 0$. Moreover, the voltage of the output nodes related to the previous states are $V_{Q1} = V_{\mathrm{DDH}}$ and $V_{Q2} = 0$. Applying (1), (2) can be rewritten as

$$\begin{aligned} I_{N1} + C_1\frac{dV_{Q1}}{dt} &= G_{mP1}\left(V_{\mathrm{DDH}} - V_{Q2} - |V_{tP1}|\right) \\ 0 + C_2\frac{dV_{Q2}}{dt} &= G_{mP2}\left(V_{\mathrm{DDH}} - V_{Q1} - |V_{tP2}|\right). \end{aligned} \quad (3)$$

By simplifying the aforementioned expressions, the differential equation related to V_{Q1} will be obtained as

$$\frac{d^2V_{Q1}}{dt^2} - \frac{G_{mP1}G_{mP2}}{C_1C_2}V_{Q1} + \frac{G_{mP1}G_{mP2}\left(V_{\mathrm{DDH}} - |V_{tP2}|\right)}{C_1C_2} = 0. \quad (4)$$

Two initial conditions required for solving (4) are the initial value of V_{Q1} and its first derivative. The initial value of the first derivative can be calculated from (3). Thus

$$V_{Q1}(0) = V_{\mathrm{DDH}} \quad \frac{dV_{Q1}}{dt}(0) = \frac{G_{mP1}(V_{\mathrm{DDH}} - V_{tP1}) - I_{N1}}{C_1}. \quad (5)$$

Using (4) and (5), $V_{Q1}(t)$ can be obtained from

$$\begin{aligned} V_{Q1}(t) = &\left(m + \frac{|V_{tP2}|}{2}\right)e^{\alpha t} \\ &+ \left(-m + \frac{|V_{tP2}|}{2}\right)e^{-\alpha t} + V_{\mathrm{DDH}} - |V_{tP2}| \end{aligned} \quad (6)$$

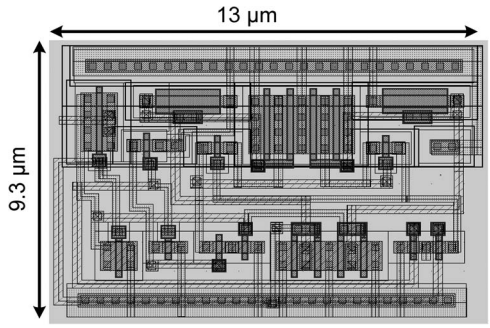

Fig. 4. Layout of the proposed level shifter.

where

$$\alpha = \sqrt{\frac{G_{mP1}G_{mP2}}{C_1C_2}} \quad m = \frac{G_{mP1}(V_{\mathrm{DDH}} - V_{tP1}) - I_{N1}}{2C_1\sqrt{G_{mP1}G_{mP2}/C_1C_2}}. \quad (7)$$

In (6), since the exponential terms with negative exponents eventually vanish, only the terms with the positive exponents are important in determining the final state of the outputs, confirming that the transition of the output will entail to the supply rails (i.e., V_{DDH} or $V_{\mathrm{SS}} = 0$). Due to the fact that, in this case (i.e., $V_{Q1}(\infty) = 0$), the coefficient of the positive exponential term must be negative, we have

$$m + 0.5|V_{tP2}| < 0. \quad (8)$$

Assuming $G_{mP1} = G_{mP2}$, $V_{tP1} = V_{tP2}$, and $C_2 = C_1$, (8) results in

$$I_{N1} = G_{mN1}(V_{\mathrm{DDL}} - V_{tN1}) > G_{mP1}V_{\mathrm{DDH}}. \quad (9)$$

According to the preceding equation, it is clear that the conventional structure has a critical problem when the voltage difference between the low supply voltage and the high supply voltage becomes large. In other words, the pull-down device (i.e., $\mathrm{M_{N1}}$) will not be able to pull the node Q_1 down to V_{SS} if its driven current is smaller than that of the pull-up device (i.e., $\mathrm{M_{P1}}$). In order to overcome this problem, as mentioned in Section I, as the difference between V_{DDH} and V_{DDL} becomes larger, the size of $\mathrm{M_{N1}}$ must be also larger; however, large size increases both the delay and the power consumption. The other solution, as used in the proposed structure, is to decrease the strength of the pull-up transistor (i.e., $\mathrm{M_{P1}}$) such that $\mathrm{M_{N1}}$ becomes able to pull the node Q_1 down to V_{SS}.

Similarly, in order to investigate the LSLEC structure, the similar procedure can be applied. For the falling transition of the output node (i.e., OUT), since the logic level of OUT is not corresponding to the logic level of IN, the dynamic current generator is on. Assuming I_{P3} is constant during the transition, the KCL equation at the output node can be written as

$$I_{N3} + C_L\frac{dV_{\mathrm{OUT}}}{dt} = I_{P3} \quad V_{\mathrm{OUT}}(0) = V_{\mathrm{DDH}}. \quad (10)$$

Solving (10) results in

$$V_{\mathrm{OUT}}(t) = \left(\frac{I_{P3} - I_{N3}}{C_L}\right)t + V_{\mathrm{DDH}}. \quad (11)$$

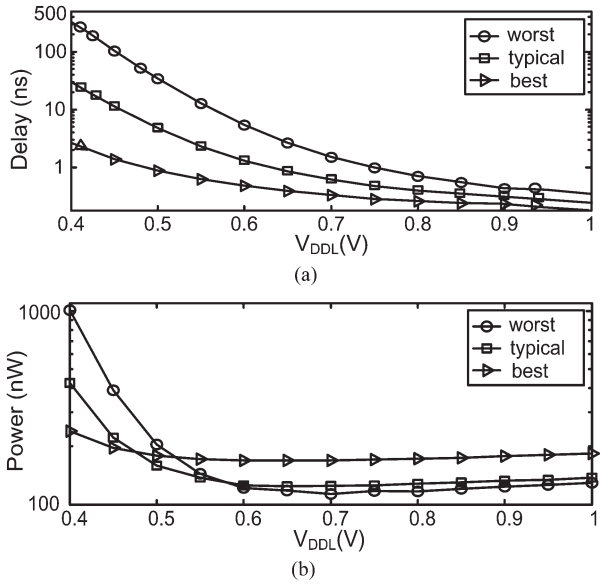

Fig. 5. Simulated values of the (a) propagation delay and (b) total power consumption of the proposed level shifter for different values of V_{DDL}. The value of the input signal frequency is 1 MHz.

It can be observed that in order to have a final state of V_{SS} for the voltage of the output node (i.e., $V_{\mathrm{OUT}}(\infty) = 0$), the coefficient of the linear term must be negative, i.e.,

$$I_{N3} > I_{P3}. \tag{12}$$

According the preceding equation, it is clear that in order for the circuit to operate correctly, it needs to meet the constraint defined by (12) to overcome the existing contention between the pull-up and the pull-down devices when the pull-down device is pulling down the output node (see Fig. 3).

Finally, in order to study the operation of the proposed structure, consider the falling transition of the output node Q_1. Assuming the current generators turn on and off completely (i.e., $I_{P1} = 0$ and I_{P2} will be constant during the transition), the KCL equations are expressed as

$$\begin{cases} I_{N1} + C_1 \frac{dV_{Q1}}{dt} = 0, & V_{Q1}(0) = V_{\mathrm{DDH}} \\ 0 + C_2 \frac{dV_{Q2}}{dt} = I_{P2}, & V_{Q2}(0) = 0. \end{cases} \tag{13}$$

Solving (13) results in

$$V_{Q1}(t) = \left(\frac{-I_{N1}}{C_1}\right) t + V_{\mathrm{DDH}}, \quad V_{Q2}(t) = \left(\frac{I_{P2}}{C_1}\right) t. \tag{14}$$

According to (14), it can be observed that in contrast to the conventional and the LSLEC structures, the proposed architecture does not need to meet the constraints defined by neither (9) nor (12), meaning that it will be able to operate correctly when the voltage difference between V_{DDL} and V_{DDH} becomes large even for the input voltages lower than the threshold voltage of an nMOS device.

IV. Simulation Results

In order to verify the efficiency of the proposed level shifter, the proposed structure and also the structures presented in [2]–[4], [6], and [7] have been simulated at the transistor level in a 0.18-μm 1P6M CMOS technology. All circuits have been optimally designed to be functional in all process, voltage, and temperature (PVT) corners for $V_{\mathrm{DDH}} = 1.8$ V, $V_{\mathrm{DDL}} = 0.4$ V, and the input frequency of 1 MHz. In order to have a fair comparison between the structures, an inverter is added as a load circuit to all the structures, and the calculated power dissipation includes the power consumption of the load.

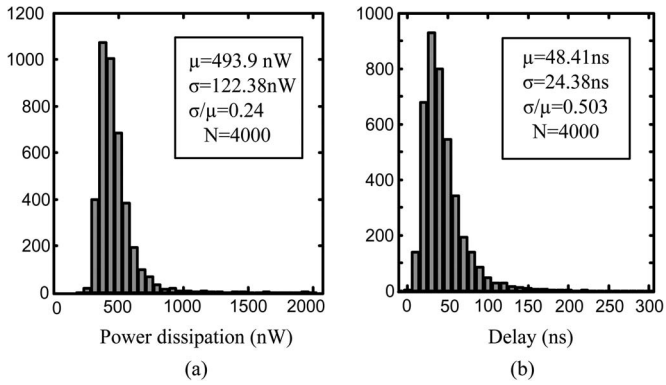

Fig. 6. Distribution of the (a) total power dissipation and (b) propagation delay of the proposed level shifter.

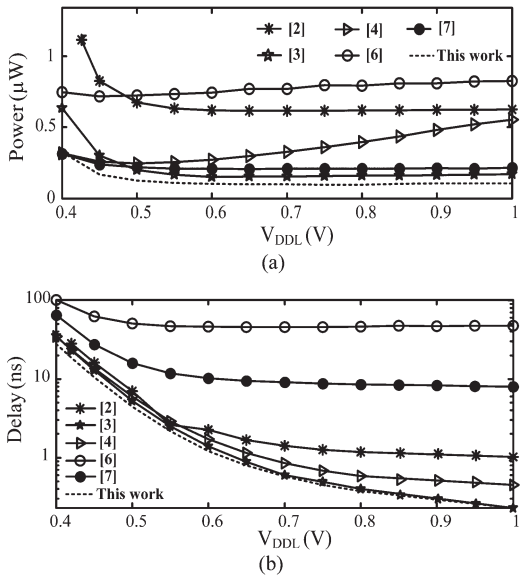

Fig. 7. Simulated (a) total power dissipations and (b) delays of the level-shifter circuits as a function of V_{DDL} at $V_{DDH} = 1.8$ V. The employed value of the input frequency is 1 MHz.

The layout of the proposed level shifter is illustrated in Fig. 4. The active area occupied by the circuit is 120.9 μm^2. The following simulation results are related to the post-layout analysis. Moreover, in the proposed structure, the typical corner includes a typical nMOS and a typical pMOS transistor, a high supply voltage of $V_{\mathrm{DDH}} = 1.8$ V, and a temperature of 25 °C. As discussed in the previous sections, due to the fact that there is no contention between the pull-up and the pull-down devices, fast nMOS and fast pMOS result in the minimum delay. Moreover, an increased voltage on V_{DDL} and a decreased voltage on V_{DDH} further improve this situation. Finally, high temperature results in a larger device current. Thus, fast nMOS, fast pMOS, $+10\%$ V_{DDL}, -10% V_{DDH}, and a temperature of 120 °C were chosen as the best corner. Contrarily, slow nMOS,

TABLE I
COMPARATIVE SIMULATION RESULTS ($V_{DDH} = 1.8$ V)

	f_{IN}=1MHz	V_{DDL}=0.45V, f_{IN}=1MHz		
	$V_{DDL,minimum}$ (V)	Delay (ns)	Total Power (nW)	PDP * (nW.ns)
[2]	0.42	16.5	800	13200
[3]	0.37	13	300	3900
[4]	0.37	14	257	3598
[6]	0.39	62	717	44452
[7]	0.4	28	238	6664
This work	0.36	12	175	2100

* PDP: Power-Delay Product

slow pMOS, -10% $V_{\rm DDL}$, $+10\%$ $V_{\rm DDH}$, and a temperature of 0 °C were chosen as conditions of the worst corner. Fig. 5 shows the simulation results of the propagation delay and the total (i.e., static and dynamic) power consumption of the proposed circuit versus the value of $V_{\rm DDL}$, for typical, best, and worst corners. Although at $V_{\rm DDL} = 0.4$ V the worst-case delay and power dissipation are 123.4 and 4.2 times higher than the best case, the circuit still operates correctly at all PVT corners for the 1-MHz input frequency.

To investigate the operation of the proposed level shifter against the mismatch of the devices, a 4000-point Monte Carlo simulation has been performed for a high supply voltage of $V_{\rm DDH} = 1.8$ V and a low supply voltage of $V_{\rm DDL} = 0.4$ V with both local and global variations. The results are shown as histograms of the delay and the power dissipation in Fig. 6. The normalized standard deviation values (σ/μ) of the delay and the power consumption are 0.503 and 0.24, respectively.

As for the range of the operating frequency of the proposed structure, the simulation results show that the minimum values of $V_{\rm DDL}$ for which the circuit operates correctly at 100 Hz and 100 MHz are 0.1 and 0.63 V, respectively.

Finally, in order to compare the proposed circuit with the other works, Fig. 7 shows the simulated values of the power dissipation and the propagation delay of the proposed structure and the circuits presented in [2]–[4], [6], and [7] for different values of $V_{\rm DDL}$. All structures were simulated at the typical PVT corner with $V_{\rm DDH} = 1.8$ V. Moreover, Table I summarizes the performance of the structures. It can be observed that the proposed structure presents superior performance compared with the other structures from both the delay and the power dissipation viewpoints. This is due to the fact that, in the proposed structure, as discussed in Section II, the strength of the pull-up device is decreased when the pull-down device is pulling down the output node.

V. CONCLUSION

In this brief, a low-power voltage level shifter was proposed to be able to convert extremely low input voltages. This is due to the fact that the strength of the pull-up device is decreased when the pull-down device is pulling down the output node. Moreover, the proposed structure does not introduce a static current path between the supply rails. Post-layout simulation results using a 0.18-μm CMOS technology confirmed the efficiency of the proposed level shifter.

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