A Novel Double Gate Tunnel Field Effect Transistor with 9 mV/dec Average Subthreshold Slope

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Abstract- **In this paper, a novel double gate tunnel field effect transistor (DGTFET) configuration with p^+-layer in the channel is proposed and investigated. The proposed structure is a Si-channel DGTFET, which has a p^+-layer in the channel connected to the P^+ source region in order to achieve improved switching and higher ON-current when compared to a conventional TFET. The simulation results of DGTFET with p^+-layer in the channel shows excellent characteristics with high I_{ON}/I_{OFF} ratio (about 5×10^{12}) and an average subthreshold slope of about 9 mV/decade over 4 decades of current at room temperature. Results suggest that, the DGTFET with p^+-layer in the channel seem to be the most optimal ones to replace MOSFET for ultralow power applications and switching devices.**

Keywords- Band-to-band tunneling (BTBT); ON-current; Average subthreshold slope (SS_{AVG}); DGTFET;

I. INTRODUCTION

In the recent decade, due to unique characteristics such as steep substhreshold slope (SS) and a very low leakage current, Band-to-band tunneling (BTBT) Tunnel Field Effect Transistors (TFETs) have attracted considerable attention as one of the promising candidates to replace MOSFET for ultralow power applications [1-4]. Recently, researchers have reported devices with SS below 60 mV/decade at room temperature, both theoretically and experimentally [5-9]. A silicon-based TFET exhibits a minimized subthreshold swing with a low OFF-current. Due to low ON-current of silicon-based TFETs, different techniques have been suggested to improve the ON-current [10-13]. Furthermore, TFETs often exhibit strong DIBL effect and this can severely limit the utility of the TFETs [14]. As a result, the ON-current, the subthreshold swing and output characteristics must be improved to employ TFET for ultralow power CMOS applications and switching devices.

Due to dependence of the tunneling current on the transmission probability of the interband tunnelling barrier, we consider the Wentzel–Kramer–Brillouin (WKB) approximation to estimate the transmission probability [15, 16]:

$$I_{on} \propto T_{WKB} \approx \exp(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\,3}}}{3q\hbar(E_g+\Delta\phi)}) \qquad (1)$$

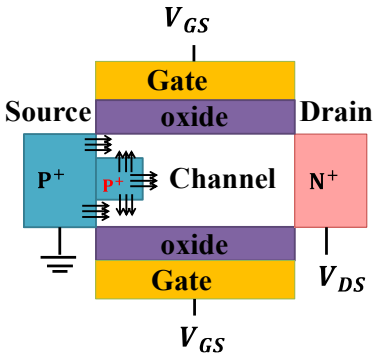

Fig. 1. Schematical representation of the DGTFET with the p^+-layer. The channel and p^+ layer lengths equal to 100 and 30 nm, respectively. Gate metal work functions = 3.8 eV.

where λ is the screening tunnelling length, m^* is the effective mass, E_g is the bandgap, q is the elementary charge, Δ□ denotes the energy overlap of valence and conduction bands and ħ is the reduced Planck's constant.

The subthreshold slope expression can be approximated to [16]:

$$SS \approx \frac{\ln(10)}{|q|}\Delta\phi \qquad (2)$$

According to (2), subthreshold slope has a direct relationship with the Δ□. Thus, a device can have a SS close to zero for very small Δ□.

In this paper, we propose a novel Si-based double gate tunnel field effect transistor (DGTFET) with a p^+-layer in the channel to achieve larger tunneling area. Compared with conventional DGTFET, by merely introducing a p^+-layer in the channel, it is possible to simultaneously achieve a minimized subthreshold swing with a high ON-current and low OFF-current and the immunity against DIBL effects. The rest of this paper is organized as follows: Section II describes the device structures and physical models and simulation parameters. Section III presents the device characteristics of the ON-/OFF-current and subthreshold swing in TFET devices. Final conclusions are presented in Section IV.

II. DEVICE STRUCTURE AND SIMULATION MODEL

The structure of a proposed Si-based double gate tunnel

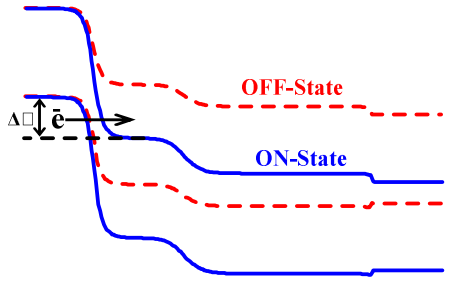

Fig. 2. Energy band diagram of DGTFET with the p^+-layer in the OFF- and On-state. OFF-state ($V_{DS} = V_G = 0$ V) and ON-state ($V_{DS} = V_G = 0.75$ V).

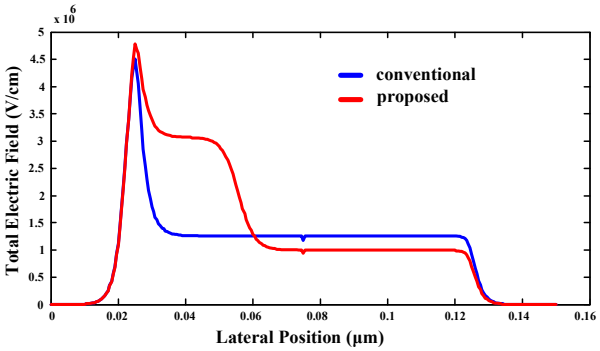

Fig. 3. Surface electric field E of proposed structure (DGTFET with the p^+-layer in the channel) and conventional DGTFET along the tunnel directions when devices turn on ($V_{DS} = 0.5$ V and $V_G = 1$ V).

field effect transistor is schematically shown in Fig. 1. Compared with conventional DGTFET, it has a p^+-layer in the channel connected to the P^+ source region with the larger tunneling area. The simulated DGTFET is a Si-channel doping concentrations $N_D = 1\times10^{15}$ cm^{-3} with a 100 nm channel length, source and drain doping concentrations N_A=N_D = 1×10^{20} cm^{-3} with extension length of 25 nm, silicon body thickness of 15 nm, 2 nm gate oxide thickness, 30 nm p^+ layer length, 5 nm p^+ layer thickness and gate metal work functions of 3.8 eV. The tool used to perform the simulations is Silvaco Atlas, of version 5.18.3.R [17]. Band-to-band tunneling has been modeled using a dynamic nonlocal path tunneling approach for the device performance calculations. Due to high doping concentration and high impurity atom in the channel, Band-gap narrowing and Shockley-Read-Hall recombination models are also enabled. Also mobility, Auger recombination and trap-assisted-tunneling models are also activated [17-20].

III. RESULTS

Fig. 2 shows the OFF- and ON-state energy band diagrams of DGTFET with the p^+-layer along the channel surface. In the OFF-state, the source valence band is located below the channel conduction band. Due to the large tunneling barrier in between the source and channel, the probability of the tunneling of electrons is negligible. So, the small TFET off-state current flows only because of the reverse-biased p-i-n diode leakage. Under the ON-state condition, applying a positive gate voltage pulls the energy bands down and the channel conduction band goes below the source valence band and the band pass window is created. Thus, a sufficiently high lateral electric field is created at the source-channel junction, which forces the electrons to tunnel from the occupied valence

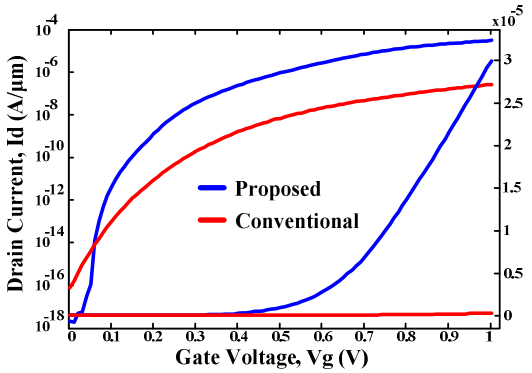

Fig. 4. Simulated transfer characteristics of proposed structure (DGTFET with the p^+-layer in the channel) and conventional DGTFET in linear and logarithm scales at $V_{DS} = 0.5$V.

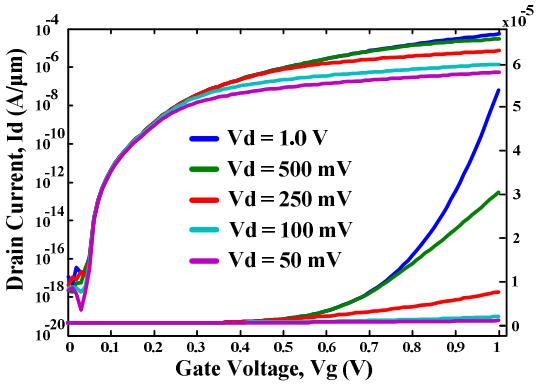

Fig. 5. Simulated transfer characteristics of the DGTFET with the p^+-layer as a function of V_D in linear and logarithm scales at room temperature. The average subthreshold slope assumes values as low as 9 mV/dec over 4 decades of drain current, from 1.4×10^{-16} to 1.4×10^{-12} μA/μm.

band states of the source to the unoccupied conduction-band states of the channel through the narrow tunneling barrier between the source and the channel. According to Eq. (1), with further increase in the gate voltage, Δ□ is increased and consequently more electrons can tunnel through the barrier and the current increases.

Fig. 3 compares the surface total electric field of DGTFET with the p^+-layer and conventional DGTFET when devices turn on. It can be seen that the proposed structure shows the higher total electric field between the source and channel because of the larger tunneling area and lower total electric field in between the drain and channel.

A comparative study between the DGTFET with the p^+-layer and conventional DGTFET at $V_{DS} = 0.5$V, is shown in Fig. 4. Parameters of the device are the same, except for p^+ layer length, which is zero for the conventional structure. As can be seen, DGTFET with the p^+-layer exhibits higher ON-current by more than a factor 2 and lower OFF-current by more than a factor 1.5. It should be mainly due to the higher total field in between the source and channel and the lower total electric field in between the drain and channel, simultaneously. So, the more electrons in the valence band of the source can tunnel through the barrier and reach the conduction band of the channel and also fewer holes in the conduction band of the drain can tunnel to the valence band of the channel, which results higher ON-current than conventional TFET as well as

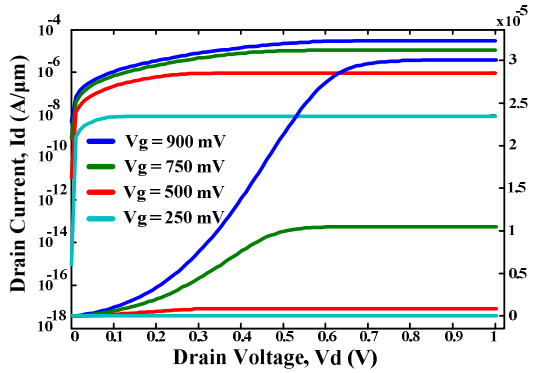

Fig. 6. Simulated output characteristics of DGTFET with the p^+-layer as a function of V_G in linear and logarithm scales at room temperature.

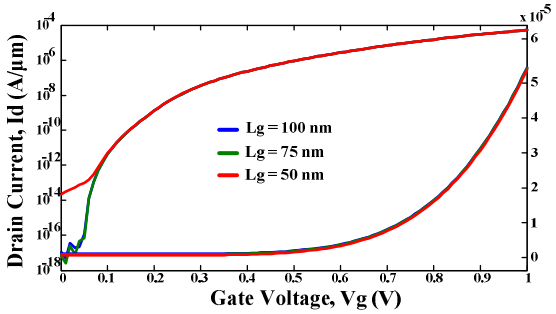

Fig. 7. Simulated Current–voltage curves of DGTFET with the p^+-layer devices with various channel lengths in linear and logarithm scales. Since the tunneling surface increases for longer channel length, ON–OFF switching is improved.

lower OFF-current. Moreover, barrier resulting from p^+-layer between the source and channel leads to a decrease in OFF-current.

The average subthreshold slope (SS_{AVG}) is high importance for switching devices and is given by [21]:

$$SS_{AVG} = \frac{(V_T - V_{OFF})}{\log(I_{V_T}) - \log(I_{V_{OFF}})} \qquad (3)$$

here V_T is the threshold voltage, V_{OFF} is the gate voltage that the drain current starts to take off; I_{VT} and I_{VOFF} are the drain current at VT and V_{OFF} respectively. As is obvious from Fig. 4, the DGTFET with the p^+-layer exhibits much steeper average SS over 4 decades of current from 35 to 9 mV/dec.

The transfer characteristics of the DGTFET with the p^+-layer as a function of V_D at room temperature are plotted Fig. 5. At $V_G = V_D = 1.0$ V, ON-current is on the order of 53.21 µA/µm. Intrinsic nature of electron tunneling limits the ON-current. OFF-current is on the order of 0.01 fA/µm. The Shockley-Read-Hall recombination is the dominant in the OFF-state. It is observed that the average subthreshold slope of 9 mV/dec over 4 decades of drain current, from about 1.4×10^{-16} to about 1.4×10^{-12} µA/µm due to an abrupt onset of the Band-to-band tunneling inside the channel. Due to the sharp variation between the OFF-state and the ON-state, the threshold voltage can be rather regarded as a transition voltage. The drain voltage variations from 50 mV to 1 V cause an increase about 2 and 3 decades in OFF- and ON-current.

Fig. 6 shows the output characteristics of DGTFET with the p^+-layer as a function of V_G at room temperature. Band-to-band tunneling devices have an exponential trend in curves linear scale at the low voltage drain [14]. As seen, the gate voltage variations have a strong impact on the output characteristics, increasing saturation current of about 5 decades passing from $V_G = 250$ mV to $V_G = 900$ mV.

Due to the strong short-channel effect, the development of TFETs was not so successful into sub-nm regimes [22]. The current-voltage curves of the DGTFET with the p^+-layer with various channel lengths are shown in Fig. 7. Due to increase in tunneling surface, longer channel length enhances the device characteristics. As seen, the 100-nm TFET retains the excellent characteristics of ON–OFF switching and OFF-current, simultaneously.

IV. CONCLUSION

In this work, we proposed and discussed a novel double gate tunnel field effect transistor (DGTFET) configuration with p^+-layer in the channel. Based on our 2D numerical simulations, the proposed device structure exhibits excellent ON–OFF characteristics. We showed a comparison with a conventional TFET. DGTFET with the p^+-layer exhibits higher ON-current by more than a factor 2 and lower OFF-current by more than a factor 1.5 in comparison with conventional TFET. The simulation results show high I_{ON}/I_{OFF} ratio (about 5×10^{12}) and an average subthreshold slope of about 9 mV/decade over 4 decades of current at room temperature.

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