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Design and comparison of nine-level single-phase inverters with a pair of coupled inductors and two dc sources

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Abstract: Four different nine-level single-phase inverters with coupled inductors are proposed in this study, for the first time. All proposed topologies are based on the well-known multilevel converters with two separate dc voltage sources in their structure, with some modifications to include a cell with the coupled inductors and a pair of half-bridge legs. Fewer number of semiconductor devices and dc sources and no need for split capacitors make the proposed inverters very attractive to both researchers and industry. The proposed inverters are compared with other conventional nine-level topologies from different points of view. Experimental results for these inverters on a low-voltage test bench are provided to demonstrate the validity of the analytical analysis.

1 Introduction

Nowadays, multilevel pulse-width modulated (PWM) voltage-source inverters (VSIs) are widely employed in many medium-voltage high-power applications such as large motor drives [1, 2], renewable energy systems [3, 4], flexible ac transmission systems [5, 6] etc. Increasing the number of output voltage levels permits the VSI to operate with a lower switching frequency, which directly results in lower losses and at the same time improved harmonic and electro-magnetic interference performance [7, 8]. Also, the need for lower-voltage rating semiconductor devices and reduced size and cost of the reactive elements such as filters may be pointed out as other main advantages of multilevel VSIs.

The most common multilevel inverter topologies are the cascaded H-bridge, diode-clamped (neutral-clamped) and flying capacitor (capacitor-clamped) structures [2, 8–10]. In recent years, other alternative approaches to the conventional topologies are also proposed in the literatures [11–17]. Yet, innovative multilevel VSIs without the need for a large number of dc sources and/or split capacitors in their structure are very attractive to both researchers and industry. Recently, a novel family of multilevel VSIs with the balanced coupled inductors are proposed [18–25]. This new family of multilevel converters offer various advantages over the conventional solutions such as [22, 24]:

- fewer number of semiconductor devices, which reduces the size, cost and losses of the converter;
- reduced number of separate dc voltage sources compared with cascaded structures;
- no need for bulky capacitors required in neutral-clamped and capacitor-clamped topologies, which eliminates the problem of dc capacitor voltage balancing with these topologies, also reduces losses;
- higher effective switching frequency, which reduces the size of the ac filters (large filters suffer from higher cost, more losses and large voltage drops) and speeds up the transient response; and
- some topologies of VSIs with coupled inductors permit a zero dead-time.

A half-bridge three-level inverter with coupled inductors is proposed in [25], which consists of two power switches, two diodes and two (one pair of) coupled inductors, while split dc-link capacitors are still needed. The need for split dc-link capacitors can be avoided by doubling the number of power semiconductors and coupled inductors. The augmented topology can generate a five-level output waveform [23, 24]. The main advantage of the proposed topologies in [19, 23–25] is the elimination of the dead-time, since inductors are placed in series with switches of the converter legs. Hereinafter, Floricau *et al.* [22] presented five-level hybrid inverter, which combines the coupled inductors with the conventional multilevel topologies. Owing to the presence of split capacitors, the risk of unbalanced voltages exists if the inverters are not correctly modulated. The VSI with only one dc source and no split capacitors, presented in [21], may be the most successful topology with balanced coupled inductors, which can provide five-level waveforms with only six power switches and two (one pair of) coupled inductors. In this paper and in order to increase the number of achievable output voltage levels and at the same time reduce the number of semiconductor devices, dc voltage sources and capacitors, four different novel nine-level VSIs are proposed and their operation principles are analysed and explained in details. As a common feature, all proposed topologies are composed of only a pair of balanced coupled inductors, two separate dc voltage sources and power transistors. A comprehensive comparative study among different proposed topologies, as well as, other conventional nine-level VSIs, in terms of the number of semiconductors, separate dc voltage sources and capacitors and the rating of semiconductors, is then followed. It should be noted that in all presented topologies, no dc component exists in the inductors currents, which is necessary to minimise the size of the inductors. In the last section, the performance of the proposed VSIs, in conjunction with the proper modulation algorithms, is confirmed through experiments.

2 Coupled inductors operation principle

A pair of balanced coupled inductors is shown in Fig. 1, where both inductors have the same number of turns. As a result, the self- and leakage inductances of these inductors are equal.

Assuming that, L and M are the self- and mutual inductances, respectively, then it is already shown that

$$V_n = \frac{V_a + V_b}{2} \tag{1}$$

This result shows that the common node voltage (n) is the average of the voltages of nodes a and b.

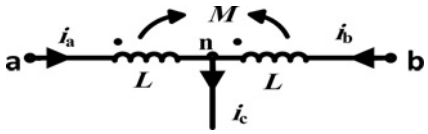

Fig. 1 *Pair of coupled inductors*

3 Generating a nine-level voltage waveform

In this paper, the extended (modified) nearest level control method is suggested for its simplicity and effectiveness. The output voltage of proposed inverters with this control technique is similar to the output waveform of the traditional nine-level inverter with nearest level control method [2, 26]. Fig. 2*a* shows one cycle of the nine-level output voltage and its reference, where different steps are numbered from 1 to 9. In the proposed method, the reference voltage is compared with the available voltage levels, then the level that is the nearest to the reference voltage is selected and the proper switching state is applied to the proposed inverters, corresponding to the appropriate voltage level, from a pre-determined table. It should be noted that in our application and in order to minimise the inductor currents, in steps with a non-zero V_{ab}, the currents in the coupled inductors should increase and decrease in opposite directions consecutively with a relatively high frequency. On the basis of this analysis, in steps with a non-zero V_{ab}, there must be at least two possible switching states with inverse V_{ab} polarity to select from. Otherwise, the currents in the coupled inductors will increase to a large value; V_{ab} is the voltage of the inductors as shown in Fig. 1. Fortunately, this is possible in all proposed topologies, i.e. for output voltage levels with non-zero V_{ab}, there are at least two switching combinations with opposite V_{ab} polarity. To minimise the inductor currents, the switches, which are directly connected to the coupled inductors, are controlled at a relatively high switching frequency in mentioned voltage levels. In other levels, all switches are controlled at low frequency. The flowchart of the proposed extended nearest level control applied to the proposed converters

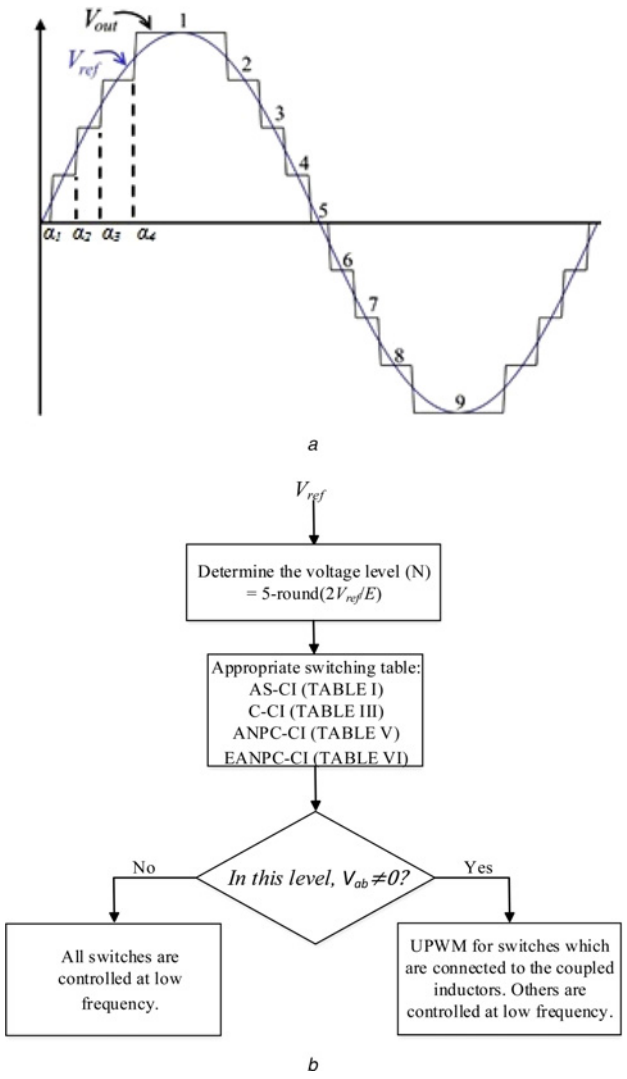

Fig. 2 *The extended nearest level switching method*

a Reference and output voltages of the nearest level control
b Flowchart of the extended nearest level control

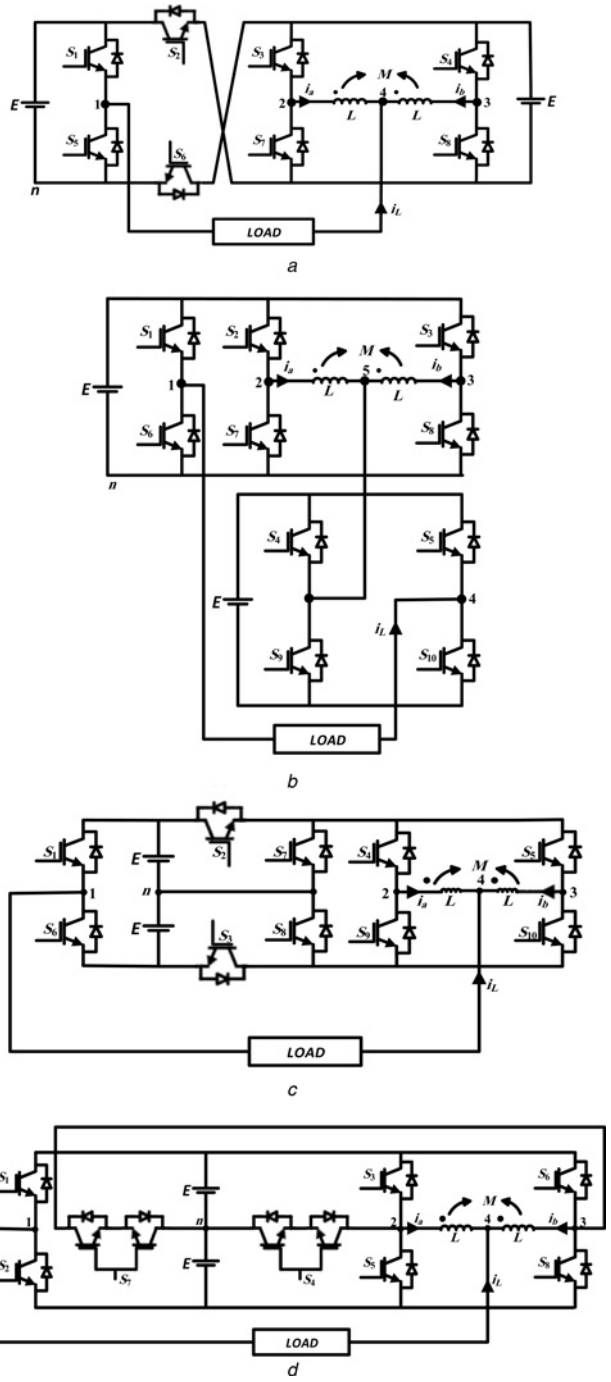

Fig. 3 *Power circuit of*

a AS-CI inverter
b C-CI inverter
c ANPC-CI inverter
d EANPC-CI inverter

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Table 1 Switching states of the AS-CI inverter

Output voltage level	(S_1, S_2, S_3, S_4)	V_{23}	V_{14}
1	(1, 0, 0, 0)	0	$2E$
2	(1, 0, 1, 0)	E	$3E/2$
	(1, 0, 0, 1)	$-E$	
3	(1, 0, 1, 1)	0	E
	(0, 0, 0, 0)		
4	(0, 0, 1, 0)	E	$E/2$
	(0, 0, 0, 1)	$-E$	
5	(0, 0, 1, 1)	0	0
	(1, 1, 0, 0)		
6	(1, 1, 1, 0)	E	$-E/2$
	(1, 1, 0, 1)	$-E$	
7	(1, 1, 1, 1)	0	$-E$
	(0, 1, 0, 0)		
8	(0, 1, 1, 0)	E	$-3E/2$
	(0, 1, 0, 1)	$-E$	
9	(0, 1, 1, 1)	0	$-2E$

is already given in Fig. 2*b*, while details of deriving the proper switching table for each proposed topology are presented in the following section.

4 Proposed nine-level VSIs with coupled inductors

In what follows, four novel VSIs are proposed for single-phase applications, which utilise a pair of balanced coupled inductors to generate a nine-level output voltage from two separate dc sources.

4.1 Active series voltage sources with coupled inductors (AS-CI) VSI

Fig. 3*a* shows the power circuit of the proposed AS-CI inverter. As shown in this figure, the single-phase nine-level AS-CI inverter is formed by adding two power switches and one dc voltage source to the proposed inverter in [21]. Also, this inverter is based on the topology proposed in [11], by substituting a half-bridge leg by the cell with the coupled inductors. In this figure, E is the voltage of dc sources. To avoid the short circuit of dc sources, the control of the power devices S_1–S_5, S_2–S_6, S_3–S_7 and S_4–S_8 must be complementary. According to (1), the output voltage of the AS-CI inverter is

$$V_{14} = V_{1n} - V_{4n} = V_{1n} - \frac{V_{2n} + V_{3n}}{2}. \quad (2)$$

Table 1 summarises all possible switching states of the AS-CI inverter. In this table, '1' and '0' indicate the ON- and OFF-states of the switches, respectively. Obvious from Table 1, this inverter can produce nine different levels in the output voltage waveform, V_{14}.

It is clear from Table 1 that the switch S_2 is always ON when $V_{14} \leq 0$ and is kept OFF when $V_{14} \geq 0$. As a result, S_2 and S_6 are controlled at the frequency of the reference signal, which simplifies the control and reduces the switching losses. In addition, S_1 and S_5 are switched at tripled the reference frequency. In the proposed AS-CI inverter, for the voltage levels 2, 4, 6 and 8 that the voltage on the coupled inductors V_{23} is not zero, there are two switching states, with inverse V_{23} polarity to choose from. This feature can be used to minimise the inductors current. To apply the extended nearest level control method to the AS-CI inverter, at output voltage levels 3, 5 and 7, one of the two possible switching states will be selected. However, at output voltage levels 2, 4, 6 and 8, the switching state must alter between two possible states, as shown in Table 1, at a relatively high frequency. It is important to note that the dwell time of these two switching states must be equal, so that the inductor is fully discharged after two consecutive switchings. Indeed, the control signals of S_3–S_7 and S_4–S_8 are similar to the uniform pulse-width modulation (UPWM), which the dwell times of ON- and OFF-states are the same [27]. On the basis of above description, one can conclude that the switches S_3, S_4, S_7 and S_8 are controlled at high frequency only at output voltage levels 2, 4, 6 and 8. While, at all output voltage levels, the switches S_1, S_2, S_5 and S_6 are controlled at low frequency. As a result, the switching losses are expected to be low.

4.2 Cascaded with coupled inductors (C-CIs) VSI

The power circuit of the proposed C-CI inverter is shown in Fig. 3*b*. This inverter is formed by adding a half-bridge leg and a pair of coupled inductors to the well-known cascaded multilevel inverter. The output terminals are nodes 1 and 4. To avoid the short circuit of voltage sources, the switches in one leg are assumed to switch complementarily. Attention should be paid that the dc voltage sources in this inverter must be isolated. According to (1), the output voltage of the C-CI inverter can be expressed as

$$\begin{aligned} V_{14} &= V_{1n} - V_{4n} = V_{1n} - V_{5n} + (V_{5n} - V_{4n}) \\ &= V_{1n} - \frac{V_{2n} + V_{3n}}{2} + V_{54}. \end{aligned} \quad (3)$$

All possible switching states are summarised in Table 2. Evidently, except for the minimum and maximum voltage levels ($-2E$ and $2E$), there are more than one possible switching state for other voltage levels. More precisely, voltage levels $3E/2$ and $-3E/2$ have two switching possibilities, voltage levels $-E$ and E have four switching possibilities and voltage levels $E/2$, 0 and $-E/2$ have six switching possibilities. Owing to the several possible switching states at different levels, many combinations can be proposed for turn-on and -off of the power switches. A proposal with the minimum commutations of switches is proposed in Table 3. According to Table 3, in the proposed switching strategy, the switches S_1 and S_4 are ON if $V_{14} \geq 0$. As a result, four power switches S_1, S_4, S_6 and S_9 operate at the frequency of the reference signal. The switches S_5 and S_{10} are also switched at tripled the reference frequency. To apply the extended nearest level control method to the C-CI inverter, at output voltage levels 3, 5 and 7,

Table 2 Switching states of the C-CI inverter

Output voltage level	(S_1, S_2, S_3, S_4, S_5)	V_{23}	V_{14}
1	(1, 0, 0, 1, 0)	0	$2E$
2	(1, 1, 0, 1, 0)	E	$3E/2$
	(1, 0, 1, 1, 0)	$-E$	
3	(0, 0, 0, 1, 0)	0	E
	(1, 0, 0, 0, 0)		
	(1, 0, 0, 1, 1)		
	(1, 1, 1, 1, 0)		
4	(0, 1, 0, 1, 0)	E	$E/2$
	(1, 1, 0, 0, 0)		
	(1, 1, 0, 1, 1)		
	(0, 0, 1, 1, 0)	$-E$	
	(1, 0, 1, 0, 0)		
	(1, 0, 1, 1, 1)		
5	(0, 0, 0, 0, 0)	0	0
	(0, 0, 0, 1, 1)		
	(0, 1, 1, 1, 0)		
	(1, 0, 0, 0, 1)		
	(1, 1, 1, 0, 0)		
	(1, 1, 1, 1, 1)		
6	(0, 1, 0, 0, 0)	E	$-E/2$
	(0, 1, 0, 1, 1)		
	(1, 1, 0, 0, 1)		
	(0, 0, 1, 0, 0)	$-E$	
	(0, 0, 1, 1, 1)		
	(1, 0, 1, 0, 1)		
7	(0, 0, 0, 0, 1)	0	$-E$
	(0, 1, 1, 0, 0)		
	(0, 1, 1, 1, 1)		
	(1, 1, 1, 0, 1)		
8	(0, 1, 0, 0, 1)	E	$-3E/2$
	(0, 0, 1, 0, 1)	$-E$	
9	(0, 1, 1, 0, 1)	0	$-2E$

Table 3 Switching states of the C-CI inverter with minimum commutations

Output voltage level	(S_1, S_2, S_3, S_4, S_5)	V_{23}	V_{14}
1	(1, 0, 0, 1, 0)	0	$2E$
2	(1, 1, 0, 1, 0)	E	$3E/2$
	(1, 0, 1, 1, 0)	$-E$	
3	(1, 1, 1, 1, 0)	0	E
	(1, 0, 0, 1, 1)		
4	(1, 1, 0, 1, 1)	E	$E/2$
	(1, 0, 1, 1, 1)	$-E$	
5	(1, 1, 1, 1, 1)	0	0
	(0, 0, 0, 0, 0)		
6	(0, 1, 0, 0, 0)	E	$-E/2$
	(0, 0, 1, 0, 0)	$-E$	
7	(0, 1, 1, 0, 0)	0	$-E$
	(0, 0, 0, 0, 1)		
8	(0, 1, 0, 0, 1)	E	$-3E/2$
	(0, 0, 1, 0, 1)	$-E$	
9	(0, 1, 1, 0, 1)	0	$-2E$

Table 5 Switching states of the ANPC-CI inverter with minimum commutations and inductor currents

Output voltage level	(S_1, S_2, S_3, S_4, S_5)	V_{23}	V_{14}
1	(1, 0, 1, 0, 0)	0	$2E$
2	(1, 0, 1, 1, 0)	E	$3E/2$
	(1, 0, 1, 0, 1)	$-E$	
3	(1, 0, 1, 1, 1)	0	E
	(1, 1, 0, 0, 0)		
4	(1, 1, 0, 1, 0)	E	$E/2$
	(1, 1, 0, 0, 1)	$-E$	
5	(1, 1, 0, 1, 1)	0	0
	(0, 0, 1, 0, 0)		
6	(0, 0, 1, 1, 0)	E	$-E/2$
	(0, 0, 1, 0, 1)	$-E$	
7	(0, 0, 1, 1, 1)	0	$-E$
	(0, 1, 0, 0, 0)		
8	(0, 1, 0, 1, 0)	E	$-3E/2$
	(0, 1, 0, 0, 1)	$-E$	
9	(0, 1, 0, 1, 1)	0	$-2E$

one of the two possible switching states will be selected. As a result, the switches S_2, S_3, S_7 and S_8 are controlled at relatively high frequency only at output voltage levels 2, 4, 6 and 8, while at all output voltage levels, the switches S_1, S_4, S_5, S_6, S_9 and S_{10} are controlled at low frequency. So, the switching losses of the C-CI inverter reduce significantly.

4.3 Active neutral point clamped with coupled inductors (ANPC-CI) VSI

The proposed single-phase nine-level ANPC-CI inverter is shown in Fig. 3*c*. This converter is realised by adding two power switches to the proposed topology in [22] (which is formerly based on ANPC-flying capacitor (FC) converter). In ANPC-CI inverter, the pair of balanced coupled inductors is placed between nodes 2 and 3 and the output terminals of the inverter are nodes 1 and 4. In this inverter, S_1–S_6, S_2–S_7, S_3–S_8, S_4–S_9 and S_5–S_{10} are complementary switch pairs. In this inverter, dc voltage sources are not isolated from each other; as a result, they can be generated from one supply (using a capacitor divider). The states of the switches for each output voltage level are given in Table 4. It is clear from Table 4 that there exist two switching possibilities at the output voltage levels 1, 2, 4, 6, 8 and 9, and more than two at others. As a result, many switching combinations can be proposed for this inverter. Again, a combination with minimum commutations and at the same time minimum inductor currents is proposed in Table 5. In this proposal, those switching states with $V_{23} = 2E$ and $-2E$ at voltage levels 3 and 7 are not used, because these states results in increased inductor currents and losses.

The switches S_4, S_5, S_9 and S_{10} are controlled at a relatively high frequency, while S_1 and S_6 are switched at the reference frequency and S_2, S_3, S_7 and S_8 at three times the reference frequency.

Table 4 Switching states of the ANPC-CI inverter

Output voltage level	(S_1, S_2, S_3, S_4, S_5)	V_{23}	V_{14}
1	(1, 0, 1, 0, 0)	0	$2E$
	(1, 1, 1, 0, 0)		
2	(1, 0, 1, 1, 0)	E	$3E/2$
	(1, 0, 1, 0, 1)	$-E$	
3	(1, 0, 0, 0, 0)	0	E
	(1, 0, 0, 0, 1)		
	(1, 0, 0, 1, 0)		
	(1, 0, 0, 1, 1)		
	(1, 0, 1, 1, 1)		
	(1, 1, 0, 0, 0)		
	(1, 1, 1, 1, 0)	$2E$	
	(1, 1, 1, 0, 1)	$-2E$	
4	(1, 1, 0, 1, 0)	E	$E/2$
	(1, 1, 0, 0, 1)	$-E$	
5	(0, 0, 1, 0, 0)	0	0
	(0, 1, 1, 0, 0)		
	(1, 1, 0, 1, 1)		
	(1, 1, 1, 1, 1)		
6	(0, 0, 1, 1, 0)	E	$-E/2$
	(0, 0, 1, 0, 1)	$-E$	
7	(0, 0, 0, 0, 0)	0	$-E$
	(0, 0, 0, 0, 1)		
	(0, 0, 0, 1, 0)		
	(0, 0, 0, 1, 1)		
	(0, 0, 1, 1, 1)		
	(0, 1, 0, 0, 0)		
	(0, 1, 1, 1, 0)	$2E$	
	(0, 1, 1, 0, 1)	$-2E$	
8	(0, 1, 0, 1, 0)	E	$-3E/2$
	(0, 1, 0, 0, 1)	$-E$	
9	(0, 1, 0, 1, 1)	0	$-2E$
	(0, 1, 1, 1, 1)		

4.4 Extended ANPC-CIs (EANPC-CIs) VSI

The power circuit of the EANPC-CI inverter is shown in Fig. 3*d*, which is based on the structure proposed in [21], just replacing the half-bridge legs with the T-type legs. In this converter, the simultaneous turn-on of S_3 or S_5 with S_4 and S_6 or S_8 with S_7 causes the voltage sources to be short-circuited. Therefore, the simultaneous turn-on of the aforementioned switches is not permitted. In addition, S_1–S_2, S_3–S_5 and S_6–S_8 must not turn-on simultaneously. Table 6 shows all possible switching states of the EANPC-CI inverter. As already mentioned, those switching states with $V_{23} = 2E$ or $-2E$ at the output voltage levels 3 and 7 are not used, i.e. the other switching state with a zero voltage on the coupled inductors is used instead. Two switches S_1 and S_2 operate at the frequency of the reference voltage, while others are switched at a relatively high frequency in some of output levels.

Evidently, for all proposed topologies along with the adopted modulation algorithm, all power switches are controlled at the low

Table 6 Switching states of EANPC-CI inverter

Output voltage level	(S_1, S_3, S_4, S_6, S_7)	V_{23}	V_{14}
1	(1, 0, 0, 0, 0)	0	$2E$
2	(1, 0,1, 0, 0)	E	$3E/2$
	(1, 0, 0, 0, 1)	$-E$	
3	(1, 0, 1, 0, 1)	0	E
	(1, 1, 0, 0, 0)	$2E$	
	(1, 0, 0, 1, 0)	$-2E$	
4	(1, 1, 0, 0, 1)	E	$E/2$
	(1, 0, 1, 1, 0)	$-E$	
5	(1, 1, 0, 1, 0)	0	0
	(0, 0, 0, 0, 0)		
6	(0, 0, 1, 0, 0)	E	$-E/2$
	(0, 0, 0, 0, 1)	$-E$	
7	(0, 0, 1, 0, 1)	0	$-E$
	(0, 1, 0, 0, 0)	$2E$	
	(0, 0, 0, 1, 0)	$-2E$	
8	(0, 1, 0, 0, 1)	E	$-3E/2$
	(0, 0, 1, 1, 0)	$-E$	
9	(0, 1, 0, 1, 0)	0	$-2E$

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Table 7 Power semiconductor requirements of proposed inverters

Inverter	Current|voltage rating of switches										Total conducting current	Total blocking voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}		
AS-CI	i_L|E	i_L|2E	i_L/2|E	i_L/2|E	i_L|E	i_L|2E	i_L/2|E	i_L/2|E	–	–	6i_L	10E
C-CI	i_L|E	i_L/2|E	i_L/2|E	i_L|E	i_L|E	i_L|E	i_L/2|E	i_L/2|E	i_L|E	i_L|E	8i_L	10E
ANPC-CI	i_L|2E	i_L|E	i_L|E	i_L/2|2E	i_L/2|2E	i_L|2E	i_L|E	i_L|E	i_L/2|2E	i_L/2|2E	8i_L	12E
EANPC-CI	i_L|2E	i_L|2E	i_L/2|2E	i_L|E	i_L/2|2E	i_L/2|2E	i_L|E	i_L/2|2E	–	–	6i_L	14E

frequency, except for those connected to the coupled inductors, which are controlled at the high frequency in voltage levels 2, 4, 6 and 8. Fortunately, these power switches carry half of the load current ($i_L/2$). Thus, the presented inverters are suitable for low-to-medium power applications (such as motor drives), to increase the output current, while the switched current through the high-frequency power devices is reduced to 50% of the load current.

5 Power semiconductor requirements

In this section and to clarify the advantages and disadvantages of the proposed inverters, a comparison from different aspects is done. The AS-CI inverter needs eight power switches, while the other proposed topologies need ten switches in their circuit. The number of gate drivers is eight in the AS-CI and EANPC-CI inverters and ten in other proposed inverters. So it can be concluded that the AS-CI is the best in terms of the number of switches and gate drivers. The conducting current and the blocking voltage of semiconductors have important roles in the cost of the multilevel inverters. In all proposed topologies, four switches (switches which are directly connected to the coupled inductors) are rated for half of the load current ($i_L/2$), while the other switches carry the full load current (i_L). The current ratings of all switches are shown in Table 7. It is notable that S_4 and S_7 are realised by two switches in series in the EANPC-CI inverter. Therefore, the current rating of these switches is reported as i_L in Table 7. The total conducting current of switches is the sum of the current rating of all switches in the inverter circuit. It is clear from Table 7 that the AS-CI and EANPC-CI inverters take benefit of a lower total conducting current. Also, the blocking voltage of switches are shown in Table 7. Again for the EANPC-CI inverter, the switches S_4 and S_7 are composed of two switches with the blocking voltage of $E/2$ for each one. As it can be seen, the total blocking voltage for the AS-CI and C-CI inverters is minimum. Of course, all switches of the C-CI inverter are rated for the same voltage, which is an interesting feature of this converter.

6 Proposed topologies among other well-known competitors

The principal reason behind the suggestion of novel multilevel inverters is to increase the number of output voltage levels, while requiring the minimum number of semiconductors, dc voltage sources and capacitors. To better highlight the features of the proposed inverters, they are compared with other conventional multilevel inverters from different points of view. Since all proposed inverters have nine-level output voltages, the comparison is done with the well-known nine-level topologies, presented yet. Since the voltage steps are $E/2$ in the proposed inverters, so as a matter of fare comparison, in conventional inverters, all dc voltage sources are equal to $E/2$. Table 8 summarises the comparison results for the number of power semiconductors, dc voltage sources, independent gate driver circuits and the total conducting current and blocking voltage of semiconductors. Total number of

Table 8 Comparison of converters

Inverter	Reference	$N_{switches}$	$N_{sources}$	$N_{drivers}$	Total conducting current	Total blocking voltage
switched dc sources (SDCSs)	[11]	10	4	10	10i_L	8E
T-type AQ2 multilevel inverter (MLI)	[15, 28]	10	4	7	10i_L	12E
switched series/parallel sources (SSPSs)	[17]	13	4	13	13i_L	12.5E
cascaded H-bridge	[29]	16	4	16	16i_L	8E
CPC-ILS	[30]	16	8	16	16i_L	8E
cascaded half-bridge-based multilevel dc link (MLDCL)	[31, 32]	12	4	12	12i_L	12E
series connected switched sources (SCSSs)	[33]	12	4	12	12i_L	14.25E
cascaded bipolar switched cells (CBSCs)	[34]	20	4	10	20i_L	16E
multilevel module (MLM)	[35]	14	4	9	14i_L	16E
reversing voltage (RV)	[36]	12	4	12	12i_L	12E
AS-CI	–	8	2	8	6i_L	10E
C-CI	–	10	2	10	8i_L	10E
ANPC-CI	–	10	2	10	8i_L	12E
EANPC-CI	–	10	2	8	6i_L	14E

Table 9 Voltage rating of switches in conventional inverters

Inverter	Reference	Voltage rating of switches															
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
SDCSs	[11]	$E/2$	$E/2$	E	E	E	E	E	E	$E/2$	$E/2$	–	–	–	–	–	–
T-type MLI	[15, 28]	3$E/2$	E	3$E/2$	2E	2E	2E	2E	–	–	–	–	–	–	–	–	–
SSPSs	[17]	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	2E	2E	2E	2E	–	–	–
cascaded H-bridge	[29]	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$
CPC-ILS	[30]	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$
cascaded half-bridge-based MLDCL	[31, 32]	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	2E	2E	2E	2E	–	–	–	–
SCSS	[33]	$E/2$	$E/2$	$E/2$	E	$E/2$	3$E/2$	$E/2$	2E	2E	2E	2E	2E	–	–	–	–
CBSCs	[34]	2E	2E	3$E/2$	3$E/2$	E	E	3$E/2$	3$E/2$	2E	2E	–	–	–	–	–	–
MLM	[35]	2E	3$E/2$	E	3$E/2$	2E	2E	2E	2E	2E	–	–	–	–	–	–	–
RV	[36]	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	$E/2$	2E	2E	2E	2E	–	–	–	–

switches in a multilevel inverter circuit is one of the important parameters, which determines the cost as well as the size of the converter. Table 8 illustrates that the AS-CI inverter needs the least number of power switches. Also, it is obvious that the proposed structures realise the nine-level voltage from the minimum number of dc sources. Of course, in the ANPC-CI and EANPC-CI inverters, the voltage sources can be simply produced from just one dc supply by using two series connected capacitors. Apparently, increasing the number of gate drivers leads to increased costs, power losses and complexity. According to Table 8, the proposed inverter in [15, 28] needs the fewest number of gate drivers, i.e. seven, while the AS-CI and EANPC-CI inverters require only eight gate driver circuits. The total conducting current and the total blocking voltage of all semiconductors are other converter figure-of-merits, which measure how well a converter utilises its semiconductor devices and are quantities to be minimised. For the proposed structures in [11, 15, 17, 28–36], the rated currents of all switches are equal to the rated load current. On the other side, some switches are rated for half of the load current ($i_L/2$) in the proposed topologies in this paper. For conventional inverters, the blocking voltage of switches are shown in Table 9 of the Appendix. It is clear from Table 8 that the total conducting current is substantially reduced in the proposed inverters. So, the proposed inverters are suitable solutions to increase the output current, while the current rating of switches is decreased compared with other available converter topologies. As it can be observed from Table 8, the total blocking voltages of proposed inverters in [11, 29, 30] are minimum. Nevertheless, the total blocking voltage of the AS-CI and C-CI inverters is also low compared with other topologies. Therefore, one can conclude that the proposed converters are appropriate for low-to-medium power applications (such as motor drives), especially for high-current cases. The coupled inductors may be the flaw of the proposed inverters. This disadvantage is well traded with a lower size, weight and core losses of the ac filter inductor.

7 Fourier analysis

The extended nearest level control, with the output voltage waveform of Fig. 2*a* is employed in our study. According to this figure, the Fourier series of the output voltage waveform is written as follows

$$V_{\text{out}}(t) = \sum_{n=1,3,\ldots}^{\infty} V_n = \sum_{n=1,3,\ldots}^{\infty} \left[\frac{2E}{n\pi}\sum_{k=1}^{4}\cos(n\alpha_k)\right]\sin(n\omega t) \quad (4)$$

where α_k is the switching angle. The angles α_k are obtained as

$$\alpha_k = \arcsin\frac{(2k-1)E}{4V_{\text{ref, peak}}}. \quad (5)$$

The total harmonic distortion (THD) of the output voltage can be obtained as

$$\text{THD} = \frac{1}{V_1}\sqrt{\sum_{n=3,5,\ldots}^{\infty} V_n^2}. \quad (6)$$

Theoretically, to get the exact THD value, infinite harmonics need to be calculated. However, it is not possible. So, certain number of harmonics will be considered. Usually, $n = 25$ is reasonably accepted. According to above discussion, the calculated THD of the output voltage is equal to 7.29%.

8 Power losses analysis

In this section, theoretical power losses and efficiency of proposed inverters are calculated. Losses include power devices losses and coupled inductors losses. During the operation of metal–oxide–semiconductor field-effect transistors (MOSFETs), mostly two types of losses occur: conduction losses and switching losses. Switching losses occur during the switch-on and the switch-off transients. The average switching loss of a switch during each transition of turn-on and turn-off can be found as

$$P_{\text{sw,on}} = \frac{fV_{\text{block}}It_{\text{on}}}{6} \quad (7)$$

$$P_{\text{sw,off}} = \frac{fV_{\text{block}}I't_{\text{off}}}{6}. \quad (8)$$

where I and I' are the currents, which pass through the MOSFETs after turning ON and before turning OFF, respectively. Total switching losses can be calculated by (9)

$$P_{\text{sw, total}} = \sum_{i=1}^{N_{\text{switch}}}\left(\sum_{j=1}^{N_{\text{on}}} p_{\text{sw, on, }ij} + \sum_{j=1}^{N_{\text{off}}} p_{\text{sw, off, }ij}\right). \quad (9)$$

In above equation, N_{on} and N_{off} are the number of turn-on and turn-off switching states during a fundamental period and N_{switch} is the number of power switches in the inverter. The conduction losses occur in the switches and in the anti-parallel diodes. The conduction losses for the MOSFETs can be calculated from (10) and for the anti-parallel diodes can be calculated from (11)

$$P_{c,M} = R_{\text{DS, on}}I^2_{\text{M, rms}} \quad (10)$$

$$P_{c,\text{D}} = V_{\text{D0}}I_{\text{D, av}} + R_{\text{D}}I^2_{D,\text{rms}} \quad (11)$$

where $R_{\text{DS,on}}$, $I_{\text{M,rms}}$, V_{D0}, $I_{\text{D,av}}$, R_{D} and $I_{\text{D,rms}}$ are drain–source ON-state resistance, root-mean-square (RMS) value of the MOSFET current, forward voltage drop of diode, average diode current, diode ON-state resistance and RMS diode current, respectively.

Coupled inductors losses include core and copper losses. The copper loss is calculated as

$$P_{\text{cu}} = R_1I_1^2 + R_2I_2^2. \quad (12)$$

In (12), R_1, R_2, I_1 and I_2 represent the resistance and RMS current of coupled inductors. Core loss is the result of an alternating magnetic field in the core material. The loss generated for a given material is a function of operating frequency and the total flux swing (ΔB), which is described by the following formula

$$\Delta B = \frac{E_{\text{pk}}t10^8}{AN}. \quad (13)$$

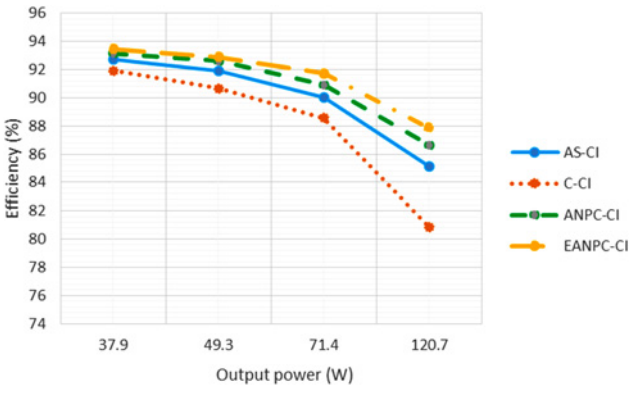

Fig. 4 *Overall efficiency as a function of output power (theoretically calculated)*

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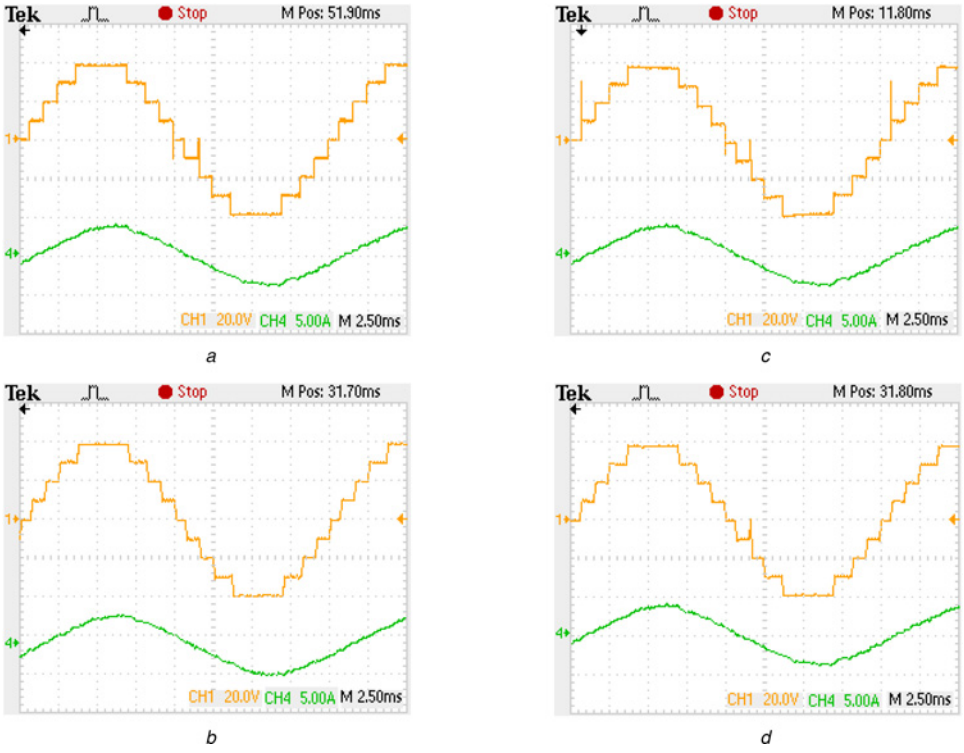

Fig. 5 *Experimental results of the output voltage and current under RL load when M = 8 for*

a AS-CI
b C-CI
c ANPC-CI
d EANPC-CI

where ΔB, E_{pk}, t, A and N are the peak-to-peak flux density (gauss), the peak voltage across the coil during t (volts), the duration of applying the voltage (seconds), the cross-sectional area (square centimetres) and the number of turns, respectively. Now, based on the core loss curve, one can simply determine the core losses.

Finally, the efficiency of the inverters is calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{sw, total}} + P_{c,\text{total}} + P_{\text{cu}} + P_{\text{core}}}. \tag{14}$$

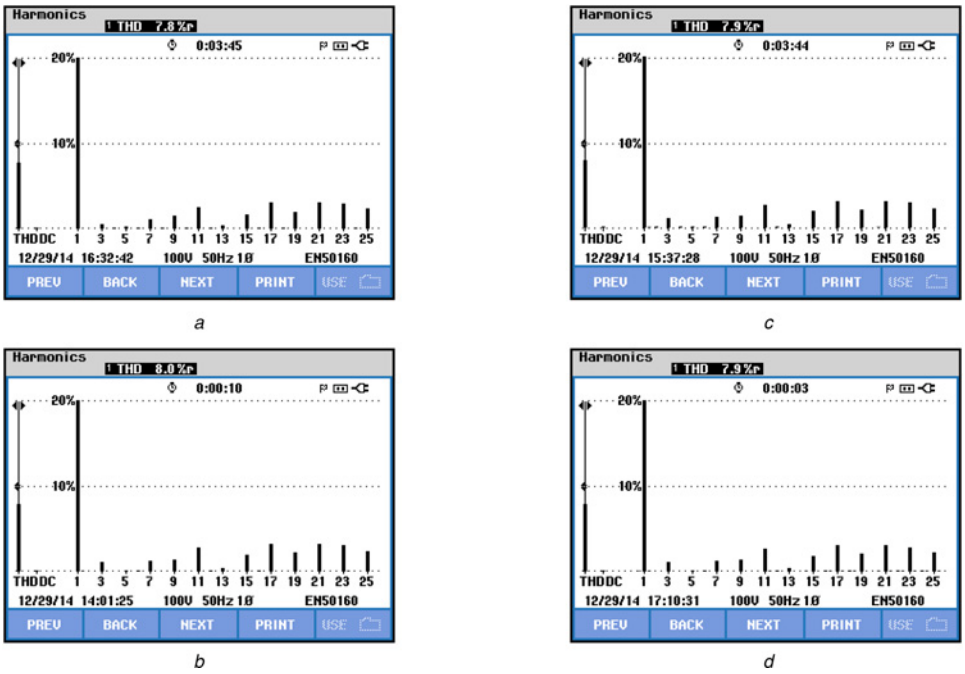

Fig. 6 *Harmonic spectrum of the output voltage under RL load when M = 8 for*

a AS-CI
b C-CI
c ANPC-CI
d EANPC-CI

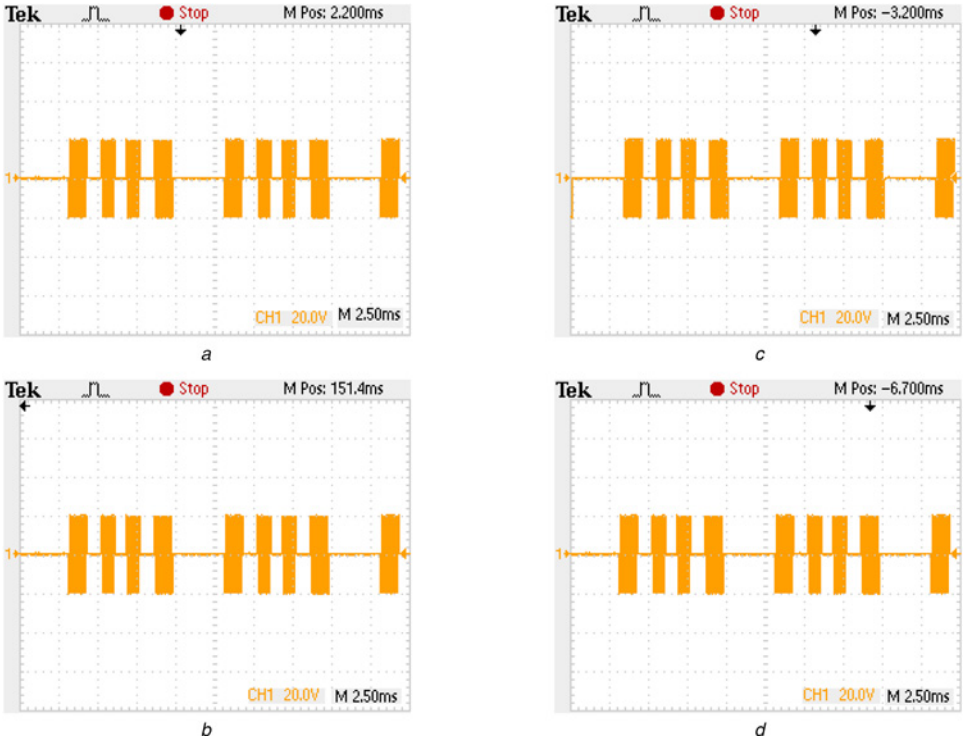

Fig. 7 *Experimental results of the inductors voltage (V_{23}) under RL load when M = 8 for*

a AS-CI
b C-CI
c ANPC-CI
d EANPC-CI

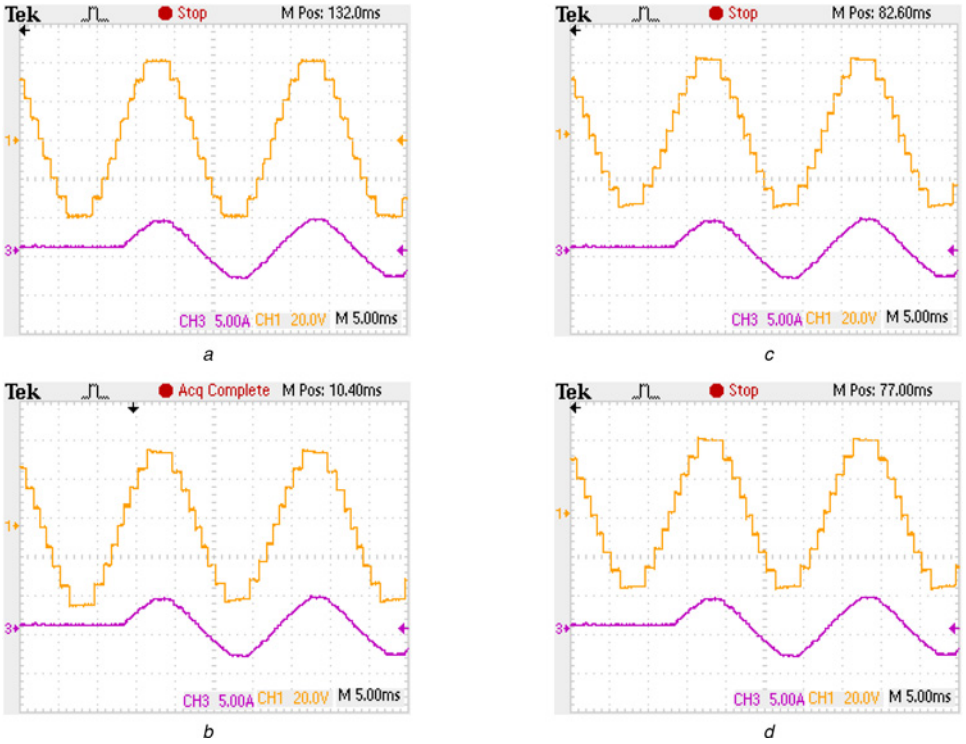

Fig. 8 *Experimental results of the output voltage and current when the load is changed from no-load to RL load (M = 8) for*

a AS-CI
b C-CI
c ANPC-CI
d EANPC-CI

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The total power losses and efficiency of the proposed inverters are calculated under various output powers and the results are shown in Fig. 4. According to this figure, the EANPC-CI offers the maximum efficiency among the proposed converters. These results will be confirmed by experimental measurements under the same conditions.

9 Performance evaluation

The performance of the proposed inverters is validated through experimental tests. The voltage and current waveforms are analysed in details. In all experiments, $E = 20$ V and the self-inductance of coupled inductors is 600 μH. Also, the switching frequency of power switches connected to the coupled inductors is 5 kHz in voltage levels 2, 4, 6 and 8. The MOSFETs used as the switching devices are IRFP460A, which are rated at 500 V and 20 A. The TMS320F28335 DSP from Texas Instruments is used to implement the modulation algorithms. In this switching method, if the modulation index (M) is in the range of 1–3, 3–5, 5–7 and above 7, the output voltage has 3, 5, 7 and 9 levels, respectively. The modulation index is defined in (15). It should be noted that the output voltage is zero if M is in the range of 0–1

$$M = \frac{V_{14\,\mathrm{ref,\,peak}}}{E/4}. \tag{15}$$

Figs. 5–8 show the experimental results of the proposed inverters under RL load ($R = 10\ \Omega$ in series with $L = 3.75$ mH). Fig. 5 shows the output voltage and current when the modulation index is 8 ($V_{14\mathrm{ref,peak}} = 40$ V). All proposed converters produce nine distinct levels in the output voltage waveform, where the steps are half of the dc-link voltage. This figure indicates that the load current waveform becomes sinusoidal because the RL load acts as a low-pass filter.

The harmonic spectrums of the output voltages in previous conditions are illustrated in Fig. 6. All topologies exhibit similar harmonics performance, especially, no dc component exists in the output voltages. The THD of the output voltages is around 8%. Also, the calculated THD of the proposed inverters is equal to 7.29%. The difference with the measurements is mainly caused by the switching dead-times, which is necessary to avoid the short circuit of dc sources. In addition, Fig. 6 shows that the magnitude of low-order harmonics are low. Also, the THD of the load current is around 3%. Fig. 7 illustrates the voltages of the inductor windings (V_{23}). Obviously, the voltages V_{23} do not have any dc component and are the same for all converters. Also, when V_{23} is not zero, this voltage changes polarity alternately, which consequently causes the current of inductors increase and decrease in opposite directions with a relatively high frequency. As a transient condition, the load is suddenly changed from no-load to RL load ($R = 10\ \Omega$ and $L = 3.75$ mH), for which the results are shown in Fig. 8. A fast and smooth current transient is obvious, also the output voltage is unaffected at the instant of load connection. The total power losses and efficiency of the proposed inverters are measured under various output powers and the test results are reported in Fig. 9. These curves are similar to the obtained curves of calculated efficiency. Of course, there are the difference between the numbers of measured and calculated efficiencies, which is caused by the other conduction losses. According to Fig. 9, the EANPC-CI offers the maximum efficiency among the proposed converters. The reason is that in this inverter eight switches carry half of the load current; therefore, the power loss is low. Increased efficiencies are possible by using low loss magnetic cores. A photograph of the experimental setup is shown in Fig. 10. This converter is used for experimental tests of four proposed inverters by changing the MOSFETs connections.

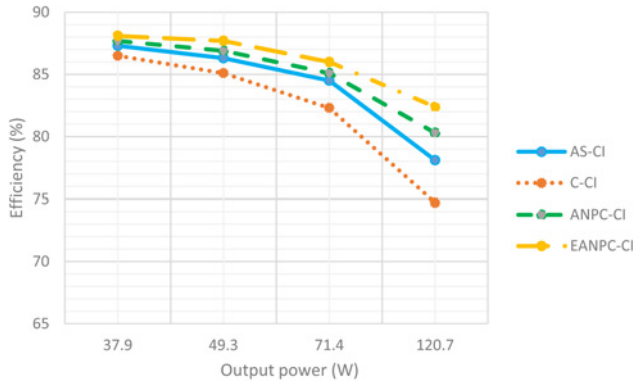

Fig. 9 *Overall efficiency as a function of output power (experimentally measured)*

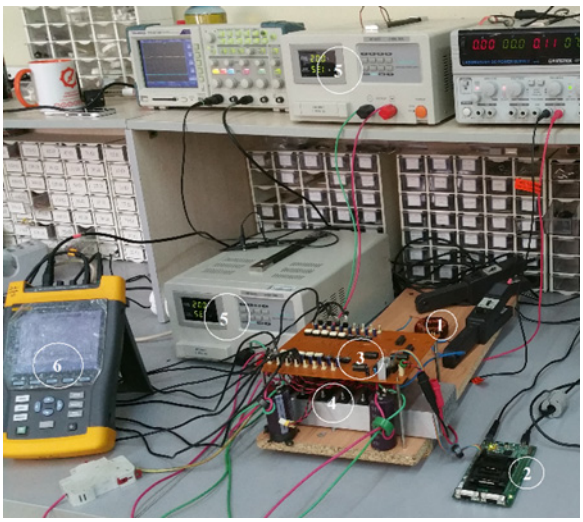

Fig. 10 *Experimental test rig: (i) coupled inductors, (ii) digital signal processor (DSP) board, (iii) MOSFETs drivers, (iv) MOSFETs, (v) dc voltage sources and (6) power analyser*

10 Conclusion

Four single-phase nine-level inverters with balanced coupled inductors are proposed for the first time. These inverters need only two dc sources. The steps of the output voltage are only half of the dc voltage. In addition, the extended nearest level control method is proposed for switching of these converters. The proposed structures were compared with other available topologies from various points of view. According to this comparison, AS-CI inverter needs the least number of power switches and anti-parallel diodes. Also, the proposed structures realise the nine-level voltage from the minimum number of dc sources. Moreover, the total conducting current of the proposed inverters is lower than that of the conventional inverters, which makes them suitable for high-current applications.

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12 Appendix

The power circuits of proposed inverters in [11, 15, 17, 28–36] are illustrated in Fig. 11. For these converters, the rated currents of all switches are equal to the rated load current. For mentioned inverters, the blocking voltage of switches are shown in Table 9. According to this table, the blocking voltage of all switches in the cascaded H-bridge and cascaded power cells with two inverter legs in series (CPC-ILS) inverters are the same, which is a favourable feature.

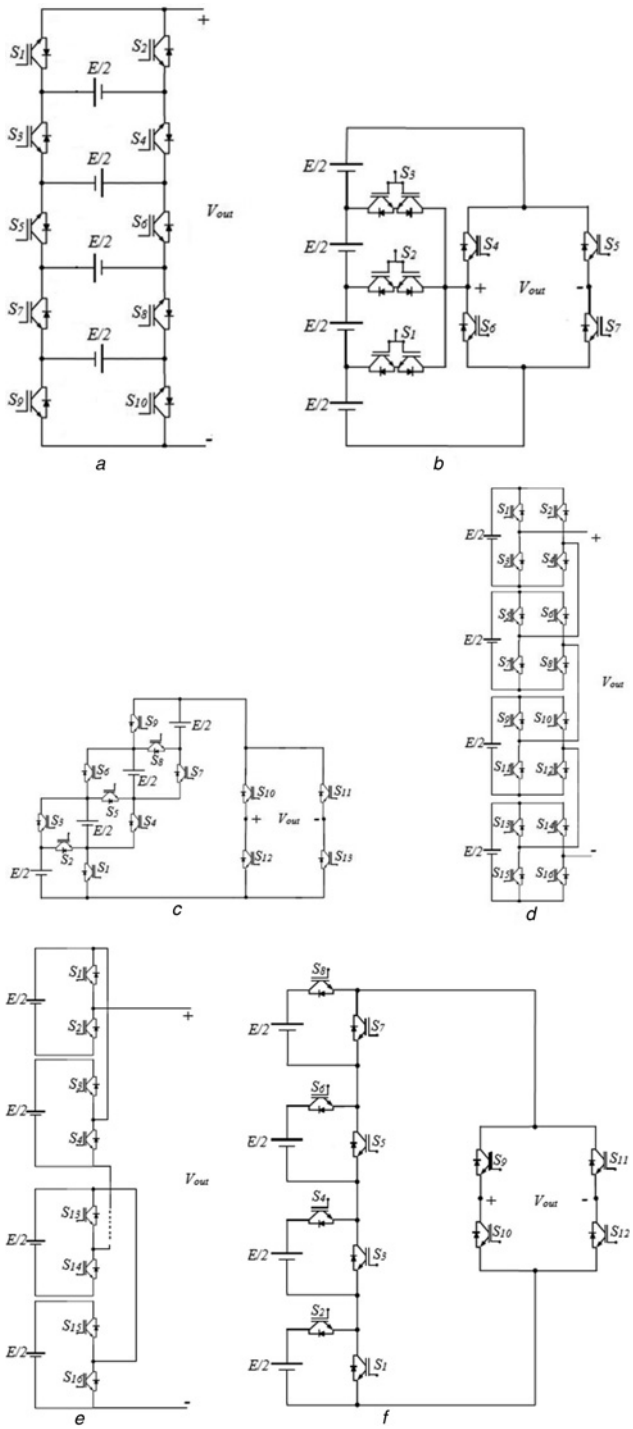

Fig. 11 *Power circuit of proposed inverters in*

a [11]
b [15, 28]
c [17]
d [29]
e [30]
f [31, 32]
g [33]
h [34]
i [35]
j [36]

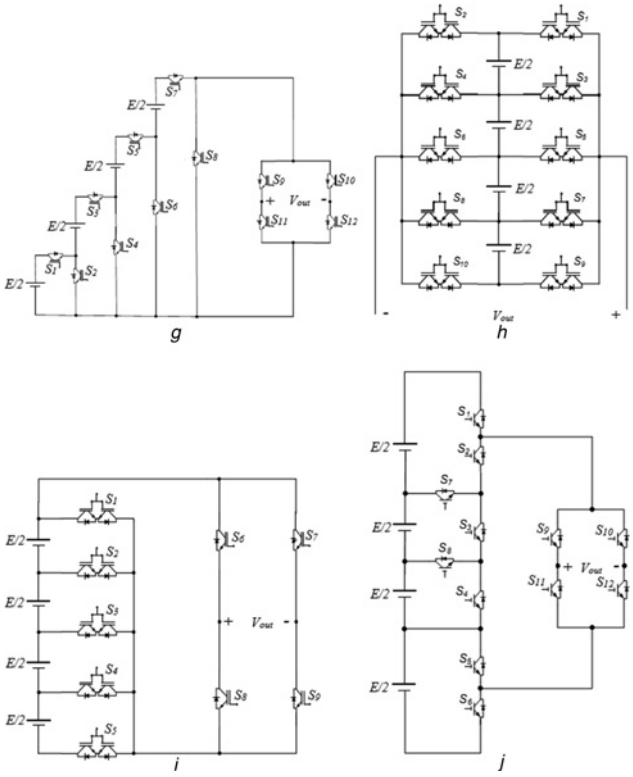

Fig. 11 *Continued*