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A novel reversible design for double edge triggered flip-flops and new designs of reversible sequential circuits

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In recent years, reversible computing and reversible logic has rapidly emerged as one of the promising technologies for designing low-power circuits. It has applications in nanotechnology, quantum computing, quantum dot cellular automata (QCA), DNA computing, optical computing and even in CMOS low-power designs. In this work, we propose basic circuits of reversible sequential logic which are the building blocks of a sequential CPU. First, a novel design of a reversible D-flip flop is proposed which is two times faster than the conventional D flip- flop as well as its reversible counterparts. Further new designs of a sequential shift register, reversible adder and multiplier is proposed. These circuits can be used for constructing a reversible CPU which has sequential elements. Practical implementation of the proposed designs can be achieved with the existing technologies in CMOS and nanotechnology.

Keywords: Reversible logic, Sequential circuits, Reversible double edge triggered flip-flop, Sequential reversible circuits

1. INTRODUCTION

In nanoscale design of current circuits, the power consumption which leads to heat dissipation in computer machinery has become one of the major challenges and attracted the attention of many researchers in various fields of computing such as [1, 2, 3] just to name a few. This challenge represents the strongest motivation to study the field of reversible computing. According to [4, 5, 6], any computation can be performed reversible both logically and thermodynamically which approaches zero energy dissipation. Quantum physics is also reversible by its nature. This is due to the existence of the reverse-time evolution specified by the unitary operator $U^{-1} = U^{\dagger}$ and also the recognition that reversible computation is executed within a quantum-mechanical system. First, R. Landauer in 1961 [4] demonstrated that irreversibility in the computing process which leads to loss of information, requires minimum heat generation in the order of KT for each irreversible function, where K is Boltzmann's constant and T is the absolute temperature at which the computation is performed. He argued that this feature is unavoidable, since the computer performs irreversible operations. Consequently C.H. Bennett in 1973 [5] showed that an irreversible computer can always be made reversible. Since then many reversible circuits for implementing conventional systems have been suggested. In sequential networks, Fredkin and Toffoli [7] have proved that any computation that can be carried out by a conventional irreversible sequential network can also be carried out by a conservative network which is by nature reversible and also they proved that it is ideally possible to build sequential circuits with zero internal power dissipation. When we try to build classical irreversible computers on the atomic scale, the dissipated heat is one of the encountered problems which can be avoided by using reversible computation.

Recently due to the need for low-power designs and also emerging field of nanotechnology, reversible computing has become more attractive. It plays an important role in the field of low-power circuit design and computational nanotechnology. The role of computational nanotechnology and nanomechanics has become critically important in the cycle of growth and development of nanotechnology [8].

The computational nanotechnology is a general term for any computing which uses nanotechnology for implementation of the computing hardware. It is emerging as a fundamental engineering analysis tool for the novel designs of nanodevices [8]. Quantum computing is one of the research areas in this broad field of technology and quantum computing and quantum devices are in the heart of the computational nanotechnology.

Quantum computing is reversible by its nature; this is why reversible computing is most important in nanotechnology. In other words, because logical irreversibility implies physical irreversibility, we need reversible logic in the high-level logical computation to take advantage of quantum devices for computation. Implementing quantum circuits in physical hardware is difficult. There are many implementations of reversible logic in nanotechnology using several unrelated implementation techniques, such as the one found in [9], but most suffer from scalability limitations [10]. On the other hand, physical complexity is not the same for various implementations of reversible circuits. NMR method was used around 2001 to demonstrate Shor's factoring algorithm- the most famous algorithm in quantum computation. Another technology that can be used in reversible logic is quantum dot cellular automata (QCA). Also in the literature there are MOS implementations of reversible gates, such as the one in [11].

However, one of the bottlenecks in combinational circuit design which is worse in reversible circuits is the extremely large amount of hardware they use. One alternative method that is often used (e.g. in general purpose multiprocessor systems) is sequential circuits.

In this paper, new designs of sequential reversible circuits are introduced, which make more efficient use of reversible gates resources. In the following section, we describe the commonly used reversible gates as basis for designing reversible circuits. Section 3 is a survey of the works done in the area of reversible circuits and especially sequential reversible designs. Section 4 discusses our designs of D flip flop, shift register, serial reversible adder and multiplier. Section 5 compares our results with the other works in terms of quantum cost, number of garbage outputs, etc. Finally, in section 6 we present our conclusions of our work and some proposals for future work.

2. REVERSIBLE GATES

A logical gate is considered reversible, if its number of inputs and outputs are equal. It means that there is a one-to-one correspondence between the input and the output vectors and any output pattern have a unique preimage [12]. So the input vector can be restored from the output vector. It was indicated that reversible circuits can avoid the above mentioned energy losses which ensures that in ideal situation there is no power dissipation in the system.

Several reversible gates have been proposed over the past decades. Among them Feynman gate [13], Toffoli gate [14, 7], Fredkin gate [14, 7], DFG (F2G) [15] and Peres gate [16], are the most popular in reversible and quantum literature and have been studied in detail. A comparison of their functionalities and sizes is shown in Fig. 1, 2, 3, 4, and 5. These are 2×2 and 3×3 reversible gates, which means they are 2 input- 2 output and 3 input- 3 output reversible gates respectively.

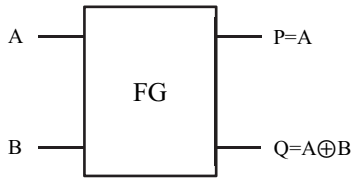

Figure 1 Feynman gate.

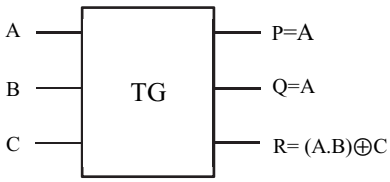

Figure 2 Toffoli gate.

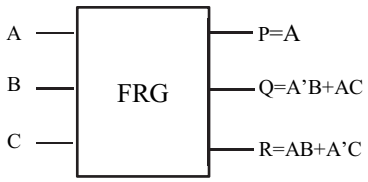

Figure 3 Fredkin gate.

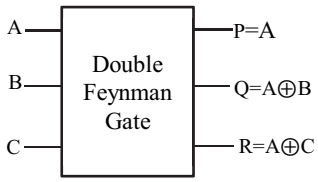

Figure 4 DFG (F2G) gate.

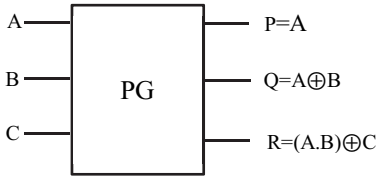

Figure 5 Peres gate.

Among other existing reversible gates is the 4×4 BVF. Having the input vector I (A, B, C, D), this gate will result in the output vector equal to O (P, Q, R, S) = (A, A+B, C, C+D). The implementation of this gate is shown in Figure 6. DPG gate is another 4 × 4 reversible gate with implementation shown in Figure 7. PFAG [17], TSG [18] and HNG [19] are other 4×4

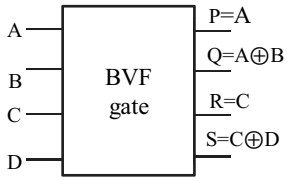

Figure 6 BVF gate.

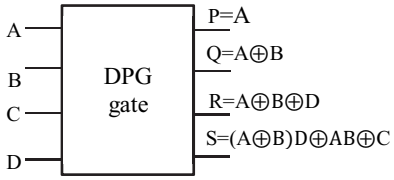

Figure 7 DPG gate.

reversible gates. Their implementations are shown in Figures 8, 9, and 10 respectively where all of them can implement all Boolean functions and can be used as full adder.

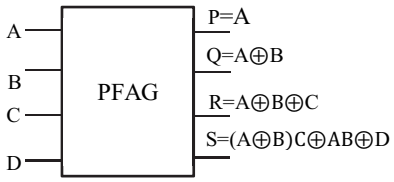

Figure 8 PFAG gate.

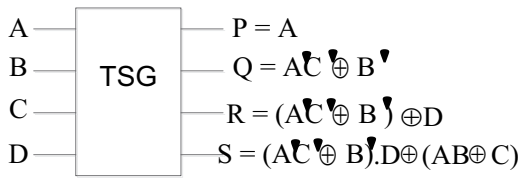

Figure 9 TSG gate.

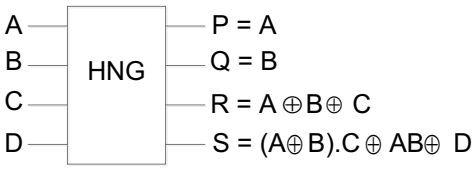

Figure 10 HNG gate.

3. RELATED WORKS

In recent years, many reversible gates and circuits have been proposed as an alternative to conventional irreversible circuits [20, 21, 22, 23, 24, 25]. Examples of these circuits are adders, subtractors and multipliers. Different designs of reversible full adders and adder circuits have been proposed in [11, 18, 21, 22, 24, 26]. Other arithmetic operations such as subtractors, multipliers, dividers as well as sequential arithmetic units which are the essential blocks of computer systems have been proposed in recent years [12, 17, 21, 23, 24, 25, 27, 28, 29, 30, 42]. As sequential elements are the basic blocks of today computers, a variety of sequential reversible elements have been introduced to date. However Fredkin and Toffoli [7] are the first who suggested the reversible design of sequential elements they didn't discuss the construction of basic elements in reversible logic. They compared the conventional and the reversible (or conservative to be precise) sequential networks and claimed that reversible logic could possibly preserve the computing capabilities of ordinary digital logic while satisfying the physical constraints of reversibility and conservation. They showed a conservative logic realization of J-K Flip Flop and a serial adder and introduced a different meaning of delay concept in these circuits.

Subsequently some other attempts have been carried out in the reversible sequential circuits. As the first attempts at the realization and designing of sequential reversible circuits were made by Picton [31], constructing a reversible circuit for SR latch. Thapliyal, et.al [32], suggested other designs of reversible sequential elements with reversible logic synthesis of flip flops. The Flip Flops that are synthesized are RS, J-K, D, T and Master Slave Flip Flops. Rice [33, 41] also discusses the construction of reversible basic memory elements including latches and Flip Flops. It uses Toffoli gate as the basic building block of the Flip Flops. Considering sequential reversible circuits, more recent work on designing reversible serial adder/subtractor has been published by Krishnaveni et al. [34]. Furthermore, they designed D flip flop and shift register by the help of a reversible gate called SRK gate which is used in the reversible serial adder/subtractor.

We consider some criteria in order to compare the results of our proposed approach with the existing literatures, The cost of a reversible circuit is determined by five parameters in the literature, number of garbage outputs, number of constant inputs, quantum cost, number of gates and delay. Number of garbage outputs refers to the number of outputs that are neither used as primary outputs nor for further computations, but they are added to make the circuit reversible [12, 30, 35]. Number of constant inputs refers to the number of inputs which their values are not to be changed in a given circuit and have to be either 0 or 1 in order for the circuit to work. They are also added to make the circuit reversible [30, 35, 36]. Number of gates refers to the total number of reversible gates in a given circuit. The Quantum Cost (QC) is defined as the number of 1×1 or 2×2 reversible quantum or logic gates that are required to realize the circuit [35]. Table 1 shows the quantum cost of some of the different reversible gates used in the literature. Delay is another parameter recently considered in many reversible circuits papers. Some articles have realized the delay as number of reversible or quantum gates in the critical path of the circuit [33, 41] which is an optimistic assumption. To be more precise, we should consider the different delays in each quantum gate separately. According to [37] and [38], the delay of basic quantum gates, i.e. 1×1 and 2×2 reversible gates is considered $\Delta$and the delay of other quantum circuits is equal to the number of delay levels of the gate where each level can be realized using basic quantum gates. So the delay of Feynman gate is $\Delta$and the delay of Fredkin, Toffoli and Peres gates are 5Δ, 5Δ and 4Δ respectively. The critical path delay is the parameter which has been used in conventional circuits for many years. Some papersin reversible computing [37, 43] have also considered this parameter as the delay of the whole

circuit. In large circuits this parameter is important because it constitutes the actual delay of the circuit.

Table 1 QC of Reversible Gates.

Gate Name	QC
Fredkin Gate	5
Feynman Gate	1
Toffoli Gate	5
Peres Gate	4
BVF Gate	2
Double Feynman Gate	2

4. REVERSIBLE D FLIP FLOP

The D flip flop is a memory cell, capturing the value of the 'D' input at the rising or falling edge of the clock. The proposed reversible D Flip Flop can be used in high-performance data-path applications. This Flip Flop is a dual-edge triggered Flip Flop. Its main advantage is the possibility of obtaining the same throughput with one half of the clock frequency by sampling the input in both rising and falling edge of the clock. Asynchronous set and reset is possible in this flip flop and additionally it is capable of capturing both data and its inverse at the output lines. The four Fredkin gates and four Feynman gates are the required reversible gates for implementing the D flip flop.. See figure 11. Another difference between our work and other reversible flip flops is that the proposed flip flop does not imitate the behavior of conventional flip flop. The Fredkin gate in the right-hand side of the flip flop is used to make the flip flop operate in different modes via controlling signals C_1 and C_2. These modes are the flip flop set and reset as well as the normal mode of the flip flop. Using this reversible gate also makes it possible to have $\overline{\text{output}}$on the other line of the gate at the same time, leaving one garbage output as useful one. Two copies of each input signal, i.e. 'clk' and 'D' are prepared using the first two Feynman gates. Both Fredkin gates-top and bottom- at level 2 from left to right of figure 11 have their required output at the third line of the gate. The first Fredkin gate from top to bottom receives the clock signal while the second Fredkin gate receiving the $\overline{\text{clock}}$. This causes the upper gate be active in the rising edge of the clock with the bottom gate being active in the falling edge of the clock. Therefore this D flip flop samples data in both the falling and rising edge of the clock so its speed is twice the ordinary flip flops which sample an incoming data at only one edge of the clock. The quantum cost of this reversible D flip flop is 24, number of gates is 8 and the number of constant inputs and the garbage outputs are 4 and 7 respectively.

The operation of the control signals is shown in Table 2:

Table 2 D FF control signals.

C1	C2	Operation
0	0	Reset
0	1	Normal Mode of flip flop
1	1	Set

Table 3 Comparative results of D flip flops.

Reversible D flip flop	Quantum Cost	Constant Inputs	Garbage Outputs	No. of Gates	Delay
Proposed Design	24	4	6	8	17
[32]	47	7	8	7	24
[38]	17	2	6	5	17
[40]	13	3	4	5	13

Actually, a valid comparison of our proposed reversible D flip flop with the existing literature is not possible, since there are fundamental differences between our work and that of the others.

In [32] the design of reversible flip flops is carried out using New Gate (NG) [39]. Their flip flop does not have the capability of set and reset and also uses the NG gate which is not the proper choice from the point of quantum cost. THAPLIYAL et al. [40] used Fredkin gate for constructing D flip flop. Also the reversible D flip flop has been designed in [38] by using Fredkin gate and has the same design as of [40], with the exception of eliminating one Feynman gate. In [38] another design of D flip flop with the capability of set/reset was introduced. Compared to [38] our design has the same delay, worse quantum cost and better performance. Dual-edge triggered D flip flop is achieved in our work by sacrificing the quantum cost and gate count. Table 4 shows the result of our work and some previous works in the field. Although except for [38] our proposed design cannot be compared to other works which are not capable of performing set/reset. Although our proposed design and the work of [38] share the set/reset capability, our design is a dual-edge flip flop which can work twice the speed of any other reversible flip flop.

Between these parameters; quantum cost, delay and number of garbage outputs are more important and have higher effects on improving the design.

The following section describes our proposed reversible shift register which may use the proposed D flip flop for storing each bit of information.

5. REVERSIBLE SHIFT REGISTER

Many sequential circuits such as serial adders and multipliers use shift registers to read the inputs and store the intermediate and final results. In this section a reversible equivalent of shift register is introduced and is used to construct our proposed reversible serial adder and the multiplier. Our approach to designing the reversible shift register can be compared to [38]. First, we use the proposed D flip flop with the capability to sample the input at both rising and falling edges of the clock, which is two times faster than the other reversible shift registers including [38]. Secondly, by just eliminating the 'shift left' capability which is not actually required, the proposed reversible shift register has considerably reduced the cost of the circuit including quantum cost and number of gates as seen in figure 12 of the proposed reversible shift register. In this circuit, in order to have a 4-bit shift register, it requires seven 2:1 multiplexers, four D flip flop and four Feynman gates. Except for the first bit which requires just one multiplexer, the other bits come with two multiplexers. Table 4 shows the operating modes of the reversible shift register.

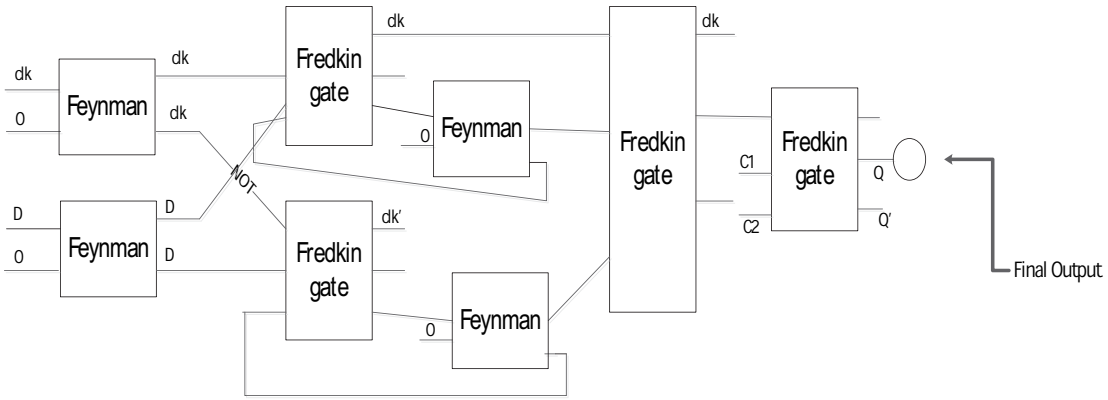

Figure 11 Proposed reversible D flip flop.

Table 4 Controlling signals of the reversible shift register.

S1	S0	Operation
0	0	Load
0	1	previous state
1	0	Shift
1	1	previous state

Referring to Figure 12, if the S_0 is zero, then the input data from left is loaded to the register. So the register works as load, independent of the value of S_1. If the S_1 is 1, the input data is not really important and it just loads the first bit with a new value. It turns out that the next clock signal is available at the output of each flip flop before the next output is affected by that clock. So in the case of shifting, each flip flop receives the correct output from the previous stage. This is the point which helps in reducing the required elements. To show this, we assume that in each flip flop the delay until the last stage Fredkin gate is T_1 where the delay of the flip flop is T. It is clear that $T_1 < T$ and each flip flop receives the clock signal from the previous stage at multiples of T_1; i.e. $n \times T_1$ where n is the flip flop number in the range from one to four. But the shifted data becomes available in each flip flop after $(n-1) \times T_1 + T$ time units and after crossing from the last Fredkin gate . As before n is the flip flop number in the range from one to four. Therefore at each flip flop the clock signal becomes active $T - T_1$ time units earlier before the altered data from the previous stage arrives at the output. This means that each flip flop receives the correct data from the previous stage and shifts it into the next stage.

Table 5 shows the comparative results of our reversible shift register and the one in [38]. But since our proposed design uses a different D flip flop with additional capabilities, it cannot be thoroughly compared with other existing literatures. For example the specified delay is the delay of one-bit shift of the register and our proposed shift register can do twice the shifts in every clock's duration. Also the delay of the multiplexers is not taken into account and we consider the same flip flop in two designs and eliminate it in our evaluation and comparison.

One of the most remarkable characteristics is that our proposed shift register can work in both falling and rising edge of the clock and this property has not led to a larger quantum cost and garbage outputs and has also not led to significant increase in constant inputs and number of gates compared to the existing literature.

Table 5 Comparative results of reversible shift registers without considering the cost of D flip flops.

Reversible shift register	Quantum Cost	Constant Inputs	Garbage Outputs	No. of Gates
Proposed Design	42	7	9	14
[38]	70	10	14	22

Another remarkable point to note is that we used 2×2 reversible multiplexers instead of 4×4 reversible multiplexers. So looking from the perspective of extra elements required for shift register, our proposed shift register uses seven Feynman gates, seven Fredkin gates and four D flip flops, which is a reduction compared to the existing literatures. Considering the fan-out problem, S_1 and S_0 signals can be passed from the previous multiplexer to the next one.

6. REVERSIBLE SERIAL ADDER DESIGN

To complete the construction of the basic elements in sequential reversible circuits, now we turn to basic arithmetic circuits namely adder and multiplier. First we focus on a sequential reversible adder. Until now the entire elements for a serial reversible adder is already available and what is needed is combining the existing structures.

In synchronous sequential circuits, clock signal is required to be applied to entire circuit synchronously. This restriction is due to the assumption that each part of the sequential design has zero internal delay. In reversible design, applying the clock signal synchronously means that we must have fan-out circuits and hence increasing the cost. So it is better to consider the internal delay of each part of the design. Each D flip flop in the shift register, has the clock signal as output, so it can be used for the consecutive D flip flops of the shift register without worrying about the delay introduced in each D flip flop, because the clock signal moves faster than the shifting data.

The proposed reversible sequential 4-bit adder has the elements of conventional sequential adders and the difference is that here the elements of the circuit are all reversible. Figure 13 shows the design of reversible sequential adder. We have

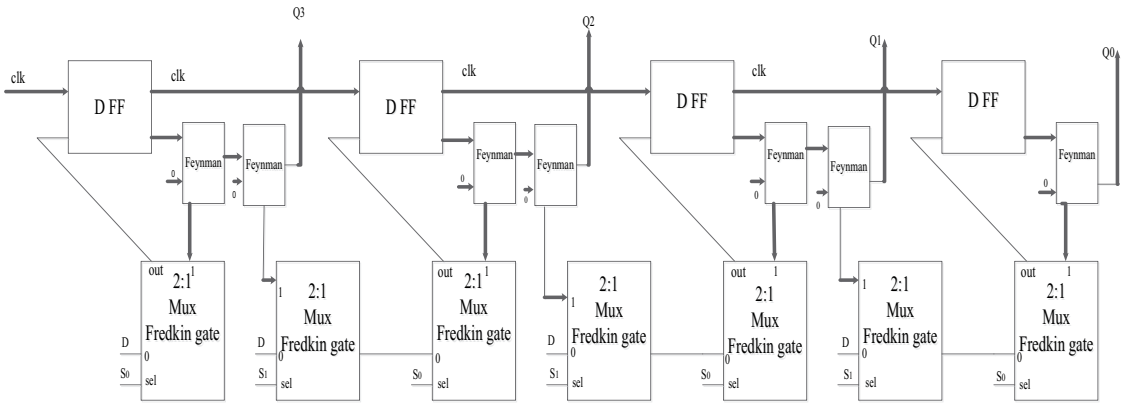

Figure 12 Proposed reversible shift register.

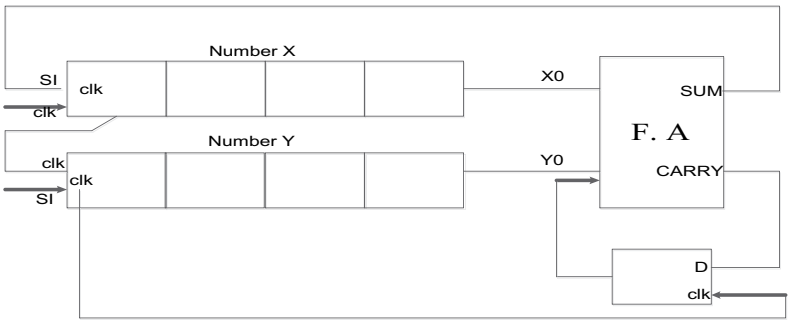

Figure 13 Reversible sequential 4-bit adder.

just described the shift register and D flip flop in the previous sections. The reversible full adder is an HNG gate [19] which receives two bits from the shift registers and the carry bit from the D flip flop just like the conventional serial adder. Except for clock generation and the type of elements used, our reversible serial adder is similar to the one proposed in [29].

7. REVERSIBLE SERIAL MULTIPLIER DESIGN

Sequential multiplication involves looking at the bits of the multiplier one by one and then adding partial products in an accumulative manner. The addition occurs in consecutive clock cycles, with a common register used for the accumulation of partial products which leads to the final result. The shift registers and adder in the proposed design are as introduced in the previous sections.

In this design, we have three registers and an 8-bit adder. The first two registers are 7-bit width registers and include the multiplier and multiplicand numbers respectively. The third register is 8-bit width and its value includes the step by step summation of partial products and at the end of the calculation it consists of the final product result. At the beginning of the operation, the first two registers are filled with the numbers which are to be multiplied and the product register is filled with zero. Controlling the operation of the clock in the circuit is achieved by a one-bit control signal which is zero at first and becomes one when the multiplication is going to start and remains one until the operation is completed. There is a 15 bit Fredkin gate with one control line and 14 data lines and with the same implementation and structure as a 3×3 Fredkin gate. It can be implemented by seven 3×3 Fredkin gates and its quantum cost is 35. If the control signal of Fredkin gate is one, multiplier is directed to the output; otherwise all-zero 7-bit number is directed to the output. The control signal of Fredkin gate is the current value of the right-hand side bit of the multiplicand number. Each clock cycle, shifts the multiplier one bit to the left and enters zero in the right-hand side bit. At the same clock, multiplicand is shifted one bit to the right and bit zero enters the left-hand side of the register. Each clock cycle also loads the product register with the currently calculated sum of the partial products. Therefore after 7 clock cycles the final result is prepared in the product register. See figure 14.

8. CONCLUSIONS

In this article, the basic elements of a reversible, sequential and clocked CPU have been presented. Because of reversible design of these elements, they can be used in low power and nanotechnology-based reversible circuits. Our proposed reversible D flip flop is the only one which can work at both rising and falling edge of the clock and can be used as the memory cell in reversible CPUs. Also we proposed a reversible shift register which has better cost metrics compared to other counterparts and uses 2×2 multiplexers instead of 4×4 multiplexer with almost the same capabilities. We further used the D flip flop and shift register to design a reversible adder and a reversible multiplier which are two mostly used circuits in computer systems.

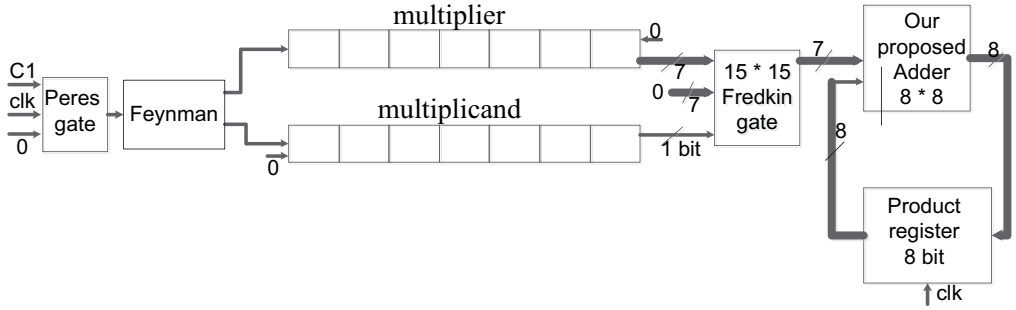

Figure 14 Proposed reversible sequential 4 × 4 multiplier.

The proposed elements can be used for constructing reversible computers containing sequential parts as well as combinational parts.

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