

A 3D analytical modeling of tri-gate tunneling field-effect transistors

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Abstract In this paper, a three-dimensional (3D) analytical solution of the electrostatic potential is derived for the tri-gate tunneling field-effect transistors (TG TFETs) based on the perimeter-weighted-sum approach. The model is derived by separating the device into a symmetric and an asymmetric double-gate (DG) TFETs and then solving the 2D Poisson's equation for these structures. The subthreshold tunneling current expression is extracted by numerical integrating the band-to-band tunneling generation rate over the volume of the device. It is shown that the potential distributions, the electric field profile, and the tunneling current predicted by the analytical model are in close agreement with the 3D device simulation results without the need of fitting parameters. Additionally, the dependence of the tunneling current on the device parameters in terms of the gate oxide thickness, gate dielectric constant, channel length, and applied drain bias is investigated and also demonstrated its agreement with the device simulations.

Keywords Analytical modeling · Three-dimensional (3D) · Perimeter-weighted-sum · Tri-gate (TG) · Tunneling field-effect transistor (TFET)

1 Introduction

Incessant downscaling of the complementary metal oxide semiconductor (CMOS) device is facing critical issues

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including leakage current, short-channel effects (SCEs), and high-power consumption. Tunneling field-effect transistors (TFETs) are now attracting much interest as an alternative to transistor design for future ultralow voltage domain because of their low off-state leakage current (I_{off}) and low subthreshold slope (SS). Since the current is controlled by the band-to-band tunneling (BTBT) mechanism on the source-channel interface, TFETs can achieve the subthreshold slope of less than 60 mV/decade at room temperature, which allows for a more aggressive reduction of the threshold and supply voltages [1–7]. However, planar silicon-based TFETs have very low on-state currents (I_{on}) compared to conventional MOSFETs (typically three to five decades) because of poor band-to-band tunneling efficiency, which is a serious drawback in circuit applications. In order to improve the TFET on-state currents, several techniques have been adopted including heterostructures [4, 8], band-gap engineering [9, 10], low band gap and high mobility materials [11], gate engineering [12, 13], vertical direction tunneling [14], extended source [15–17], and source-pocket doping (p–n–p–n) [18, 19].

In order to improve the gate control over the channel, Intel has developed tri-gate (TG) device structures [20]. Tri-gate transistors provide a dramatic combination of high-power efficiency and improved performance. In particular, attention is focused on TG MOSFETs because of their high current drive capability, lower leakage current, steep subthreshold slope, high on–off-current ratio, low body-effect coefficient, and improved short-channel effects as reported in the literature [20–25]. Although there have been reports on the design, optimization, and physical simulations of the three-dimensional (3D) TG TFET structures for better performance in terms of the on-state current, subthreshold slope, and short-channel effects [26–29], their 3D analytical modeling has been seldom reported.

In this paper, we have developed a 3D analytical model for the electrostatic potential distribution along the channel of the tri-gate TFETs. The electrostatic potential model is developed by solving the 2D Poisson’s equation using a perimeter-weighted-sum approach of symmetric and asymmetric double-gate (DG) TFETs. The numerical integration of the band-to-band tunneling generation rate is used to extract the subthreshold drain current. The proposed model is validated against 3D device simulation results calibrated with experimental results. The model also predicts the impacts of structural parameters without the need of fitting parameters. This feature is useful to provide a design insight of the tri-gate TFETs.

The paper is organized as follows: Sect. 2 describes the device structures, simulation, and calibration of the tri-gate TFET model. In Sect. 3, the potential profile and electric field components are derived by separating the device into a symmetric and an asymmetric double-gate (DG) TFETs. Furthermore, a semi-analytical expression for the tunneling current is extracted by integrating the BTBT generation rate. The results, discussion, and validation of the model are presented in Sect. 4. Finally, the conclusion is drawn.

2 Device structure, simulation and calibration of the TFET model

A 3D schematic view of the device structure for a tri-gate TFET is shown in Fig. 1a. The 3D-simulated TG TFET has a channel length (L) of 30 nm, silicon body thickness (t_{si}) of 10 nm, and channel width (W) of 10 nm. The gate electrode covers the top surface and two sidewalls of the

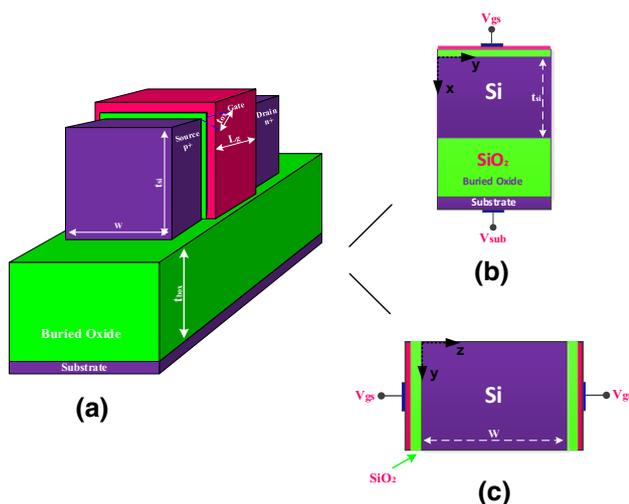


Fig. 1 a 3D schematic view of a tri-gate TFET. The device can be equivalently composed of ASDG TFET with width of t_s as shown in b and SDG TFET with width of W as shown in c

silicon body with a gate oxide thickness (t_{ox}) and buried oxide thickness (t_{box}). Its gate oxide and buried oxide thicknesses are 1 and 100 nm, respectively. Aluminum is used to form the gate electrode with work function of 4.2 eV and SiO₂ is applied to the gate insulator with permittivity (ϵ_{ox}) of $3.9\epsilon_0$. The device doping concentrations are as follows: source doping concentration $N_A = 1 \times 10^{20} \text{cm}^{-3}$, drain doping concentration $N_d = 1 \times 10^{19} \text{cm}^{-3}$, and channel doping concentration $N_A = 1 \times 10^{17} \text{cm}^{-3}$. The source and drain junctions doping profiles are assumed to be abrupt.

Three-dimensional device simulations are done using the 3D Silvaco ATLAS device simulator [30]. Kane’s tunneling model was used for all simulations and the parameters of this model were calibrated with experimentally measured results reported by Tura *et al.* [31]. The parameters values for the Kane’s model are $A = 4 \times 10^{19} \text{eV}^{1/2}/\text{cm} - \text{s} - \text{V}^2$ and $B = 41 \text{ MV}/\text{cm} - \text{eV}^{3/2}$. The Auger recombination, band-gap narrowing, and Hurkx and Shockley–Read–Hall (SRH) recombination models were also included to describe the recombination, generation and carriers’ lifetimes in the highly doped regions. Meanwhile, the concentration and field-dependent mobility models and trap-assisted tunneling models were also used [5, 7, 16].

The energy band diagram along the horizontal direction at 1 nm away from the oxide–silicon interface and $z = W/2$ is plotted in Fig. 2 for the off-state ($V_g = 0 \text{ V}$ and $V_d = 0.01 \text{ V}$) and the on-state ($V_g = 0.7 \text{ V}$ and $V_d = 0.01 \text{ V}$) of 30-nm channel length tri-gate TFET. As seen, the source valence band is located below the channel conduction band under the off-state condition. Therefore, the probability of the tunneling of electrons from source to drain is very low and the small off-current flows in structure because of the large tunneling barrier between the source and channel. By looking at the energy band diagram for on-state, the channel conduction band goes below the source valence

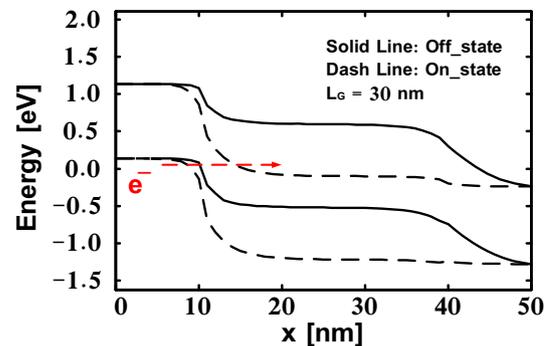


Fig. 2 The energy band diagrams of 30-nm channel length tri-gate TFET along the horizontal direction at 1 nm away from the oxide–silicon interface and $z = W/2$

band and the band-pass window is created due to applied positive gate voltage. This band-pass window causes the electrons tunnel from the occupied valence band states of the source to the unoccupied conduction band states of the channel. Consequently, the on-current increases as compared with the off-current because of the narrow tunneling barrier between the source and the channel. More details of the working principles of TFET can be found in the literature [1–3].

3 Model formulation

3.1 3D poisson's equation solution

In order to develop a model for the tri-gate TFET, the potential distribution throughout the silicon body must be accurately determined by solving the 3D Poisson's equation with the appropriate boundary conditions. Recently, to avoid solving for the 3D Poisson's equation that is too difficult to be derived, the 3D potential distribution in TG MOSFETs have been modeled by considering it to be a combination of two independent devices including a symmetric double-gate (SDG) MOSFET and an asymmetric double-gate (ASDG) MOSFET, which results in a good agreement between the numerical solution and analytical expressions [32–35]. In this way, the resulting analytical potential for the TG devices can be obtained as the perimeter-weighted sum of the analytical potential for the SDG and ASDG devices. The coupling effects between two DG MOSFETs can be ignored by the restrictions required to obtain operational TG devices that $L/W > 2$, $L/t_{si} > 2$ and $t_{box} \geq L$ [34,35]. Consequently, following the same notion of perimeter-weighted, we consider that the tri-gate TFET device consists of two independent DG TFET, an asymmetric and a symmetric one as shown in Fig. 1b, c, respectively.

On the other hand, quantum mechanical effects including quantization of energy and reduction of the electron density of states appeared in narrow channels with a silicon body thickness is < 10 nm [36–39]. Therefore, these effects can be ignored in our study because a silicon body thickness of 10 nm is used, as in other simulation-based TFET studies [16,40–45].

According to the Poisson's equation, the channel potential distribution of silicon body $\varphi(x, y)$ into ASDG TFET can be calculated as

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}}, \quad (1)$$

where q is the magnitude of electron charge (positive) and N_A and ϵ_{si} are the channel uniform doping concentration and permittivity of silicon, respectively. The x -axis is vertical to the channel thickness and the y -axis presents the channel length.

The 2D channel potential function can be approximated as the parabolic along the x -axis and expressed as

$$\varphi(x, y) = c_0(y) + c_1(y)x + c_2(y)x^2, \quad (2)$$

where the coefficients c_0 , c_1 , and c_2 are arbitrary function of y which are obtained by applying the boundary condition for the Poisson's equation. By assuming vertical electric fields at the gate oxides, the electric fluxes are continuous at the interface of silicon-gate oxide and silicon-buried oxide as

$$\frac{\partial \varphi(x, y)}{\partial x} \Big|_{x=0} = -\frac{\epsilon_{ox}}{\epsilon_{si}} \times \frac{V_g - V_{fb,t} - \varphi(0, y)}{t_{ox}} \quad (3)$$

$$\frac{\partial \varphi(x, y)}{\partial x} \Big|_{x=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \times \frac{V_{sub} - V_{fb,b} - \varphi(t_{si}, y)}{t_{box}}, \quad (4)$$

where V_g is the top gate bias; V_{sub} is the substrate bias; ϵ_{si} and ϵ_{ox} are permittivity of silicon and oxide, respectively; t_{ox} and t_{box} are gate oxide and buried oxide thicknesses, respectively. $V_{fb,t}$ and $V_{fb,b}$ are the flat-band voltages of top and bottom gate, respectively, and given as the difference between gate material work function and silicon work function, which are given by

$$V_{fb} = \phi_M - \phi_{si}, \quad (5)$$

where ϕ_{si} is the silicon work function and can be written as

$$\phi_{si} = \chi_{si} + \frac{E_g}{2q} - \phi_B, \quad (6)$$

where χ_{si} is the electron affinity of silicon, E_g is the energy band gap of the silicon, ϕ_B is the Fermi potential ($\phi_B = V \times \ln(N_A/n_i)$) with V as the thermal voltage; and N_A and n_i as the channel doping concentration and intrinsic carrier concentration, respectively.

The coefficients c_0 , c_1 , c_2 , and $\varphi(t_{si}, y)$ can be obtained by solving the system of Eqs. (2)–(4). Substituting the c_i coefficients and $\varphi(t_{si}, y)$ into Eq. (2), we obtain a second-order differential equation for the surface potential as

$$\frac{\partial^2 \varphi(0, y)}{\partial y^2} + \alpha \varphi(0, y) = \beta, \quad (7)$$

where

$$\alpha = \frac{\epsilon_{ox} [\epsilon_{ox} t_{si} + \epsilon_{si} (t_{ox} + t_{box})]}{\epsilon_{si} t_{si} t_{ox} (\epsilon_{ox} t_{si} + \epsilon_{si} t_{box})} \tag{8}$$

$$\beta = \frac{2\epsilon_{si}\epsilon_{ox} [t_{ox} (V_{sub} - V_{fb,b}) + t_{box} (V_g - V_{fb,t})] + 2\epsilon_{ox}^2 t_{si} (V_g - V_{fb,t}) - qN_A t_{si} t_{ox} (2\epsilon_{si} t_{box} + \epsilon_{ox} t_{si})}{2\epsilon_{si} t_{si} t_{ox} (\epsilon_{ox} t_{si} + \epsilon_{si} t_{box})} \tag{9}$$

The potential distribution at the top gate interface $\varphi(0, y)$ can be found by solving Eq. (7) with boundary conditions at the source and drain ends as follows:

$$\varphi(x, y) \Big|_{y=0} = V_{bi,p} \tag{10}$$

$$\varphi(x, y) \Big|_{y=t_{si}} = V_d + V_{bi,n}, \tag{11}$$

where V_d is the drain bias and $V_{bi,p}$ and $V_{bi,n}$ are built-in potentials at the source–channel and channel–drain interfaces, respectively. Values of $V_{bi,p}$ and $V_{bi,n}$ are $V_{bi,p} = -V_T \times \ln(N_{A,s}/N_A)$ and $V_{bi,n} = V_T \times \ln(N_{D,d} \times N_A/n_i^2)$,

boundary conditions given by Eqs. (10) and (11), and then replacing n with t_{si}/x , we get the channel potential distribution of ASDG TFET $\varphi_{AS}(x, y)$ as

$$\varphi_{AS}(x, y) = \frac{1}{e^{\frac{2L}{\lambda_{AS}}} - 1} \times \left[(V_{bi,p} - \gamma_{AS}) \left(e^{\frac{2L-y}{\lambda_{AS}}} - e^{\frac{y}{\lambda_{AS}}} \right) + (V_d + V_{bi,n} - \gamma_{AS}) \left(e^{\frac{L+y}{\lambda_{AS}}} - e^{\frac{L-y}{\lambda_{AS}}} \right) \right] + \gamma_{AS} \tag{13}$$

where

$$\lambda_{AS} = \sqrt{\frac{\epsilon_{si} t_{si} t_{ox}}{2\epsilon_{ox}} \times \left(1 + \frac{\epsilon_{ox} x}{\epsilon_{si} t_{ox}} \right) \left(\frac{\epsilon_{ox} t_{si} + 2\epsilon_{si} t_{box}}{\epsilon_{ox} t_{si} + \epsilon_{si} (t_{ox} + t_{box})} \right) - \frac{x^2}{2}} \tag{14}$$

$$\gamma_{AS} = \frac{2\epsilon_{si}^2 \epsilon_{ox} [t_{ox} (V_{sub} - V_{fb,b}) + t_{box} (V_g - V_{fb,t})] + 2\epsilon_{si} \epsilon_{ox}^2 [t_{si} (V_g - V_{fb,t}) + x (V_{sub} - V_g + V_{fb,t} - V_{fb,b})]}{2\epsilon_{si} \epsilon_{ox} [\epsilon_{ox} t_{si} + \epsilon_{si} (t_{ox} + t_{box})]} - \frac{qN_A \{ \epsilon_{si} \epsilon_{ox} [t_{box} x (2t_{si} - x) + t_{ox} (t_{si}^2 - x^2)] + \epsilon_{ox}^2 t_{si} x (t_{si} - x) + 2\epsilon_{si}^2 t_{si} t_{ox} t_{box} \}}{2\epsilon_{si} \epsilon_{ox} [\epsilon_{ox} t_{si} + \epsilon_{si} (t_{ox} + t_{box})]} \tag{15}$$

with $N_{A,s}$, $N_{D,d}$, and N_A as the doping concentrations of the source, drain, and channel, respectively; n_i as the intrinsic carrier concentration and V_T as the thermal voltage.

By applying the above boundary conditions into Eq. (7), we get

$$\varphi(0, y) = \frac{1}{e^{2\sqrt{\alpha}L} - 1} \times \left[\left(V_{bi,p} - \frac{\beta}{\alpha} \right) \left(e^{\sqrt{\alpha}(2L-y)} - e^{\sqrt{\alpha}y} \right) + \left(V_d + V_{bi,n} - \frac{\beta}{\alpha} \right) \left(e^{\sqrt{\alpha}(L+y)} - e^{\sqrt{\alpha}(L-y)} \right) \right] + \frac{\beta}{\alpha} \tag{12}$$

The potential distribution at the top gate interface can be described by Eq. (12) but we need the potential distribution within the channel at different depths x from the top gate interface. In order to achieve a relation between the potential distribution within the whole channel and potential distribution at the front gate interface $\varphi(0, y)$, at first, we replace x with t_{si}/n ($n \neq 0, \dots$) in Eq. (2). By substituting the obtained relation into Eq. (1), solving the differential equation with the

An analytical expression for the potential distribution of SDG TFET $\varphi_S(y, z)$ is extracted from the potential distribution expression of ASDG TFET $\varphi_{AS}(x, y)$ by replacing x , t_{si} , t_{box} and V_{sub} with z , W , t_{ox} , and V_g [46], which can be as Eqs. (16)–(18) below:

$$\varphi_S(y, z) = \frac{1}{e^{\frac{2L}{\lambda_S}} - 1} \times \left[(V_{bi,p} - \gamma_S) \left(e^{\frac{2L-y}{\lambda_S}} - e^{\frac{y}{\lambda_S}} \right) + (V_d + V_{bi,n} - \gamma_S) \left(e^{\frac{L+y}{\lambda_S}} - e^{\frac{L-y}{\lambda_S}} \right) \right] + \gamma_S \tag{16}$$

where

$$\lambda_S = \sqrt{\frac{\epsilon_{si} t_{ox} W}{2\epsilon_{ox}} \times \left[1 + \left(\frac{\epsilon_{ox} z}{\epsilon_{si} t_{ox}} \right) \left(1 - \frac{z}{W} \right) \right]} \tag{17}$$

$$\gamma_S = V_g - V_{fb,t} - \frac{qN_A [\epsilon_{si} t_{ox} W + \epsilon_{ox} z (W - z)]}{2\epsilon_{si} \epsilon_{ox}} \tag{18}$$

By using the perimeter-weighted-sum method [32, 46], the 3D analytical potential distribution along the channel of the

TG TFETs can be derived as the perimeter-weighted sum of the analytical potential distributions of SDG and ASDG devices. Accordingly, the 3D analytical potential distribution $\varphi(x, y, z)$ for the tri-gate TFET device can be defined by

$$\varphi(x, y, z) = \alpha_S \times \varphi_S(y, z) + (1 - \alpha_S) \times \varphi_{AS}(x, y) \quad (19)$$

with

$$\gamma'_{AS} = \frac{2qN_A \varepsilon_{si}(t_{ox}x + t_{box}(x - t_{si})) + \varepsilon_{ox}(qN_A t_{si}(2x - t_{si}) + 2\varepsilon_{si}(V_{sub} - V_g + V_{fb,t} - V_{fb,b}))}{2\varepsilon_{si}[\varepsilon_{ox}t_{si} + \varepsilon_{si}(t_{ox} + t_{box})]} \quad (23)$$

$$\alpha_S = \frac{2t_{si}}{W + 2t_{si}}, \quad (20)$$

where α_S is the ratio of SDG TFET to the entire TG TFET. Its value is 1 and 0 for pure SDG and ASDG TFET, respectively. For TG TFETs, one obtains $0 < \alpha_S < 1$.

It must be noted that, when replacing the TG device with the equivalent asymmetric and symmetric DG structures, the physical lengths of the DG devices must be reduced by the square root of 2 [22].

3.2 Tunneling current derivation

At first, the electric field components are found by differentiating the electrostatic potential expression as

$$\begin{aligned} E_x(x, y, z) &= -\frac{\partial \varphi(x, y, z)}{\partial x} = -\gamma'_{AS}(1 - \alpha_S) \left(1 - \cosh\left(\frac{L - 2y}{2\lambda_{AS}}\right) \operatorname{sech}\left(\frac{L}{2\lambda_{AS}}\right) \right) \\ &+ \frac{4\lambda'_{AS}(1 - \alpha_S) e^{\frac{2L}{\lambda_{AS}}}(V_d + V_{bi,n} - \gamma_{AS}) \left[y \cosh\left(\frac{y}{\lambda_{AS}}\right) \sinh\left(\frac{L}{\lambda_{AS}}\right) - L \cosh\left(\frac{L}{\lambda_{AS}}\right) \sinh\left(\frac{y}{\lambda_{AS}}\right) \right]}{\lambda_{AS}^2 \left(e^{\frac{2L}{\lambda_{AS}}} - 1 \right)^2} \\ &+ \frac{2\lambda'_{AS}(1 - \alpha_S) e^{\frac{2L}{\lambda_{AS}}}(V_{bi,p} - \gamma_{AS}) \left[y \cosh\left(\frac{y}{\lambda_{AS}}\right) \sinh\left(\frac{2L}{\lambda_{AS}}\right) + (y - 2L) \sinh\left(\frac{y}{\lambda_{AS}}\right) + y \cosh\left(\frac{2L}{\lambda_{AS}}\right) \sinh\left(\frac{y}{\lambda_{AS}}\right) \right]}{\lambda_{AS}^2 \left(e^{\frac{2L}{\lambda_{AS}}} - 1 \right)^2} \end{aligned} \quad (21)$$

where

$$\lambda'_{AS} = \frac{\frac{t_{si}(\varepsilon_{ox}t_{si} + 2\varepsilon_{si}t_{box})}{2(\varepsilon_{ox}t_{si} + \varepsilon_{si}(t_{ox} + t_{box}))} - x}{\sqrt{2 \left(\frac{t_{si}(\varepsilon_{si}t_{ox} + \varepsilon_{ox}x)(\varepsilon_{ox}t_{si} + 2\varepsilon_{si}t_{box})}{\varepsilon_{ox}(\varepsilon_{ox}t_{si} + \varepsilon_{si}(t_{ox} + t_{box}))} - x^2 \right)}} \quad (22)$$

$$\begin{aligned} E_y(x, y, z) &= -\frac{\partial \varphi(x, y, z)}{\partial y} \\ &= -\frac{\alpha_S}{\lambda_S} \left[\left(V_d + V_{bi,n} - \gamma_S + \cosh\left(\frac{L}{\lambda_S}\right)(V_{bi,p} - \gamma_S) \right) \right. \\ &\quad \times \left. \left(\cosh\left(\frac{y}{\lambda_S}\right) \operatorname{csch}\left(\frac{L}{\lambda_S}\right) + \sinh\left(\frac{y}{\lambda_S}\right)(V_{bi,p} - \gamma_S) \right) \right] \\ &\quad - \frac{1 - \alpha_S}{\lambda_{AS}} \left[\left(V_d + V_{bi,n} - \gamma_{AS} + \cosh\left(\frac{L}{\lambda_{AS}}\right)(V_{bi,p} - \gamma_{AS}) \right) \right. \\ &\quad \times \left. \left(\cosh\left(\frac{y}{\lambda_{AS}}\right) \operatorname{csch}\left(\frac{L}{\lambda_{AS}}\right) \right) + \sinh\left(\frac{y}{\lambda_{AS}}\right)(V_{bi,p} - \gamma_{AS}) \right] \end{aligned} \quad (24)$$

$$\begin{aligned}
 E_z(x, y, z) = & -\frac{\partial\varphi(x, y, z)}{\partial z} = -\alpha_S\gamma'S \left(1 - \cosh\left(\frac{L-2y}{2\lambda_S}\right) \operatorname{sech}\left(\frac{L}{2\lambda_S}\right)\right) \\
 & + \frac{4\alpha_S\lambda'_{AS}e^{\frac{2L}{\lambda_S}}(V_d + V_{bi,n} - \gamma_S) \left[y \cosh\left(\frac{y}{\lambda_S}\right) \sinh\left(\frac{L}{\lambda_S}\right) - L \cosh\left(\frac{L}{\lambda_S}\right) \sinh\left(\frac{y}{\lambda_S}\right) \right]}{\lambda_S^2 \left(e^{\frac{2L}{\lambda_S}} - 1\right)^2} \\
 & + \frac{2\alpha_S\lambda'_{AS}e^{\frac{2L}{\lambda_S}}(V_{bi,p} - \gamma_S) \left[y \cosh\left(\frac{y}{\lambda_S}\right) \sinh\left(\frac{2L}{\lambda_S}\right) + (y - 2L) \sinh\left(\frac{y}{\lambda_S}\right) + y \cosh\left(\frac{2L}{\lambda_S}\right) \sinh\left(\frac{y}{\lambda_S}\right) \right]}{\lambda_S^2 \left(e^{\frac{2L}{\lambda_S}} - 1\right)^2}
 \end{aligned} \tag{25}$$

where

$$\lambda'_S = \frac{W - 2z}{2\sqrt{2z(W - z) + \frac{2\varepsilon_{si}t_{ox}W}{\varepsilon_{ox}}}} \tag{26}$$

$$\gamma'S = -\frac{qN_A(W - 2z)}{2\varepsilon_{si}}. \tag{27}$$

The electric field components so obtained are then used to derive the total electric field E_T at the tunneling junction as

$$|E_T| = \sqrt{E_x^2 + E_y^2 + E_z^2}. \tag{28}$$

Knowing the electric field, the BTBT generation rate, expressed in terms of the number of carriers tunneling from the valence band of the source to the conduction band of the channel per unit volume per unit time (G_{BTBT}), can be calculated using Kane’s tunneling model as [45,47]:

$$G_{BTBT} = A \frac{|E_T|^{2.5}}{\sqrt{E_g}} \exp\left(-B \frac{E_g^{3/2}}{|E_T|}\right) \tag{29}$$

where E_g is the energy band gap and A and B are material-dependent parameters of Kane’s model. The values of these parameters depend on the hole and electron effective masses, which can be as below [30]:

$$A = \frac{q^2\sqrt{2m_{\text{tunnel}}}}{h^2\sqrt{E_g}} \tag{30}$$

$$B = \frac{\pi^2 E_g^{3/2} \sqrt{m_{\text{tunnel}}/2}}{qh} \tag{31}$$

with

$$m_{\text{tunnel}} = \frac{m_0 m_e m_h}{m_e + m_h} \tag{32}$$

where m_0 , m_e , and m_h are the rest mass of an electron, electron, and hole effective masses, respectively.

Finally, the tunneling current can be computed by integrating the BTBT generation rate on the volume of the device:

$$I_{BTBT} = q \int G_{BTBT} dV, \tag{33}$$

where dV is an elementary volume in the device.

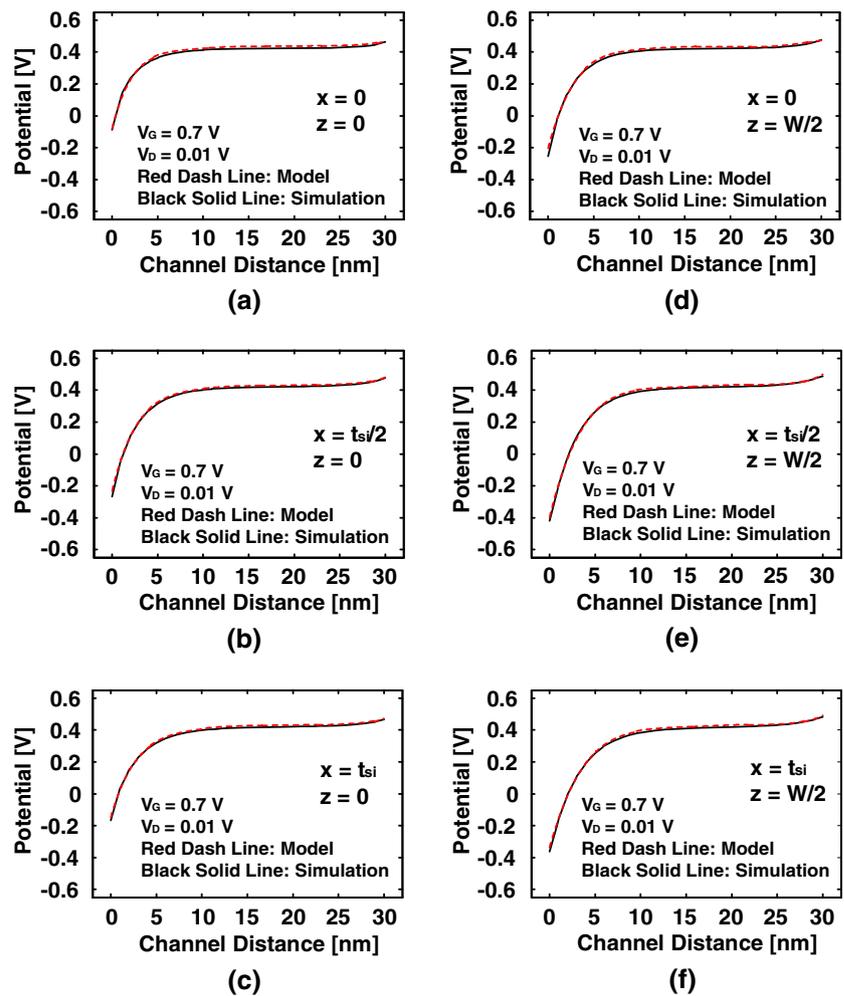
4 Model validation, results and discussion

The proposed model for the potential distributions, electric field profile, and tunneling current is verified by using the 3D numerical simulations in this section. Figure 3a–f compares the 3D potential distributions calculated from the analytical solution, Eq. (19), with numerical simulations for the tri-gate TFET as a function of the channel length position (y – axis) for different x and z positions. Two cut-lines, along the edge and middle of the channel at different x positions, are used for this purpose. It is obviously seen that a close agreement for the 3D potential distribution between the analytical model and device simulator is obtained without the need of fitting parameters. Similarly, Fig. 4a–f compares the electric field profile given by our model with 3D numerical simulations for the tri-gate TFET as a function of channel length position (y – axis) for different x and z positions. A good agreement between the model results with those simulated using the device simulator is obtained.

Figure 5 shows the subthreshold $I_{ds} - V_g$ characteristic of a tri-gate TFET with L of 30 nm, t_{ox} of 1 nm, and ε_{ox} of $3.9\varepsilon_0$ at $V_d = 0.01$ V as calculated by the model and simulations in linear and logarithm scales. It can be observed that our model well captures the subthreshold tunneling current.

In addition, we analyze the dependence of the subthreshold tunneling current on design and operation parameters including gate oxide thickness, gate dielectric constants,

Fig. 3 Modeling (red dash line) and device simulation (black solid line) values of the 3D analytical potential distribution $\varphi(x, y, z)$ for the tri-gate TFET device with L of 30 nm and t_{ox} of 1 nm biased at $V_g = 0.7$ V and $V_d = 0.01$ V and its variation with the channel length position (y – axis) for the different channel locations. **a** $x = 0$, $z = 0$; **b** $x = t_{si}/2$, $z = 0$; **c** $x = t_{si}$, $z = 0$; **d** $x = 0$, $z = W/2$; **e** $x = t_{si}/2$, $z = W/2$; and **f** $x = t_{si}$, $z = W/2$



channel length, and applied drain bias. Figure 6 shows the dependence of the subthreshold tunneling current on the gate voltage for different values of t_{ox} . Scaling the gate dielectric has the effective impact on the device performance of the TFET because the tunneling current increases exponentially with decreasing gate oxide thickness [40]. As t_{ox} is scaled from 3 to 1 nm, the tunneling current increases more than one order of magnitude at high voltages. Figure 7 shows the impact of varying gate dielectric constant on the transfer characteristics of a tri-gate TFET with L of 30 nm and t_{ox} of 1 nm biased at $V_d = 0.01$ V. Three different values of gate dielectric constant, 3.9, 7.5, and $21\epsilon_0$, are used for this purpose. The higher tunneling current is achieved with increasing ϵ_{ox} because there is a linear scaling of $\log(I_{ds})$ with $\epsilon_{ox}^{-0.5}$ [40, 48]. In addition to improved tunneling current as the result of the better gate coupling given by a high- κ dielectric, the average subthreshold slope decreases because the threshold voltage falls on a steeper part of the transfer curves [48]. As seen from Figs. 6 and 7, our model well predicts the changes of subthreshold $I_{ds} - V_g$ characteristic induced by varying t_{ox} and ϵ_{ox} .

Figure 8 shows the transfer curves of a tri-gate TFET for four different values of channel length as 15, 30, 50, and 90 nm with constant t_{ox} of 1 nm and ϵ_{ox} of $3.9\epsilon_0$ at $V_d = 0.01$ V. The impact of scaling the channel length on the transfer curves is negligible because effective tunneling width is constant with varying channel length [5, 16, 49]. The variation of the subthreshold $I_{ds} - V_g$ characteristic with channel length shows good agreement with the numerical results for a tri-gate TFET, confirming the accuracy of our model.

Figure 9 shows the subthreshold tunneling current as a function of drain voltage for a tri-gate TFET with L of 30 nm, t_{ox} of 1 nm, and ϵ_{ox} of $3.9\epsilon_0$. As seen, the modeled and simulated subthreshold $I_{ds} - V_g$ characteristics are in qualitative agreement. As expected, the deviation between the model and the simulation increases at high V_d as the gate voltage increases. This is due to the exclusion of mobile charge density. Because the mobile charges prevent the further increase band bending at high gate voltages by pinning the channel potential to the drain potential. Therefore, the modeled $I_{ds} - V_g$ characteristic increases with higher rate when com-

Fig. 4 Comparison of modeling (red dash line) and device simulation (black solid line) values of the 3D electric field profile $E(x, y, z)$ for the tri-gate TFET device with L of 30 nm and t_{ox} of 1 nm as a function of the channel length position for the different x and z positions. **a** $x = 0, z = 0$; **b** $x = t_{si}/2, z = 0$; **c** $x = t_{si}, z = 0$; **d** $x = 0, z = W/2$; **e** $x = t_{si}/2, z = W/2$; and **f** $x = t_{si}, z = W/2$. The gate voltage is 0.7 V and the drain voltage is 0.01 V

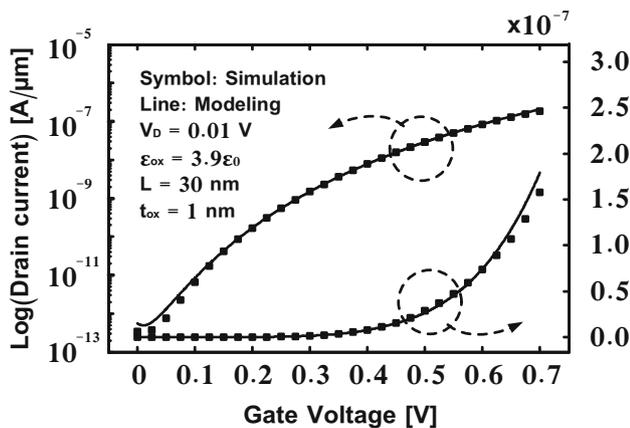
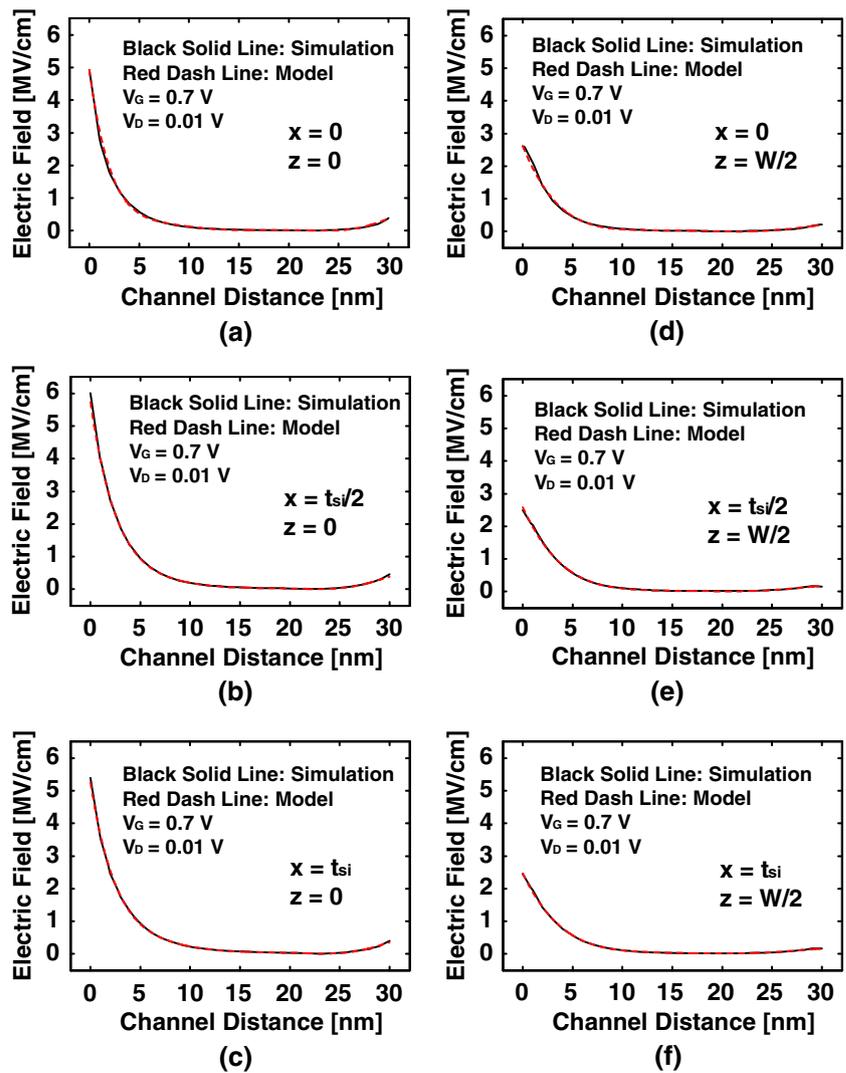


Fig. 5 Modeling (solid line) and device simulation (symbol) of the sub-threshold $I_{ds} - V_g$ characteristic of a tri-gate TFET with L of 30 nm, t_{ox} of 1 nm and ϵ_{ox} of $3.9\epsilon_0$ at $V_d = 0.01$ V in linear (right) and logarithm (left) scales

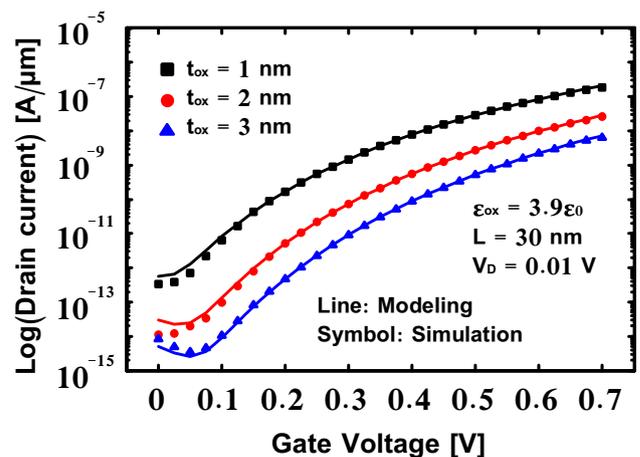


Fig. 6 The transfer characteristics of a tri-gate TFET in logarithm scale for three different values of t_{ox} as 1, 2, and 3 nm with L of 30 nm and ϵ_{ox} of $3.9\epsilon_0$ biased at $V_d = 0.01$ V. The solid lines represent the calculated results from model, and the symbols the simulation results

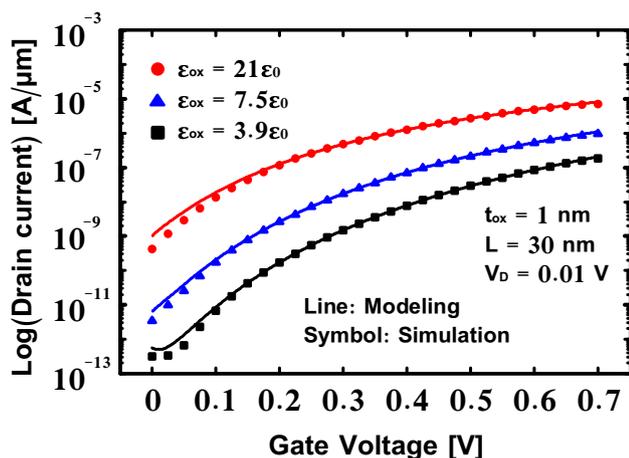


Fig. 7 The dependence of subthreshold tunneling current on the gate voltage for different values of gate dielectric constant for a tri-gate TFET with L of 30 nm and t_{ox} of 1 nm. The drain voltage is 0.01 V. The symbols correspond to the simulated results, and the lines to the calculated results from model

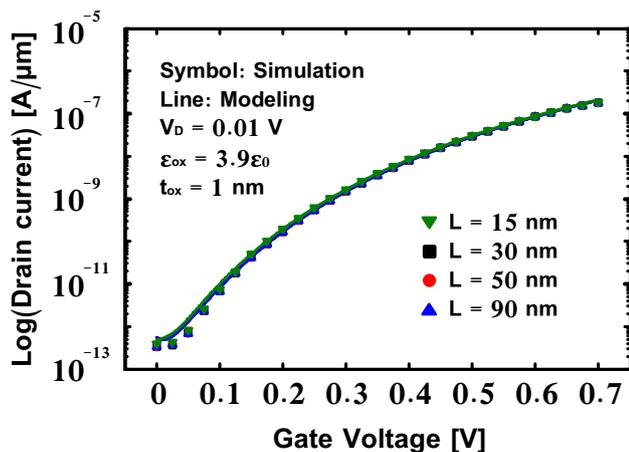


Fig. 8 The transfer characteristics of a tri-gate TFET for various channel lengths as 15, 30, 50, and 90 nm with constant t_{ox} of 1 nm and ϵ_{ox} of $3.9\epsilon_0$ at $V_d = 0.01$ V. The modeling and simulation results are represented by the lines and symbols, respectively

pared with the simulation results at high V_g , as reported in previous works [50,51].

5 Conclusions

A 3D analytical model for TG TFETs has been developed using a perimeter-weighted-sum approach. In this way, the resulting analytical potential for the TG TFETs has been obtained as the perimeter-weighted sum of the analytical potential for the SDG and ASDG TFETs. The semi-analytical expression of the subthreshold tunneling current is extracted by integrating the BTBT generation rate over the volume of the device and compared with 3D device simulation results.

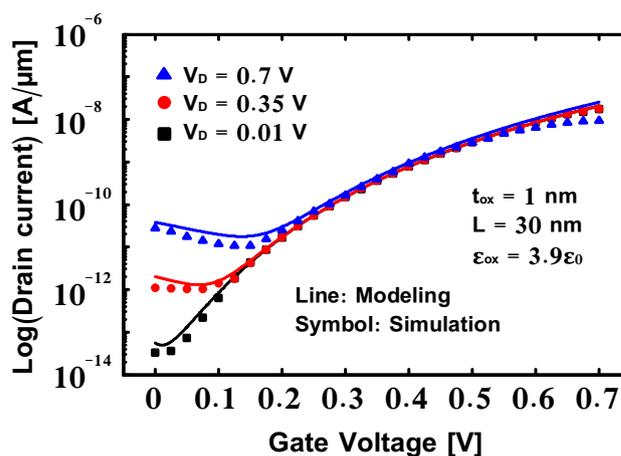


Fig. 9 The subthreshold tunneling current variation with the gate voltage at different drain bias for a tri-gate TFET with L of 30 nm, t_{ox} of 1 nm and ϵ_{ox} of $3.9\epsilon_0$. The symbols correspond to the simulated results, and the lines to the calculated results from model

This model takes into account the influences of all the device geometry parameters including gate oxide thickness, gate dielectric constants, channel length, and applied drain bias and predicts well the effects of them without the need of the fitting parameters. Comparing the model results for different electrical parameters, i.e., the potential distributions, electric field profile, and tunneling current, with the 3D simulation results shows a good agreement.

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