Deadbeat Control of the Stand-Alone Four-Leg Inverter Considering the Effect of the Neutral Line Inductor

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***Abstract*—Distributed generation (DG) has been considered as an alternative source of power generation, especially in stand-alone applications, where both single- and three-phase loads must be supplied with fixed amplitude and frequency sinusoidal voltages. Therefore, the presence of the neutral wire is inevitable. A four-leg inverter is a common solution to connect DGs to stand-alone loads as well as providing the neutral wire. In this paper, by considering a filter inductor in the fourth (neutral) leg of the four-leg inverter, a detailed model is presented, which illustrates a strong coupling among different phases. In order to remove this coupling effect, it is proposed to transform the quantities from the *abc* to the $\alpha\beta\gamma$ reference frame. Furthermore, based on the proposed decoupled model, a new deadbeat control scheme is proposed to provide balanced sinusoidal voltages at the output of the inverter. To confirm the effectiveness of the proposed modeling and control techniques, experimental results on a 3-kW setup with the digital-signal-processor-based digital controller are provided under various loading conditions, such as linear/nonlinear, balanced/unbalanced, and single-/three-phase loads.**

***Index Terms*—Deadbeat (DB) control, four-leg inverter, stand alone.**

I. Introduction

NOWADAYS, distributed generation (DG) has attracted much attention due to various advantages, especially for powering remote loads. Most DGs provide electrical power in dc (e.g., fuel cells) or ac with variable frequency (e.g., wind turbines). Therefore, to supply loads with sinusoidal voltages with already defined amplitude and frequency, an interface power electronic converter is necessary [1]–[3].

Stand-alone systems usually supply a various combination of balanced/unbalanced, linear/nonlinear, single-/three-phase loads, simultaneously. Under any loading condition, the voltage of the loads must be controlled precisely to have a fixed amplitude and frequency, especially when feeding highly unbalanced loads. Consequently, the neutral wire must be available for these systems. In addition, the control system should guarantee sinusoidal voltages, with minimum harmonic distortions, especially under nonlinear loading conditions, in accordance to the harmonic limit standards like IEC62040-3 and IEEE 1547 for uninterruptible power supplies (UPSs).

If isolation is necessary for the interface inverter, then adding a transformer with the star or zig-zag secondary connection, at the output of a conventional three-phase three-leg voltage source inverter (VSI) is the simplest way to provide the neutral path [4]. On the other hand, in three-phase transformerless applications, the load neutral point can be simply connected to the midpoint of the dc-link [5]. This topology needs a very high capacitance in the dc-link to limit the dc voltage fluctuations due to the load neutral current flowing through the dc-link capacitors [4], [5].

A three-phase four-leg inverter is the most advanced solution to provide the neutral wire for the load connection. This structure offers several advantages, especially for the transformerless systems, such as utilizing the DC-Link voltage more effectively in comparison to the three phase three-leg topology (15% higher), having lower dc-link voltage ripple, needing lower dc-link capacitance, and having lower size, weight, and cost [6], [7]. The four-leg inverter has been used widely in both grid-connected and stand-alone applications [8], [9]. In grid-connected applications, the four-leg inverter is followed by an inductive filter and the injected current to the grid is regulated. Shunt active power filters, distributed static compensators (DSTATCOMs) [10], series active power filters, dynamic voltage restorers (DVRs) [11], active front-end rectifiers [12], and common-mode active filters [13] are examples of gird-connected applications [14], [15]. In stand-alone applications, the four-leg inverter is equipped with an *LC* filter and the output voltage is regulated. Examples of stand-alone applications are UPSs [16] and electric motor drives [17], [18]. A general application example of the four-leg inverter in a stand-alone power system is shown in Fig. 1.

Several techniques have already been proposed to control the four-leg inverter. Nonlinear control methods, such as pole placement [19], variable structure [20], and sliding mode control [21], mainly suffer from complexity, which makes their implementation very complicated. In addition, the repetitive and resonant controllers can also be used to achieve sinusoidal output voltages with a fixed switching frequency [22]–[24].

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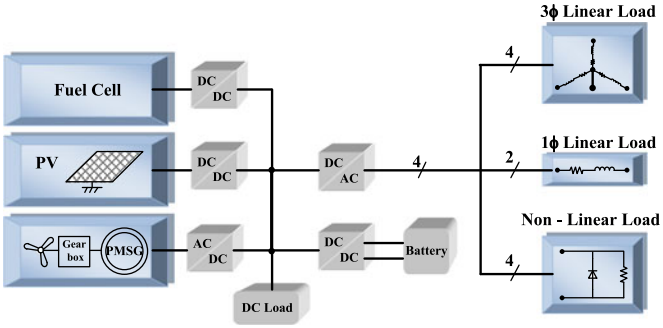

Fig. 1. Application example of the stand-alone power system with four-leg inverters.

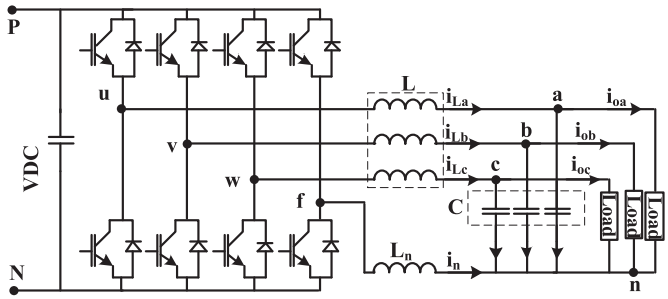

Fig. 2. Power circuit of the four-leg inverter with output *LC* filter and neutral leg inductor.

The model predictive control (MPC) is another control method that is also proposed for the four-leg inverters [3], [7], [8], [25]. The MPC has a simple structure and good performance, but it needs an accurate model of the converter system, which makes it highly sensitive to model uncertainties and parameter mismatches. Also, the switching frequency is variable. In addition, the proposed method in [3] needs to calculate a cost function for 16 possible switching vectors to select the optimum one among them. These calculations impose a high computational burden. Moreover, in [3] and in order to reduce the switching frequency of the fourth leg, and consequently, its switching losses, not only a higher value for the L_n should be employed but also, a software solution was proposed, which imposes additional computational burden.

The deadbeat (DB) controller is an attractive technique for discrete-time control platforms [26]–[28]. Theoretically, the DB controller places all the closed-loop poles at the origin of the z-plane [26], achieving the fastest possible dynamic performance. The main requirement associated with the DB controller to show its good performance is the model of the system, which should be correct and accurate. The power circuit of the four-leg inverter with the output *LC* filter and the neutral line inductor is depicted in Fig. 2. The fourth leg inductor is intended to provide more attenuation of the switching harmonics and to reduce the current rating of the fourth leg switches, at either standard operation or short-circuit condition. To model the four-leg inverter, several studies have been carried out [3], [7]–[9], [21], [26]. In most these studies, the neutral inductor is not considered in the modeling of the four-leg converter. In other words, since there is no neutral leg inductor, the four-leg inverter is considered as three independent single-phase inverters. In addition, the model presented in [3] is just used for the estimation of the load voltage, and consequently, it seems that the exact modeling of the four-leg inverter and investigating the effect of the neutral leg inductor is necessary.

In this paper, a simple model for the four-leg inverter with the output *LC* filter and the neutral inductor is presented. It will be shown that the presence of the neutral leg inductor introduces a strong coupling among different phases. This coupling makes the controller design and performance analysis somewhat complicated. A simple solution to eliminate this coupling effect is proposed in this paper. After that and based on the decoupled equations, a new DB controller is proposed for the four-leg inverter. Simulations in MATLAB/SIMULINK and experimental results on a 3-kW test rig are provided to confirm the validity of theoretical achievements.

This paper is organized as follows. The model of the four-leg inverter with the neutral inductor is presented in Section II, which also proposes a simple decoupling technique. In Section III, the proposed DB control system is proposed based on the decoupled model. Performance evaluation with simulation and experimental results is presented in Section IV. Section V concludes this paper.

II. System Modeling

A. System Description

The four-leg inverter with the output *LC* filter and the neutral inductor is shown in Fig. 2.

The midpoint of the fourth leg (f) is connected to the load neutral point (n) through an inductor L_n. This connection provides a path for the zero-component of the load current. For the converter of Fig. 2, the average generated voltages during a switching period, v_{uN}, v_{vN}, v_{wN}, and v_{fN}, are

$$\begin{bmatrix} v_{uN} \\ v_{vN} \\ v_{wN} \\ v_{fN} \end{bmatrix} = \text{VDC} \begin{bmatrix} d_{uN} \\ d_{vN} \\ d_{wN} \\ d_{fN} \end{bmatrix} \tag{1}$$

where d_{uN}, d_{vN}, d_{wN}, and d_{fN} are the duty cycles of each phase according to the negative point of the dc-Link. Based on (1), each phase voltage with respect to the fourth leg can be defined as

$$\begin{bmatrix} v_{uf} \\ v_{vf} \\ v_{wf} \end{bmatrix} = \text{VDC} \begin{bmatrix} d_{uN} - d_{fN} \\ d_{vN} - d_{fN} \\ d_{wN} - d_{fN} \end{bmatrix}. \tag{2}$$

Applying the Kirchhoff's voltage law at the output of the inverter, the following equation is obtained:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{uf} \\ v_{vf} \\ v_{wf} \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \begin{bmatrix} L_n & 0 & 0 \\ 0 & L_n & 0 \\ 0 & 0 & L_n \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix}. \tag{3}$$

It is worth mentioning that to simplify the overall model of the system, the effect of the series resistance of the inductors is neglected. It is mainly due to the small values of these resistances compared to the inductor impedances. Also, by using the Kirchhoff's current law at the output node of the inverter, the following equations are obtained:

$$\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} + \begin{bmatrix} C & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{4}$$

$$i_n + i_{La} + i_{Lb} + i_{Lc} = 0. \tag{5}$$

Replacing (5) in (3) and (4) and after some calculations, the state equations of the system are derived as (6) and (7). It is worth mentioning that the voltages of the output capacitors are equal to the load voltages.

$$\frac{d}{dt} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \frac{1}{L+3L_n} \begin{bmatrix} 1+\frac{2L_n}{L} & -\frac{L_n}{L} & -\frac{L_n}{L} \\ -\frac{L_n}{L} & 1+\frac{2L_n}{L} & -\frac{L_n}{L} \\ -\frac{L_n}{L} & -\frac{L_n}{L} & 1+\frac{2L_n}{L} \end{bmatrix} \times \begin{bmatrix} V_{uf}-V_{an} \\ V_{vf}-V_{bn} \\ V_{wf}-V_{cn} \end{bmatrix} \tag{6}$$

$$\frac{d}{dt} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{C} \begin{bmatrix} i_{La}-i_{oa} \\ i_{Lb}-i_{ob} \\ i_{Lc}-i_{oc} \end{bmatrix}. \tag{7}$$

According to (6), it is evident that there is a high level of coupling among the currents of different phases. This coupling is proportional to the L_n/L ratio. Hence, the source of this coupling is the neutral leg inductor. Since the phase currents are strongly coupled to each other, the voltage equations are also coupled. This makes the analysis and design of the controller a difficult task.

B. Decoupled State Equations

The state equations of the four-leg inverter with the output *LC* filter and the neutral leg inductor are coupled to each other in the natural (*abc*) reference frame. In this paper, it is proposed to transform the state equations from the *abc* to the stationary ($\alpha\beta\gamma$) reference frame. It will be shown that this simple transformation will successfully decouple the state equations.

Each three-phase variable can be transformed from the *abc* reference frame to the $\alpha\beta\gamma$ reference frame using the transformation matrix T defined as

$$T = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{8}$$

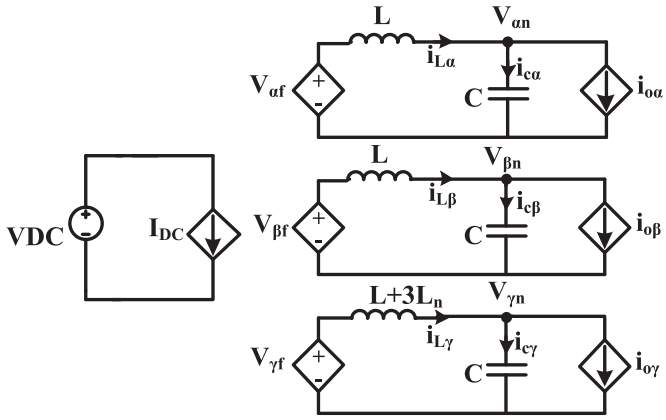

Fig. 3. Decoupled model of the four-leg converter system in the $\alpha\beta\gamma$ reference frame.

Multiplying both sides of (6) by (8) yields

$$\frac{d}{dt} \underbrace{T \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}}_{G} = T \frac{1}{L+3L_n} \times \begin{bmatrix} 1+\frac{2L_n}{L} & -\frac{L_n}{L} & -\frac{L_n}{L} \\ -\frac{L_n}{L} & 1+\frac{2L_n}{L} & -\frac{L_n}{L} \\ -\frac{L_n}{L} & -\frac{L_n}{L} & 1+\frac{2L_n}{L} \end{bmatrix} \begin{bmatrix} V_{uf}-V_{an} \\ V_{vf}-V_{bn} \\ V_{wf}-V_{cn} \end{bmatrix}. \tag{9}$$

where

$$G = \begin{bmatrix} i_{L\alpha} & i_{L\beta} & i_{L\gamma} \end{bmatrix}^T. \tag{10}$$

The right-hand side of (9) can also be readily calculated, which results in

$$\frac{d}{dt} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L\gamma} \end{bmatrix} = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L+3L_n} \end{bmatrix} \begin{bmatrix} V_{\alpha f}-V_{\alpha n} \\ V_{\beta f}-V_{\beta n} \\ V_{\gamma f}-V_{\gamma n} \end{bmatrix} \tag{11}$$

where $(V_{\alpha f}, V_{\beta f}, V_{\gamma f})$ and $(V_{\alpha n}, V_{\beta n}, V_{\gamma n})$ denote the inverter and the load voltages in the $\alpha\beta\gamma$ reference frame, respectively. In addition, multiplying both sides of (7) by (8), transforms all the variables from the *abc* to the $\alpha\beta\gamma$ reference frame as presented in the following equation:

$$\frac{d}{dt} \begin{bmatrix} V_{\alpha n} \\ V_{\beta n} \\ V_{\gamma n} \end{bmatrix} = \frac{1}{C} \begin{bmatrix} i_{L\alpha}-i_{o\alpha} \\ i_{L\beta}-i_{o\beta} \\ i_{L\gamma}-i_{o\gamma} \end{bmatrix}. \tag{12}$$

According to (11) and (12), the overall model of the converter system in the $\alpha\beta\gamma$ reference frame is shown in Fig. 3. It is evident that all state variables are decoupled from each other. It is a very important achievement, because lets design the controllers for α, β, and γ components independently with no effect on each other.

III. DB Controller

The DB control uses the system model and the measured and reference values at the current sampling instant (k) to calculate

the proper reference quantities for the start of the following sampling period (instant *k+1*). Therefore, the control variable will be set at its reference value at the end of this sampling period (instant *k+2*). This procedure ensures that there are only two sampling period delays between the input reference variation and the output quantity change. In other words, the DB controller places all the closed-loop system poles at the origin of the *z*-plane. This leads to a fast dynamic response for a digital control implementation. To drive the DB control law, it is essential to initially present the model of the system. The final equations of the four-leg inverter in the $\alpha\beta\gamma$ reference frame are given in (11) and (12). Since these equations are completely decoupled from each other, the analysis and calculations for one component is the same for the two others. In this paper, the DB control law is derived for the α component, which is applicable to β and γ components too.

According to (11) and (12), the state equations of the system for the α component can be rearranged as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L\alpha} \\ V_{\alpha n} \end{bmatrix} = A\begin{bmatrix} i_{L\alpha} \\ V_{\alpha n} \end{bmatrix} + BV_{\alpha f} + Ei_{o\alpha} \tag{13}$$

where

$$A = \begin{bmatrix} 0 & \dfrac{-1}{L} \\ \dfrac{1}{C} & 0 \end{bmatrix},\ B = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \text{ and } E = \begin{bmatrix} 0 \\ \dfrac{-1}{C} \end{bmatrix}.$$

In (13), $V_{\alpha f}$ and $i_{o\alpha}$ are considered as the input and the disturbance to the system, respectively. If the sampling frequency is high enough ($f_s/f >> 20$), then the backward approximation can be used and the derivatives can be estimated from the sampled variables as

$$\begin{aligned} \frac{di_{L\alpha}}{dt} &= \frac{i_{L\alpha}(k+1) - i_{L\alpha}(k)}{T_s} \\ \frac{dV_{\alpha n}}{dt} &= \frac{V_{\alpha n}(k+1) - V_{\alpha n}(k)}{T_s} \end{aligned} \tag{14}$$

where T_s is the sampling time. Based on (13) and (14), the inductor current at $k+1$ sampling instant ($i_{L\alpha}(k+1)$) is given by

$$i_{L\alpha}(k+1) = i_{L\alpha}(k) + \frac{T_s}{L}(V_{\alpha f}(k) - V_{\alpha n}(k)). \tag{15}$$

Updating (15) for the next sampling period results in

$$i_{L\alpha}(k+2) = i_{L\alpha}(k+1) + \frac{T_s}{L}(V_{\alpha f}(k+1) - V_{\alpha n}(k+1)). \tag{16}$$

Assuming a linear estimation of $i_{L\alpha}(k+2)$ from the previous samples, (16) is rewritten as follows:

$$\begin{aligned} i_{L\alpha}(k+2) &= \underbrace{i_{L\alpha}(k+1) + i_{L\alpha}(k+1) - i_{L\alpha}(k)}_{i_{L\alpha}(k+2)} \\ &= i_{L\alpha}(k+1) + \frac{T_s}{L}(V_{\alpha f}(k+1) - V_{\alpha n}(k+1)) \end{aligned} \tag{17}$$

which can be simplified to

$$i_{L\alpha}(k+1) = i_{L\alpha}(k) + \frac{T_s}{L}(V_{\alpha f}(k+1) - V_{\alpha n}(k+1)). \tag{18}$$

For the DB controller with one sample period delay, all variables in the $k+1$ sampling instant can be considered as the reference values for the current instant. Thus, (18) is rewritten as follows:

$$i_{L\alpha,\mathrm{Ref}}(k) = i_{L\alpha}(k) + \frac{T_s}{L}(V_{\alpha f,\mathrm{Ref}}(k) - V^*_{\alpha n}(k)). \tag{19}$$

The final goal of the DB controller is to calculate the inverter reference voltage. Therefore, (19) is rearranged for $V_{\alpha f,\mathrm{Ref}}(k)$ $V_{\alpha f,\mathrm{Ref}}(k)$ as

$$V_{\alpha f,\mathrm{Ref}}(k) = V^*_{\alpha n}(k) + \frac{L}{T_s}(i_{L\alpha,\mathrm{Ref}}(k) - i_{L\alpha}(k)). \tag{20}$$

where $V^*_{\alpha n}$ is the load voltage reference value or the command input. Consequently, for calculating$V_{\alpha f,\mathrm{Ref}}$, the value of $i_{L\alpha,\mathrm{Ref}}$ should be determined. The same procedure, which was done for $V_{\alpha f,Ref}(k)$can be followed to calculate$i_{L\alpha,\mathrm{Ref}}$. According to (13) and (14), the second state variable ($V_{\alpha n}$) can be discretized as follows:

$$\frac{V_{\alpha n}(k+1) - V_{\alpha n}(k)}{T_s} = \frac{1}{C}i_{L\alpha}(k) - \frac{1}{C}i_{o\alpha}(k). \tag{21}$$

As previously mentioned, to calculate $i_{L\alpha,\mathrm{Ref}}$, (21) should be updated for the next sampling period as

$$\frac{V_{\alpha n}(k+2) - V_{\alpha n}(k+1)}{T_s} = \frac{1}{C}i_{L\alpha}(k+1) - \frac{1}{C}i_{o\alpha}(k+1). \tag{22}$$

Again, using the linear estimation for $V_{\alpha n}(k+2)$ results in

$$\begin{aligned} &\frac{\overbrace{V_{\alpha n}(k+1) + (V_{\alpha n}(k+1) - V_{\alpha n}(k))}^{V_{\alpha n}(k+2)} - V_{\alpha n}(k+1)}{T_s} \\ &= \frac{V_{\alpha n}(k+1) - V_{\alpha n}(k)}{T_s} = \frac{1}{C}i_{L\alpha}(k+1) - \frac{1}{C}i_{o\alpha}(k+1). \end{aligned} \tag{23}$$

Assuming that the load current ($i_{o\alpha}$) has almost no changes during a very small sampling period and replacing the values at $k+1$ with the reference values, (23) simplifies to

$$\frac{V^*_{\alpha n}(k) - V_{\alpha n}(k)}{T_s} = \frac{1}{C}i_{L\alpha,\mathrm{Ref}}(k) - \frac{1}{C}i_{o\alpha}(k). \tag{24}$$

Solving the aforementioned equation for $i_{L\alpha,\mathrm{Ref}}$, gives

$$i_{L\alpha,\mathrm{Ref}}(k) = i_{o\alpha}(k) + \frac{C}{T_s}(V^*_{\alpha n}(k) - V_{\alpha n}(k)). \tag{25}$$

The final equations of the proposed DB control law, (20) and (25), which are used to generate the reference signals for the PWM modulator, are rewritten as

$$\begin{aligned} V_{\alpha f,\mathrm{Ref}}(k) &= V^*_{\alpha n}(k) + \frac{L}{T_s}(i_{L\alpha,\mathrm{Ref}}(k) - i_{L\alpha}(k)) \\ i_{L\alpha,\mathrm{Ref}}(k) &= i_{o\alpha}(k) + \frac{C}{T_s}(V^*_{\alpha n}(k) - V_{\alpha n}(k)). \end{aligned} \tag{26}$$

As the aforementioned equation shows, the final equations of the proposed DB controller consist of only a few addition, subtraction, and multiplication operations. As a result, the control system has a very simple structure and low computational burden, especially when compared to the MPC methods, which

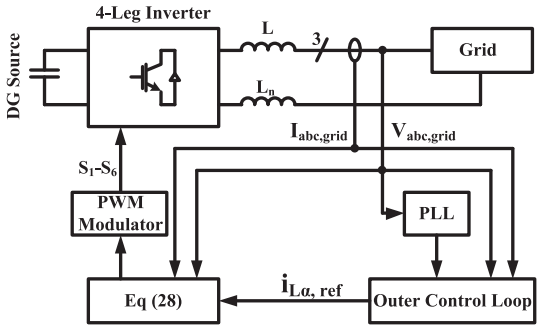

Fig. 4. Schematic of the grid-connected DG application.

TABLE I
SYSTEM PARAMETERS

Variable	Description	Value
P_o	Rated output power	3 [kW]
L	Filter inductance	880 [μH]
C	Filter capacitance	33 [μF]
L_n	Neutral filter inductance	440 [μH]
F_{sw}	Switching frequency	12 [kHz]
F_{samp}	Sampling frequency	12 [kHz]
V_o	Nominal output Voltage	110 [V_{rms}]
f_o	Nominal output voltage frequency	60 [Hz]
VDC	DC-Link voltage	390 [V]

simplifies the digital implementation. Besides, since the proposed DB controller calculates the inverter reference voltages, a PWM modulator with the fixed switching frequency can be used. By applying the same procedure for the β and γ components, the inverter reference voltages in the $\alpha\beta\gamma$ reference frame are achieved, which can be transformed back to the *abc* reference frame as

$$\begin{bmatrix} V_{uf,\mathrm{Ref}}(k) \\ V_{vf,\mathrm{Ref}}(k) \\ V_{wf,\mathrm{Ref}}(k) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} V_{\alpha f,\mathrm{Ref}}(k) \\ V_{\beta f,\mathrm{Ref}}(k) \\ V_{\gamma f,\mathrm{Ref}}(k) \end{bmatrix}. \quad (27)$$

As it is mentioned in Section III, the DB controller dynamics can be considered as only two pure sampling period delays. In other words, the DB controller places all the closed-loop system poles at the origin of the z-plane, and consequently, inside the unit circle, which ensures the stability of the control scheme. In the real condition, if the model of the system is accurate, the stability of the whole system will be guaranteed. In practice, the main issues that challenge the stability are model mismatches and parameter uncertainties. The effect of these two problems, under severe conditions, will be investigated in Section IV to confirm the stability over a wide range of possible mismatches and uncertainties.

It is worth noting that the proposed model and the DB control algorithm can be readily adapted to suit the grid-connected applications. Since grid-connected inverters are commonly followed by an *L*-type smoothing filter, (12) is not anymore valid and the load voltages are replaced in the algorithm by the grid

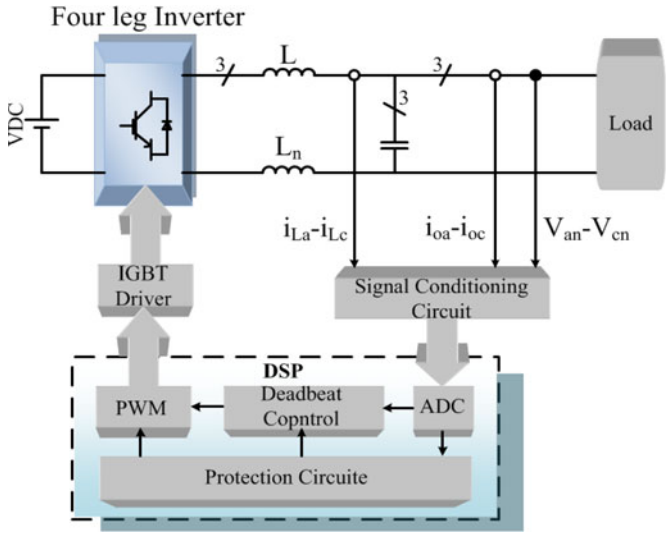

Fig. 5. Schematic of the whole control system.

Fig. 6. Photograph of the experimental test bench.

voltages. As a result, the model of the system simplifies to (11). To derive the DB control law, the same procedure starting from (14) can be followed until (20). Thus, (20) can be rearranged to generate the inverter reference voltages as follows:

$$V_{\alpha f,\mathrm{Ref}}(k) = V_{an}(k) + \frac{L}{T_s}(i_{L\alpha,\mathrm{Ref}}(k) - i_{L\alpha}(k)). \quad (28)$$

The reference inductor current injected to the grid is usually generated by the user or an outer control loop, such as the power controller or the dc-link voltage regulator. Also, a phase-locked loop must be used to synchronize the injected current with the grid voltage. A simple schematic of the grid-connected DG with the proposed control scheme is depicted in Fig. 4.

IV. PERFORMANCE EVALUATION

To validate the theoretical achievements and confirm the performance of the proposed control system, an extended simulation is done in MATLAB/SIMULINK software. Also, various experimental results are reported with the same parameters of the simulations, which are given in Table I.

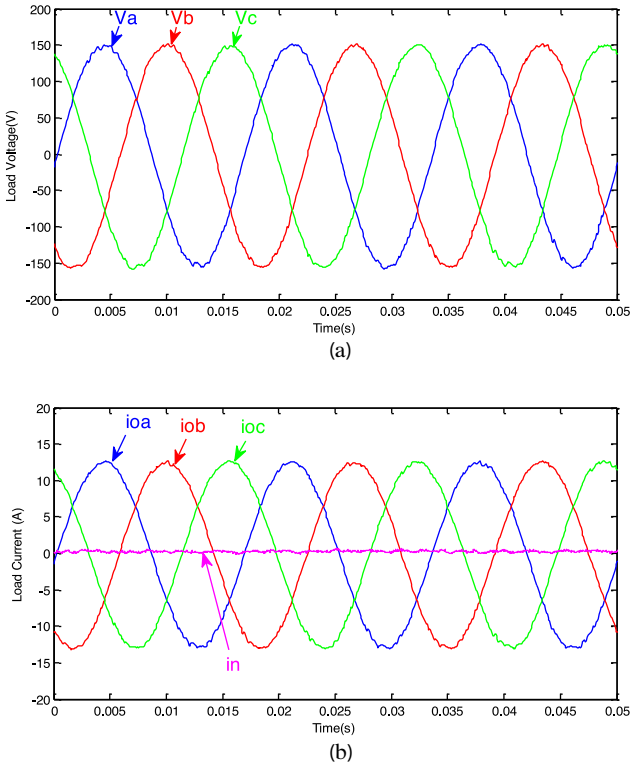

Fig. 7. Simulation results under nominal three phase linear load: (a) phase output voltages and (b) phases and neutral load currents.

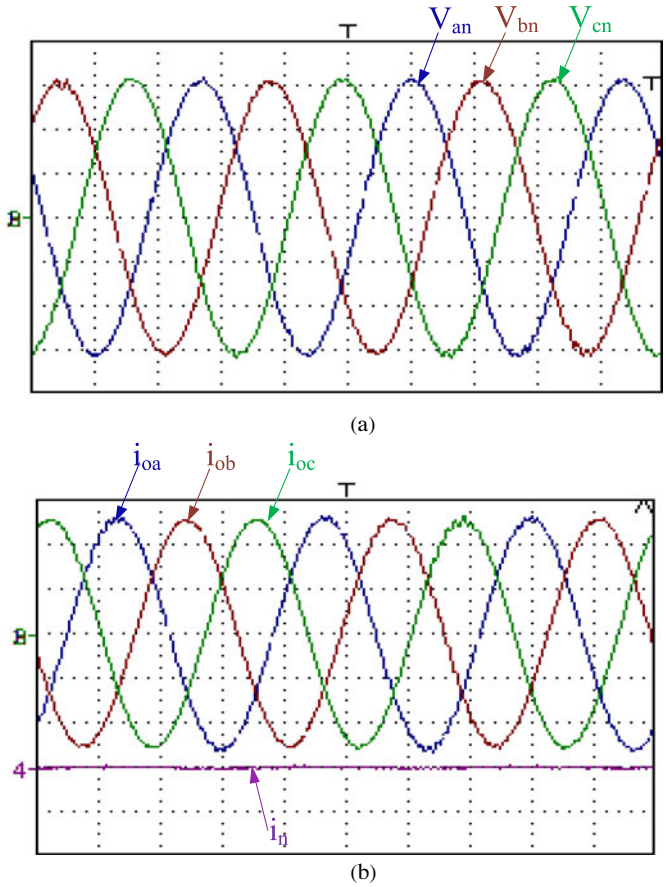

Fig. 8. Experimental results under nominal three-phase linear load: (a) ch1–ch3: phase output voltages (50 V/div) and (b) ch1–ch3: phase load currents, (5.5 A/div), ch4: neutral load current (13 A/div).

The schematic of the experimental setup and an image of the test rig are shown in Figs. 5 and 6, respectively. The control system is implemented on a developed board using TMS320F28335 DSP from Texas Instruments. A low-ripple dc voltage is provided by the three-phase diode rectifier at the input of the inverter.

The output *LC* filter is used to attenuate the switching and high-frequency ripples. The resonant frequency of the *LC* filter is usually selected about 10% of the switching frequency to limit the switching ripples to 1% [6]. Neglecting the L_n, the inductor current ripple at the worst case is determined as follows:

$$\text{Inductor Current Ripple} = \frac{\text{VDC}}{2 * L * F_{\text{sw}}} |D| * (1 - |D|) \quad (29)$$

where D is defined as the line to neutral duty ratio. Based on the maximum permitted current ripple, the value of L is selected from (29). Then, according to the resonant frequency and the reactive power limit (about 5% of the rated converter power), the proper value of C will be calculated. As already proposed in [29], the neutral inductor (L_n) is then selected as half of the three-phase inductors (L).

Various PWM modulation techniques have been proposed for the three-phase four-leg inverter, such as the carrier-based (like sinusoidal PWM (SPWM)) [30]–[32] and the 3-D space vector modulation (3D-SVM) [5], [33]–[35]. The SPWM provides a very simple structure and almost good load harmonics profile. Therefore, in this paper, the SPWM modulator with 12-kHz switching frequency is used to generate the gate signals from the reference voltages calculated from (26) and (27).

Different operating conditions with linear/nonlinear, balanced/unbalanced loads are tested to evaluate the effectiveness of the proposed DB controller.

In the first study, a three-phase linear load is connected to the output and both simulation and experimental results are shown in Figs.7 and 8.

Simulation and experimental results are in good accordance and the converter tracks the reference voltages precisely where the total harmonic distortion (THD) value of the output voltage is 1.1%. The voltage reference tracking error ($e_v[\%] = (V_{o,\text{measured}} - V_{o,\text{reference}})/V_{o,\text{reference}} \times 100$) is below 2%. Since the three-phase balanced currents are delivered to the load, the neutral current is nearly zero.

In the second study, the inverter is run under the single-phase linear loading condition and the results are shown in Fig. 9.

According to this figure, the load phase and neutral currents are the same and supplying an unbalanced load does not affect the output voltage quality. In this condition, the THD and e_v values of the load voltage are 1.2% and 1%, respectively, which

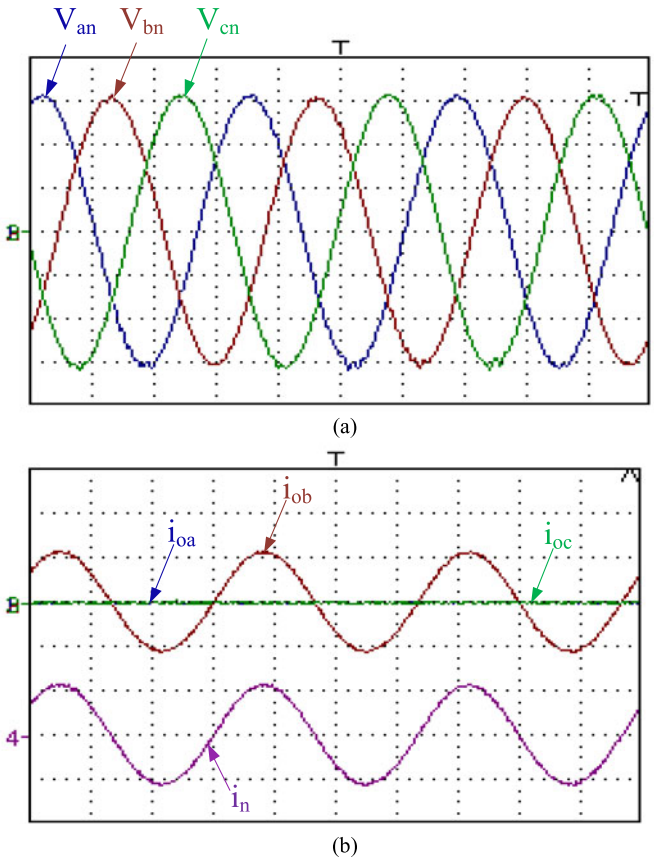

Fig. 9. Experimental results under single phase linear load: (a) ch1-ch3: phase output voltages (50 V/div) and (b) ch1-ch3: phase load currents, ch4: neutral load current (13 A/div).

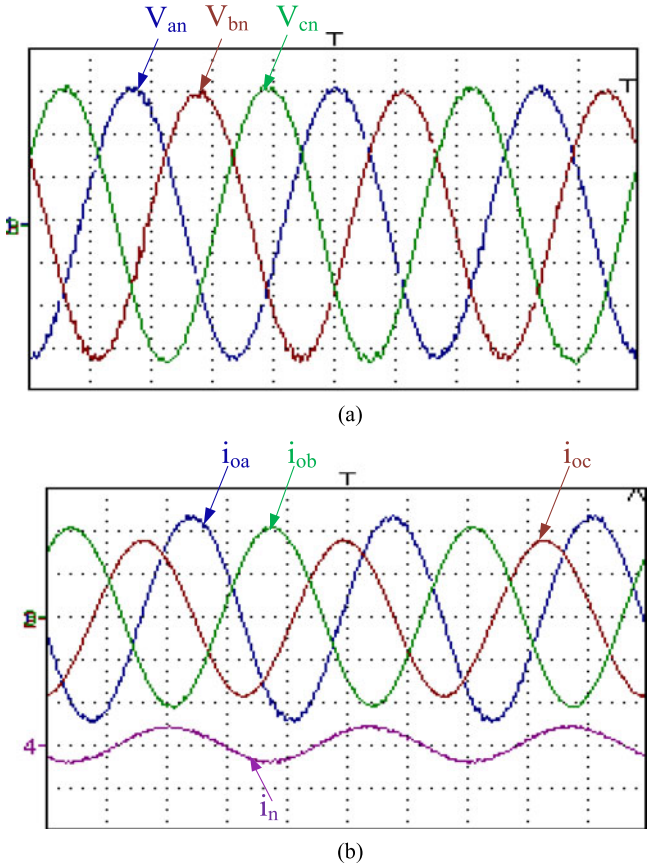

Fig. 10. Experimental results under three phase unbalanced RL load: (a) ch1–ch3: phase output voltages (50 V/div) and (b) ch1–ch3: phase load currents (5.5 A/div), ch4: neutral load current (13 A/div).

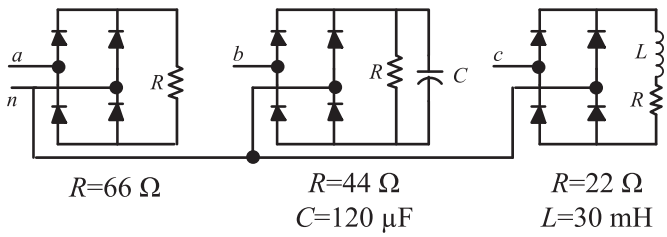

Fig. 11. Nonlinear load.

do not have a considerable change in comparison with the previous test. Thanks to the large capacitive filter in the dc side, the voltage ripple is too small. For the unbalanced condition (even single-phase loading), since the fourth leg provides a path for the zero current flow, the dc-link voltage ripple does not alter considerably. It is one of the advantages of the four-leg inverter compared to the conventional split dc-Link four-wire inverters.

Supplying different loads on each phase with different power factors is usual in stand-alone DG power systems. In this condition, the zero current path must be provided by the inverter. In the next study, the system is tested under three-phase unbalanced loads with different power factors and the results are shown in Fig. 10. The load power factor is 0.85 lagging for phase *a*, 0.9 lagging for phase *b*, and 1 for phase *c*. It is evident that the fourth leg provides the zero current path without any effect on the load voltages. Due to the unbalanced load, the neutral current is not zero flowing through the fourth leg. The THD and e_v values are less than 1.2% and 1.8%, respectively.

In stand-alone power systems, the output load may be in any kind of linear/nonlinear or balanced/unbalanced condition. Supplying nonlinear loads with a severe harmonic profile is inevitable in standalone power systems. To validate the performance of the proposed control system under the nonlinear loading condition, single-phase diode bridge rectifiers, which are shown in Fig. 11 are connected to different phases.

The output waveforms are reported in Fig. 12, where the control system precisely tracks the reference voltages even with severe harmonically polluted load currents. Just for phases *b* and *c*, a little voltage ripple is evident compared to phase *a*. The THD value for phases *a*, *b*, and *c* are 1.1%, 1.8%, and 1.4%, respectively.

To evaluate the dynamic performance of the control system, the transient waveforms in response to the no-load to nominal resistive load step change are shown in Fig. 13. According to this figure, the control system recovers the load voltage in a

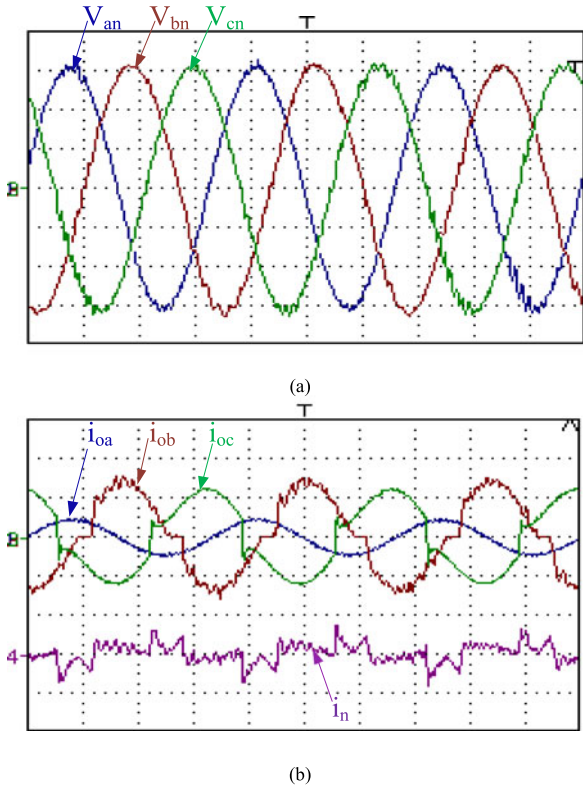

Fig. 12. Experimental results under three phase nonlinear load condition: (a) ch1–ch3: phase output voltages (50 V/div) and (b) ch1–ch3: phase load currents, ch4: neutral load current (13 A/div).

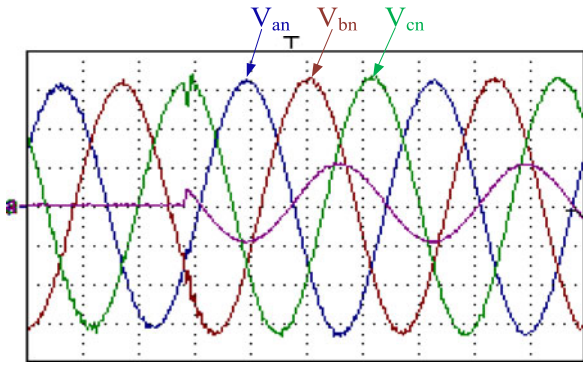

Fig. 13. Experimental results under three-phase no-load to nominal resistive load step change: (a) ch1–ch3: phase output voltages (50 V/div) and (b) ch4: phase-a load current (13 A/div).

few microseconds. Phase *c* experiences the most severe conditions, since the load step is done near the peak of the phase *c* load voltage. The control system compensates the voltage error with a small undershoot of about 12% of the nominal voltage.

A four-leg inverter should be able to generate unbalanced voltages whenever required, especially in applications such as DVRs. In this test, the unbalanced reference voltages; phase *a*: 110 V, phase *b*: 100 V, phase *c*: 90 V, are considered and the results are shown in Fig. 14. As the worst case of unbalances

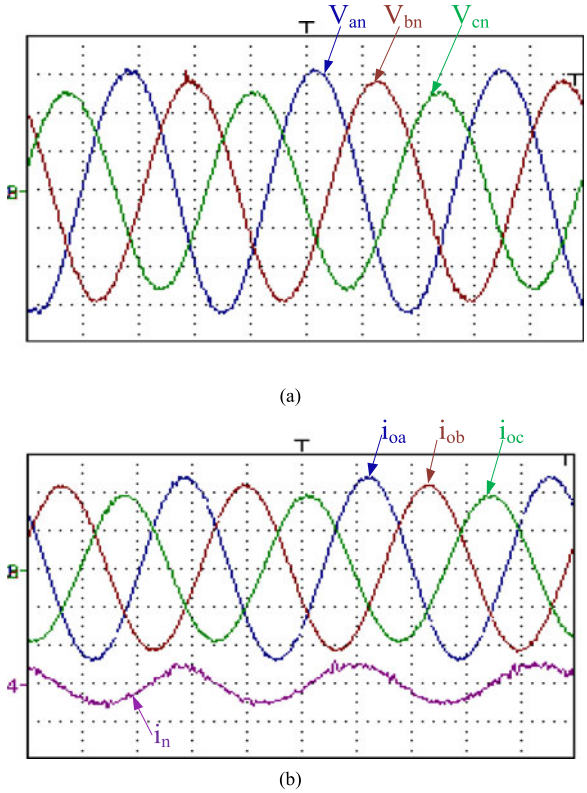

Fig. 14. Experimental results under three-phase unbalanced reference voltages: a) ch1–ch3: phase output voltages (50 V/div) and (b) ch1–ch3: phase load currents, ch4: neutral load current (5.5 A/div).

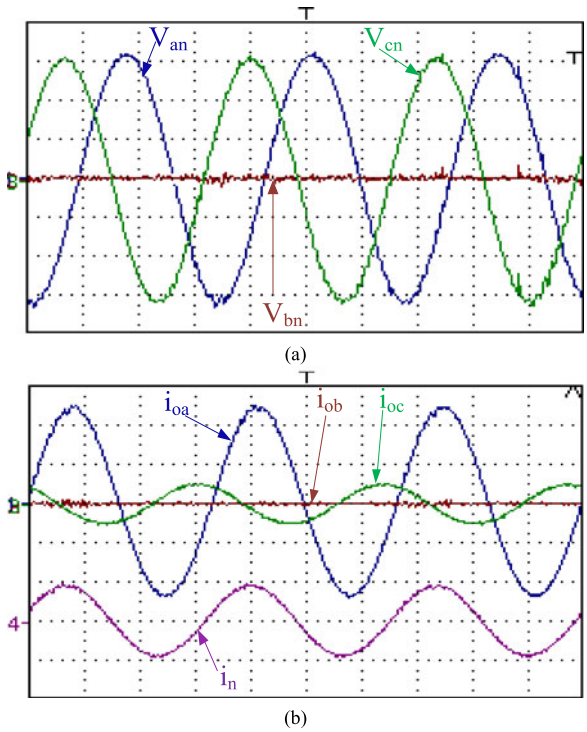

Fig. 15. Experimental results under three-phase unbalanced load with short circuit in phase *b*: (a) ch1–ch3: phase output voltages (50 V/div) and (b) ch1–ch3: phase load currents (5.5 A/div), ch4: neutral load current (13 A/div).

TABLE II
EXPERIMENTAL ANALYSIS WITH DIFFERENT SAMPLING FREQUENCIES

Sampling Frequency	8 kHz		10 kHz		12 kHz		15 kHz	
Parameters (%)	THD	e_v	THD	e_v	THD	e_v	THD	e_v
No Load	2.6	0	1.8	0	1.2	0	0.5	0
Full Linear Load	2.4	2.2	1.6	1.9	1.1	1.8	0.4	1.7

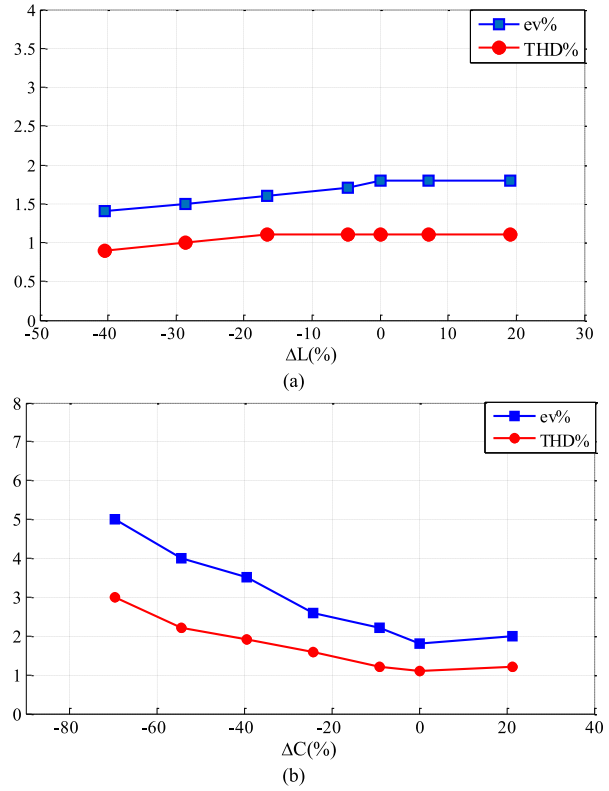

Fig. 16. Experimental evaluation of the THD% and e_v% with mismatches in (a) *L*, (b) *C*.

voltages, a short-circuit condition in phase *b* with unbalanced loads is also tested and the results are shown in Fig. 15. The proper performance of the converter system with small THD and e_v values is obvious. It is worth noting that based on the IEEE 1547 standard, the THD value should not exceed 5% and each harmonic up to 11th must have an amplitude lower than 4%. Also, according to IEC62040-3, the THD value must be lower than 8%. For all tests and conditions, reported here, the THD value of the load voltages does not exceed 1.8%, which is far below the standards requirements.

In another study and in order to evaluate the effect of the sampling frequency on the control performance, the steady-state tests are repeated with different sampling frequencies and the results are presented in Table II.

In this paper, the sampling and switching frequencies are the same. Generally, increasing the sampling frequency improves the accuracy of digital implementation of the control algorithm, mainly due to minimizing the effect of delays. However, the sampling frequency has to be limited in order to finish the calculation of the control algorithm within a sampling period. So, as illustrated in Table II, by increasing the sampling frequency, as already expected, the THD% value decreases as a result of increasing the switching frequency, as a result of improved filtering effect. On the other hand, the value of e_v is also decreased slightly.

As mentioned before, the DB controller needs the accurate model of the system to work properly. As a result, the performance of the proposed controller, considering the model parameter mismatches should be investigated. According to (26), the filter parameters, *C* and *L*, are the most important parameters in the proposed DB control law. Consequently, the performance of the controller, in terms of the THD and the e_v, in response to mismatches in these parameters is studied. The results for the inductance and capacitance mismatches are shown in Figs. 16(a) and (b), respectively.

Based on Fig. 16, it can be concluded that the performance of the proposed DB controller is not degraded even under a wide range of mismatches of the inductor values. The variations of the THD and the e_v against mismatches in the *C* value are more considerable when the *C* value is under estimated, however the THD is still below the standard limits.

V. CONCLUSION

The stand-alone DG systems, interfacing power electronic converters, are alternative efficient solutions to supply different remote loads. To supply both single- and three-phase ac loads, the fourth wire is mandatory. The three-phase four-leg inverter with the neutral inductor seems the best solution for such applications. In this paper, a decoupled model of the four-leg inverter was proposed, based on which, the DB control was proposed to control the output voltages of the inverter. The final DB control law is very simple to understand and implement. The switching frequency is constant, which simplifies the converter design and lets utilize advanced modulation techniques. Several experiments under different loading conditions were performed, which confirmed the superiority of the proposed scheme in generating balanced and highly sinusoidal voltages. Furthermore, the control system is robust against inductive and capacitive filter parameter mismatches.

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