

Investigation of the possibility of removing the grid side inductance from the *LLCL* filter circuit

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Abstract—It has been shown in the literature that in the grid connected converters, which uses trap based filters, like *LLCL*, the grid side inductance and therefore the filter size is effectively reduced. This paper with the goal of further reducing the filter size and cost, investigates the possibility of removing the grid side inductance of the *LLCL* filter considering a minimum value for the grid inductance. The proper range of other parameters of the *LLCL* filter is explored and a systematic design procedure for them is proposed, which ensures that the common practical filtering requirements are met. Simulation and experimental results confirm the effectiveness of the proposed filter design.

Keywords—*LLCL* filter; grid connected converter; filter design; grid inductance.

I. INTRODUCTION

The application of high order filters in grid-connected voltage source converters (VSCs) have recently become a common interest of researches because of their good attenuation performance with smaller size and lower cost [1]. Compared to the traditional *L* filter, the high order filters, such as the *LCL* and the *LLCL* have a very high attenuation at the switching harmonic frequency. The *LCL* filter offers a good attenuation by -60 dB/dec roll-off at high frequency against the *LLCL* filter with only -20 dB/dec roll-off. On the contrary, the *LLCL* filter can almost completely suppress the first switching sideband harmonics, which has the largest amplitude and smallest frequency among all switching sidebands. Therefore, the *LLCL* filter can effectively reduce the grid side inductance compared to the *LCL* filter and consequently reduce the size of the filter [2]–[4]. Additionally, it was shown in [5] that the size of the filter can be further reduced by using multiple *LC* traps instead of one trap of the *LLCL* filter. Combinations of the *LCL* filter with some *LC* traps are also presented in [6] and [7] and are called the *LCL-LC* and the *LTCL*, respectively, which can even more reduce the filter total inductance in addition to having -60 dB/dec roll-off.

The resonance arisen from the combination of capacitors and inductors in the high order filters challenges the stability of the current controlled grid-connected VSCs. In order to damp the resonance and gain stability in the closed-loop system several methods are already presented in the literature. Passive damping [4], active damping [8] and inherent damping [9] are the main stabilizing techniques, which use extra elements,

digital filters and digital implementation delays to damp the resonance of the high order filters.

Designing the filter parameters is also another main issue regarding the high order filters, which is addressed by many papers. An *LCL* filter design procedure is proposed in [1] by presenting practical filtering requirements. The converter side inductor is selected to limit the current ripple, the capacitor value is limited by its rated reactive power and then the grid side inductor is selected to further reduce the ripple in the grid current in comply with the standards, such as IEEE-1547.2-2008 and 519-1992 [10], [11]. Almost the same design procedures for the *LLCL* and the *LTCL* filters are proposed in [2] and [7], respectively.

It has been shown in [2], [5]–[7] that by using the *LC* traps, the grid side inductance and consequently the size of the filter can be effectively reduced. In this paper the possibility of further reducing the size of the filter by removing the grid side inductance of the *LLCL* filter considering a minimum grid inductance is investigated. The effect of removing the grid side inductor on the selection of other filter parameters with different minimum grid inductors is also explored. Filter parameters are calculated in a systematic manner to meet the common practical filtering requirements. In addition, the stability analysis of the closed-loop current controlled system using the simple inherent damping is also carried out.

II. MODELING OF *LLCL* FILTER

The structure of the grid-connected single phase VSC with the *LLCL* filter is shown in Fig. 1. The converter output voltage and current and the grid injected current are noted as v , i_1 and i_2 , respectively. The transfer function of the converter output voltage to the grid current can be simply derived as [2]

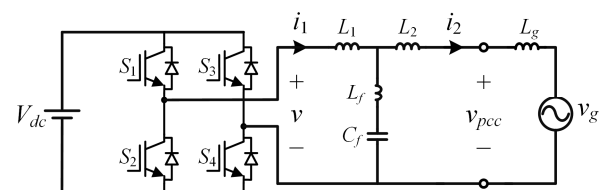


Fig. 1: Grid-connected single phase VSC.

$$G_{i2}(s) = \frac{i_2(s)}{v(s)} = \frac{C_f L_f s^2 + 1}{C_f [L_1 L_2' + (L_1 + L_2') L_f] s^3 + (L_1 + L_2') s} \quad (1)$$

$$= \frac{1}{(L_1 + L_2')(1 + L/L_f)} \frac{s^2 + \omega_f^2}{s(s^2 + \omega_{res}^2)}$$

where $L_2' = L_2 + L_g$ is the total grid side inductance, L is defined as $L_1 \parallel L_2'$ and ω_f and ω_{res} are the trap tuned frequency and the filter resonance frequency, respectively, which is defined as

$$\omega_f^2 = \frac{1}{C_f L_f} \quad (2)$$

$$\omega_{res}^2 = \frac{1}{C_f (L + L_f)}. \quad (3)$$

The frequency of trap, ω_f , is tuned at the first switching sideband. In the single phase VSC with the unipolar PWM, the switching sideband harmonics are located at even multiples of the switching frequency ($2\omega_{sw}$, $4\omega_{sw}$, ...). By adopting the asymmetrical sampling technique, the sampling frequency, ω_s , is twice the switching frequency ($\omega_s = 2\omega_{sw}$), consequently ω_f is set to ω_s [12].

III. LLCL FILTER DESIGN

In this section, the possibility of removing the grid side inductor L_2 from the filter circuit is investigated. The minimum value of grid inductance, which lets successfully meet the grid injected current requirements is determined and the proper values of other filter components, i.e. L_1 and C_f when L_2 is removed, are calculated in a systematic manner.

A. Practical Filtering Requirements

The filtering requirements for a grid connected VSC can be generally divided in three groups as follows [2].

- 1) In order to limit the reactive power of the capacitor, the maximum value of the capacitor is limited to a percent (usually 5%) of the converter base impedance, i.e.

$$C_{f,max} = \frac{0.05 P_{rated}}{\omega_1 V_{rated}^2} \quad (4)$$

where P_{rated} and V_{rated} are the rated power of the converter and the rms voltage of the grid, respectively.

- 2) In order to limit the converter current ripple (usually to 30-60% of the rated current) and consequently the current rating of semiconductor devices, a lower limit for the converter side inductor is defined as

$$L_{1,min} = \frac{V_{dc} T_s}{8 \Delta i_{1,max}} = \frac{V_{dc} T_s}{8(0.3 I_{P,rated})} \quad (5)$$

where $I_{P,rated}$ is the peak rated current of the converter.

- 3) Based on IEEE-1547.2-2008 standard, all harmonics higher than 35th order in the grid injected current must be lower than 0.3% of the rated current. Therefore, the amplitude of all switching sideband components must be restricted to 0.3%. Assuming that the first switching sideband is effectively suppressed by the $L_f C_f$ trap, the second switching sideband must be then limited as

$$(i_{2, sb2, max} = V_{sb2, max} |G_{i2}(s \approx j 2\omega_s)|) \leq 0.003 I_{P,rated} \quad (6)$$

where $i_{2, sb2, max}$ and $V_{sb2, max}$ are the maximum amplitudes of the second sideband of the grid current and the converter voltage, respectively.

B. Proper Range of L_1 and C_f with Removing L_2

The presence of a grid inductance with enough value lets eliminate the grid side inductor from the filter circuit without scarifying the above mentioned filtering requirements. The inductance of transmission lines and cables and also the leakage inductance of transformers are the main sources of the grid inductance. In the following the effect of removing L_2 on choosing other parameters of the filter, such as C_f , L_1 and ω_s with the goal of fulfilling the practical requirements of the filter is investigated and then a filter design procedure for this especial case is proposed.

Assuming that the filter resonance frequency is related to the sampling frequency as $\omega_{res} = k \omega_s$, then the capacitor value can be calculated from (3) as

$$C_f = \frac{1}{(k \omega_s)^2 (L_1 \parallel L_g + L_f)}. \quad (7)$$

Assuming that $L_g \ll L_1$ and using (2) and $\omega_f = \omega_s$, the capacitor value from (7) is approximated as

$$C_f \approx \frac{1/k^2 - 1}{L_g \omega_s^2}. \quad (8)$$

Fig. 2 shows the computed C_f with different values of k , ω_s and L_g . As expected, with increasing the sampling frequency and k (i.e. the resonance frequency) the required capacitance decreases. Also, this figure shows that for a given rated power and its corresponding maximum allowed capacitance (defined by (4)), which value for k and ω_s could be chosen. Moreover, for a grid with smaller L_g , higher k and ω_s is needed in order to meet the maximum capacitor limit (4). The intersection between computed C_f and maximum limit of capacitor shows the acceptable range for k and ω_s , which by removing C_f from (4) and (8) this range is calculated as

$$\frac{1/k^2 - 1}{L_g \omega_s^2} \leq \frac{0.05 P_{rated}}{\omega_1 V_{rated}^2}. \quad (9)$$

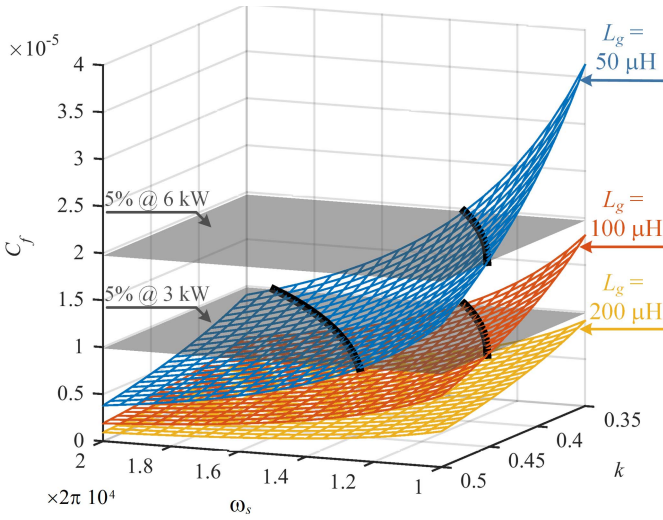


Fig. 3: Variations of C_f with k and ω_s .

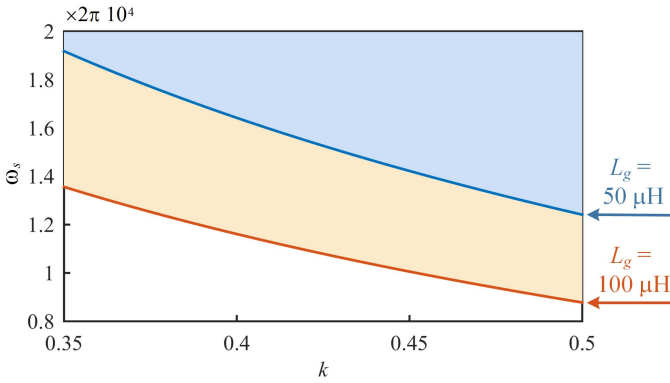


Fig. 4: Acceptable range of k and ω_s for a 3 kW converter.

The acceptable range of k and ω_s for a 3 kW converter for different grid inductances is plotted in Fig. 3.

On the other side, the grid injected current should meet the amplitude limitation of 0.3% for second sideband switching harmonics as (6). The high frequency characteristic of G_{i2} can be calculated as

$$G_{i2,HF}(s) = G_{i2}(s) \Big|_{s \rightarrow \infty} = \frac{1}{(L_1 + L_g)(1 + L_1 \parallel L_g / L_f)s} \quad (10)$$

Assuming that $L_g \ll L_1$ and using (2) the high frequency characteristic is approximated as

$$G_{i2,HF}(s) \approx \frac{1}{L_1(1 + L_g/L_f)s} = \frac{1}{L_1(1 + L_g C_f \omega_s^2)s} \quad (11)$$

The above equation shows that at high frequencies the LLCL filter behaves like a simple L filter with the inductance value of $L_1(1 + L_g/L_f)$. By substituting (11) into (6) the converter side inductance range is calculated as

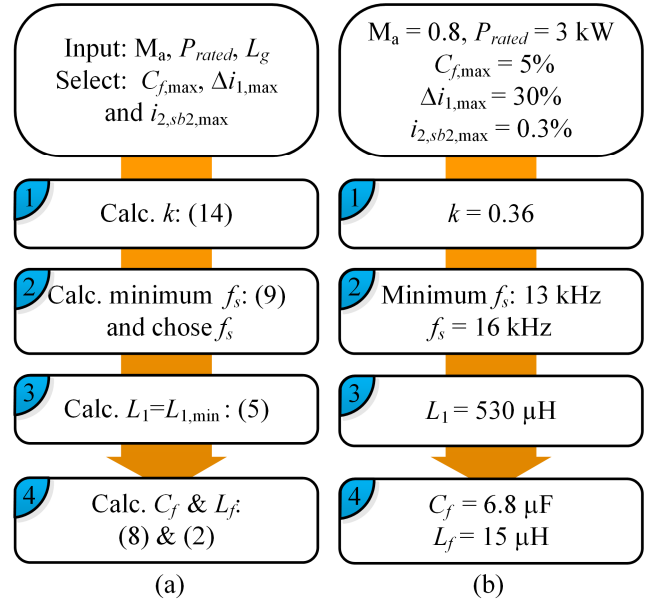


Fig. 2: Filter design flow (a) general case (b) an example.

$$L_1 \geq \frac{V_{sb2,max}}{(1 + L_g C_f \omega_s^2)(2\omega_s)(0.003 I_{P,rated})} \quad (12)$$

and by substituting (8) into (12), it simplifies to

$$L_1 \geq \frac{k^2 V_{sb2,max}}{(2\omega_s)(0.003 I_{P,rated})} \quad (13)$$

It is clear that, a smaller value for L_1 is achieved with increasing the sampling frequency and decreasing k . This calculated range of L_1 can be compared with the minimum limit of (5) as shown in (14), in which $V_{sb2,max}$ for modulation index $M_a = 0.8$ is $0.12 V_{dc}$ [12]. As it is clear, in order to satisfy the minimum limit for L_1 , the value of k should be selected higher than $1/\sqrt{7.64} = 0.36$.

$$\frac{L_1}{L_{1,min}} = \frac{0.12 \times 0.3}{0.003} \frac{2k^2}{\pi} = 7.64k^2 \quad (14)$$

C. Design Filter parameters

The proposed step-by-step design procedure and the following example are summarized as flowcharts in Fig. 4. In the filter design procedure, the minimum grid inductance is assumed to be 100 μH , the converter rated power is 3kW, the maximum capacitor value is 5%, the switching sideband current is limited to 0.3% (based on IEEE-1547) and it is assumed that $\Delta i_{1,max} = 30\%$. Usually the inductors are more bulky than capacitors of the filter, so, in order to reduce the size of the filter, the inductance should be selected as low as possible. The minimum allowable size for L_1 is achieved by selecting it equal to the minimum limit (5), which according to (14) results to $k = 0.36$. Based on (9) and as depicted in Fig. 3, in order to reach $k = 0.36$ without violating the capacitor

TABLE I
DESIGNED FILTER PARAMETERS

L_1	L_2	L_f	C_f	$k = \omega_{res}/\omega_s$
530 μ H (1%)	0	15 μ H	6.8 μ F (3.4%)	0.38

TABLE II
SYSTEM PARAMETERS

Parameter	Symbol	Value
VSC rated power	S_{rated}	3 kVA
Grid voltage/frequency	V_{rms}/f	220 V _{rms} /50 Hz
DC link voltage	V_{dc}	380 V
Switching frequency	f_{sw}	8 kHz
Sampling frequency	f_s	16 kHz

maximum limit of (4) the sampling frequency should be selected higher than 13 kHz, which here 16 kHz is selected (i.e. $f_{sw} = 8$ kHz). Then, the value of L_1 can be calculated from (5).

The value of C_f and consequently the value of L_f can be calculated from (8) and (2), respectively. The final chosen values for the filter parameters are listed in Table I. The resulted filter inductance and capacitance are 1% and 3.4% of their base values, respectively, which demonstrates the small size of the filter. Due to the approximation, the final calculated value for k is 0.38, which is slightly higher than the desired value of 0.36.

It should be noted that, the filter is designed for the worst case of grid inductance (i.e. its minimum), with increasing the grid inductance, however the $L_g \ll L_1$ approximation is weakened, but the attenuation level will increase and the filtering performance is not deteriorated.

As it can be seen in Fig. 2, the required capacitor for the especial case of a relatively low sampling/switching frequency is high. Therefore it could be concluded that the proposed method is practically suited for applications with a high switching frequency, which translates to the low to medium power applications.

IV. STABILITY ANALYSIS AND CURRENT CONTROLLER DESIGN

A. Resonance Stability

In the grid-connected VSC filtered by the high order filters, the instability arises due to the inherent resonance of the filter. As already mentioned, different methods are presented in order to damp the resonance and stabilize the closed-loop control system. Here, according to the resultant resonance frequency in the filter design procedure, the inherent damping or delay based stabilization method is used. In this method, the closed-loop system with the grid current feedback is stable if the resonance frequency lies inside the stable range of $\omega_s/6 < \omega_{res} < \omega_s/2$ ($1/6 < k < 1/2$). The resonance frequency of the designed filter with parameters listed in Table I is calculated as $0.38\omega_s$, which is inside the stable range and the single loop controlled system is stable. Although, the resonance frequency decreases with increasing L_g , which may lead to instability. The tolerable value of the grid inductance, for

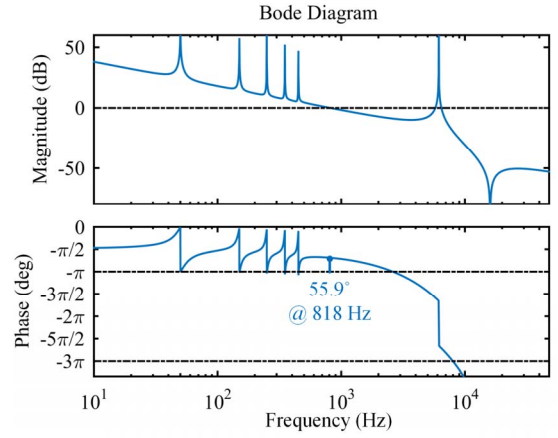


Fig. 5: Bode diagram of the system open-loop transfer function.

which the system remains stable can be calculated from (3) by setting $\omega_{res} = \omega_s/6$ as

$$L_{g,max} = \frac{L_1(1-1/6^2)}{C_f(L_1+L_f)(\omega_s/6)^2-1}. \quad (15)$$

With the designed filter parameters, the value of $L_{g,max}$ is calculated as 13 mH, which is really high and almost not expected in a real situation. Therefore the designed filter is stable in a wide range of grid inductance variations simply by the inherent damping method.

B. Current Controller Design

The proportional resonant (PR) controller with a harmonic compensation network (HC) is used to eliminate the steady state error of the fundamental component and compensate the low order harmonics in the grid current. The transfer function of the PR+HC in the s -domain is

$$G_c(s) = k_p + k_i \sum_{n=1,3,5,\dots} \frac{s}{s^2 + (n\omega_1)^2}. \quad (16)$$

In a digitally controlled system, a one and half sampling period delay ($T_d = 1.5T_s$) exists due to the computations and PWM update. Considering this delay, the controller gains are selected to achieve the decided gain crossover frequency ω_{gc} as, $k_p = \omega_{gc}(L_1 + L_g)$ and $k_i = 0.02\omega_{gc}$ [13]. With $\omega_{gc} = \omega_s/20$, $L_g = 100 \mu$ H and using HC resonant compensators at 3rd, 5th, 7th and 9th order harmonics the Bode diagram of the open loop current control system is plotted in Fig. 5. The attained phase margin is 55.9° , which is quite enough.

V. SIMULATION AND EXPERIMENTAL RESULTS

The filter design is verified by simulation and experimental tests. The system parameters are listed in Table II and the filter parameters are chosen through the proposed method and listed in Table I. The PR+HC controller, which is tuned at 1st, 3rd, 5th, 7th and 9th order harmonics is discretized by the impulse invariant method [14]. The system is simulated in PLECS software and a 3 kW laboratory prototype is developed for the

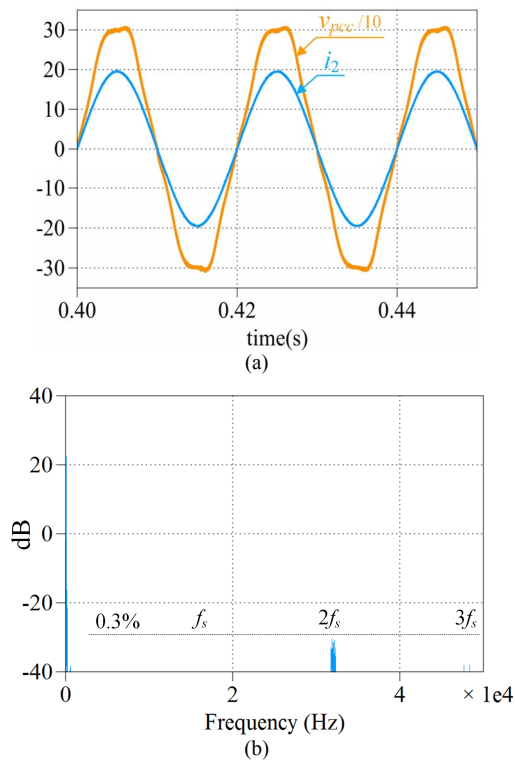


Fig. 6. Simulated steady-state results with minimum grid inductance (a) v_{pcc} and i_2 waveforms, (b) i_2 spectrum.

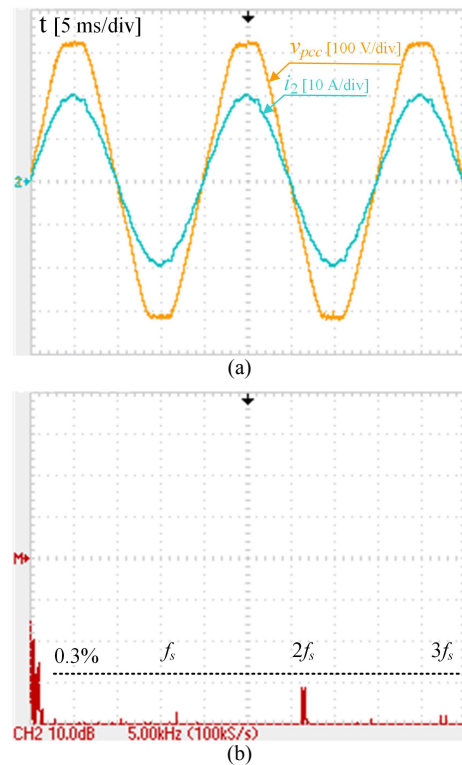


Fig. 7. Experimental steady-state results (with minimum grid inductance) (a) v_{pcc} and i_2 waveforms, (b) i_2 spectrum.

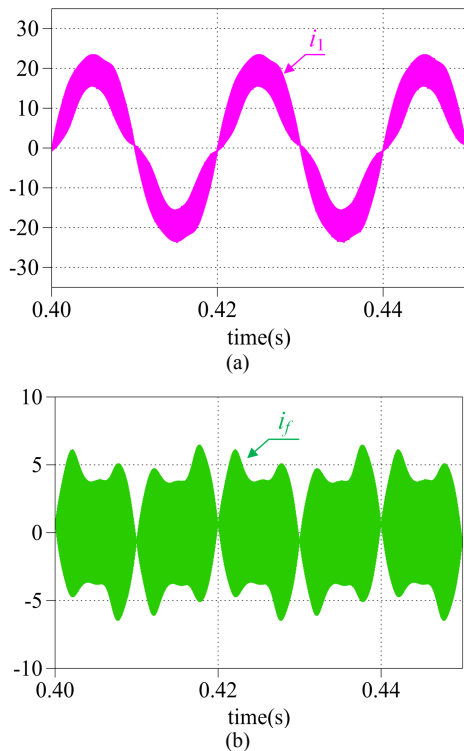


Fig. 8. Simulated waveforms of (a) converter current i_1 (b) trap current i_f .

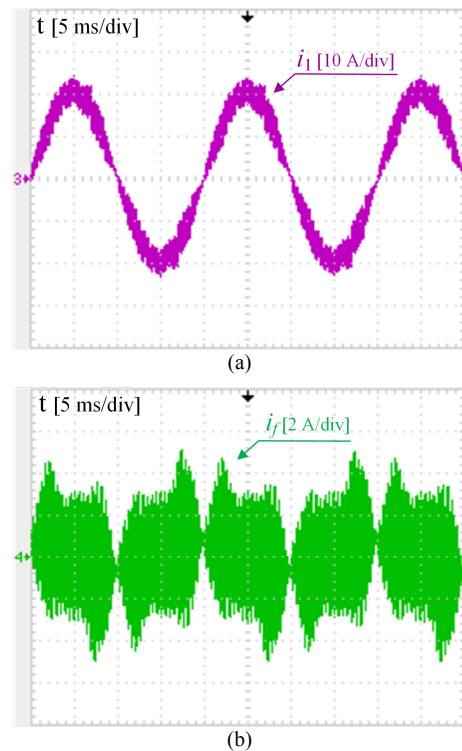


Fig. 9. Experimental waveforms of (a) converter current i_1 (b) trap current i_f .

experimental tests. The control algorithm is implemented on a Texas Instruments TMS320F28335 floating point digital signal controller.

The steady state simulated and experimental waveforms for the minimum value of grid inductance $L_g = 100 \mu\text{H}$ are shown in Figs. 6 and 7. Clearly, in both simulation and experiment the

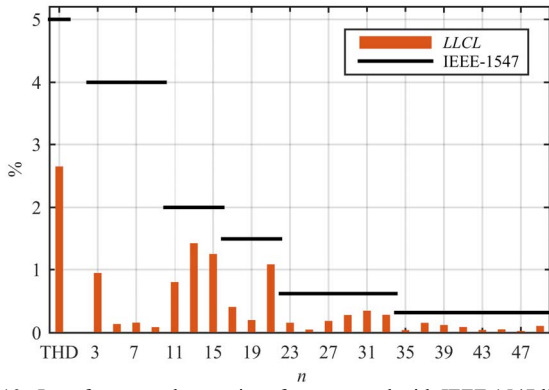


Fig. 10. Low frequency harmonics of i_2 compared with IEEE 1547 limits.

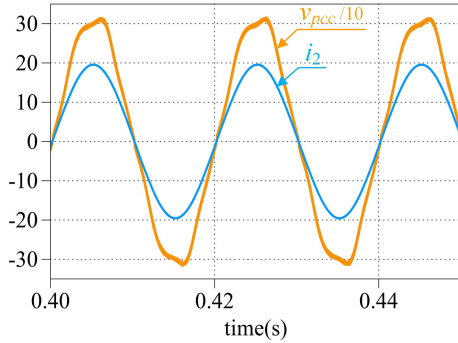


Fig. 11. Simulated steady-state results with $L_g = 2$ mH.

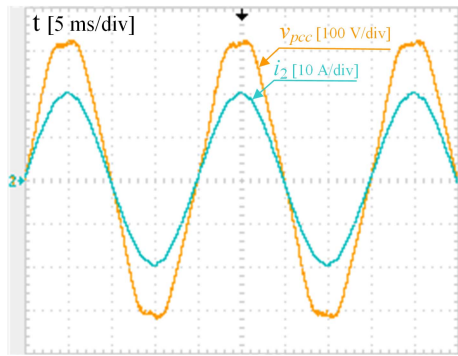


Fig. 12. Experimental steady-state results with $L_g = 2$ mH.

switching sidebands of the grid current are well attenuated below the 0.3% limit. The converter and trap branch currents are shown in Figs. 8 and 9. The maximum peak current ripple of the converter current is about 5.7A, which is almost equal to the designed value as $0.3I_{P,rated}$. The grid current THD for the experiment is 2.65%. The low frequency spectrum (the zoomed view of Fig. 7(b) for $n < 50$), compared with the IEEE-1547 limits is shown in Fig. 10. As mentioned in [15], decreasing the filter inductance results to increasing the low frequency components of the grid current, which are mainly generated from the grid voltage background harmonics and the non-idealities of the real system, such as the switching dead times and the inductor core nonlinearity and saturation. However, as it can be seen in Fig. 10, the designed filter successfully meets the IEEE-1547 standard limits for all low frequency

components. The waveforms in Figs. 11 and 12 for a large grid inductance ($L_g = 2$ mH) confirm the stability of the system even with increasing the grid inductance.

VI. CONCLUSION

This paper investigate the effect of removing the grid side inductance of the LLCL filter considering a minimum grid inductance on the filter parameter design. A specific range for the capacitor value depending on the converter rated power, the sampling and the resonance frequencies is obtained. Simulation and experimental results are presented to confirm the effectiveness of the designed filter to meet the practical filtering requirements.

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